THAYER SCHOOL OF ENGINEERING AT DARTMOUTH

Quanta Image Sensor (QIS) Concept and Progress

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October 1, 2014

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http://scien.stanford.edu/index.php/professor-eric-fossum/

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Presentation Plan

- Overview
- QIS Imaging Properties
- Jot Devices
- Readout Circuits
- Making Pixels from Jots
- Summary

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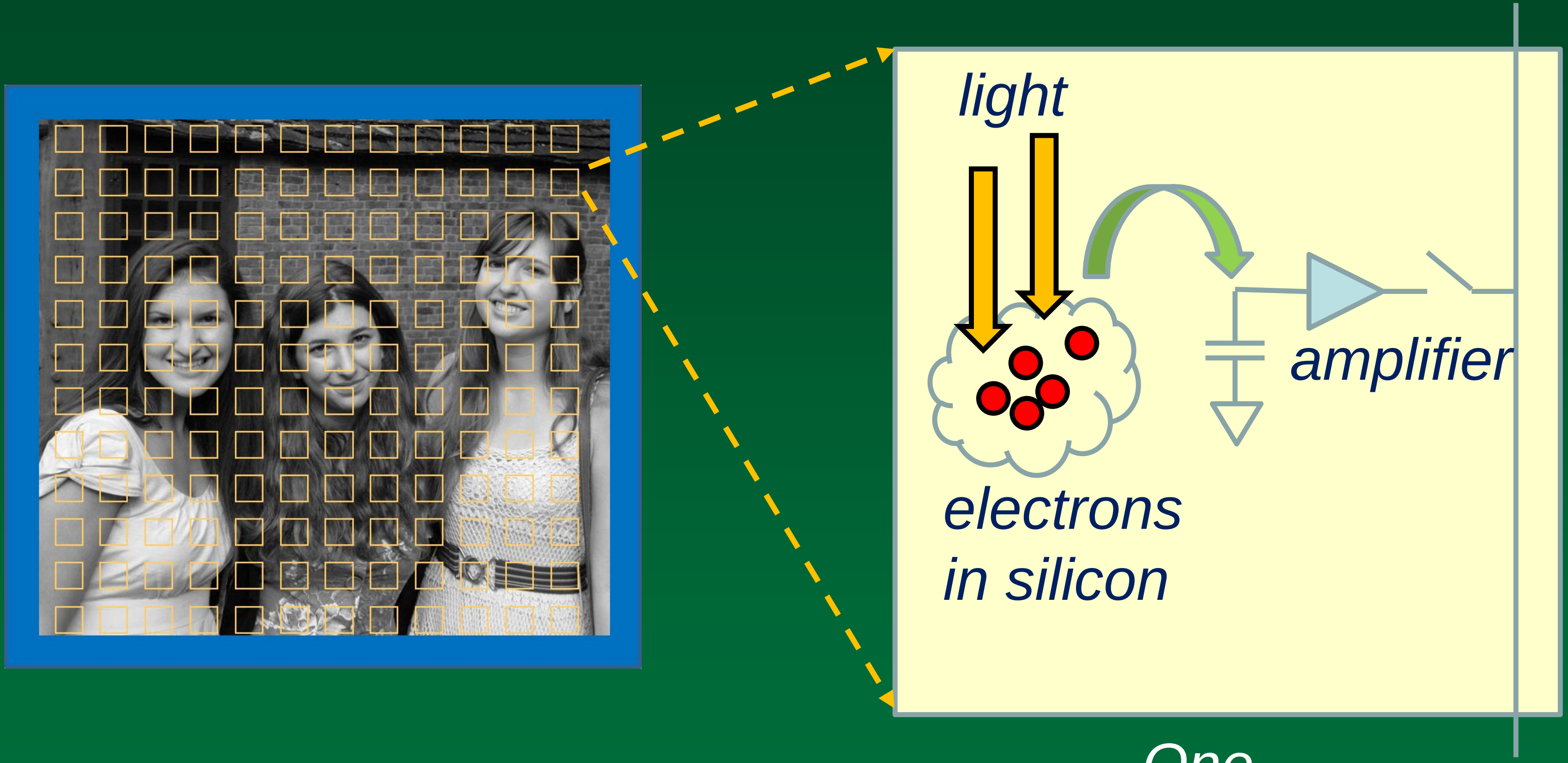
Active Pixels with Intra-Pixel Charge Transfer



One pixel

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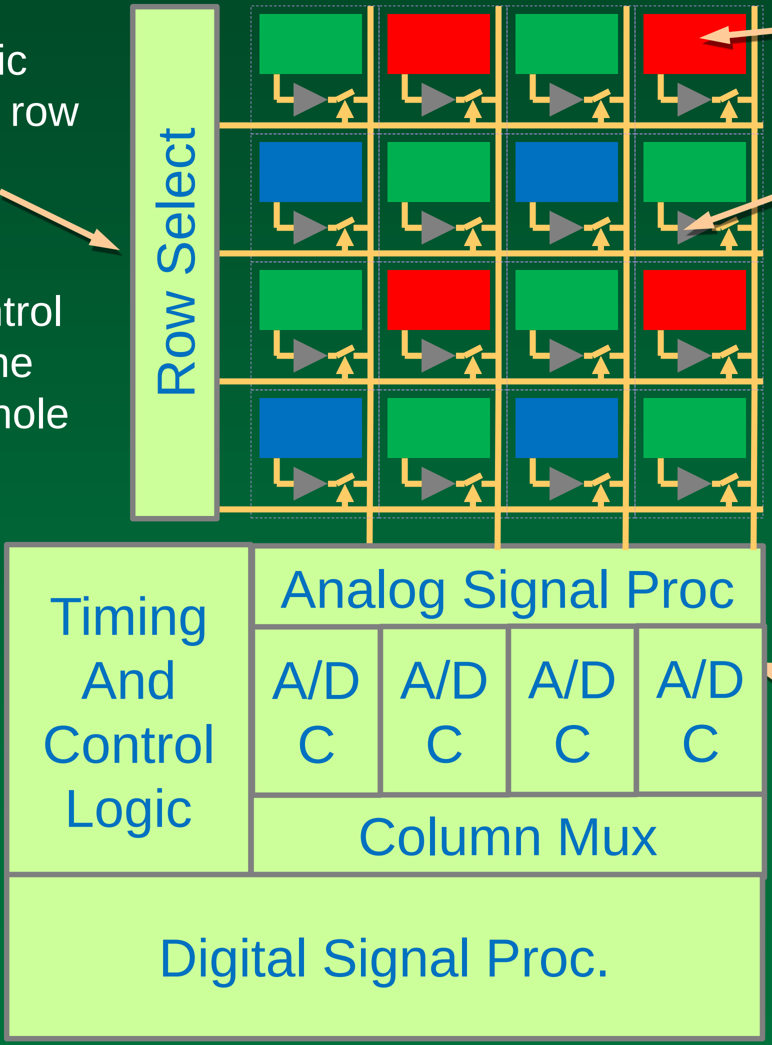
CMOS Active Pixel Sensor
2nd Generation Image Sensor

Read pixel signals out thru switches and wires



Row select logic chooses which row is selected for readout.

Timing and control logic controls the timing of the whole sensor

SoC functionality for color processing, compression, etc.

Photodetector converts photons to electrons

Amplifier converts electrons to voltage after intrapixel complete charge transfer

Analog signal processor suppresses noise and further amplifies signal

Analog-to-digital converters (ADC) convert signals from volts to bits (usually 10-12 bits resolution) in parallel

Column multiplexer used to scan ADC outputs

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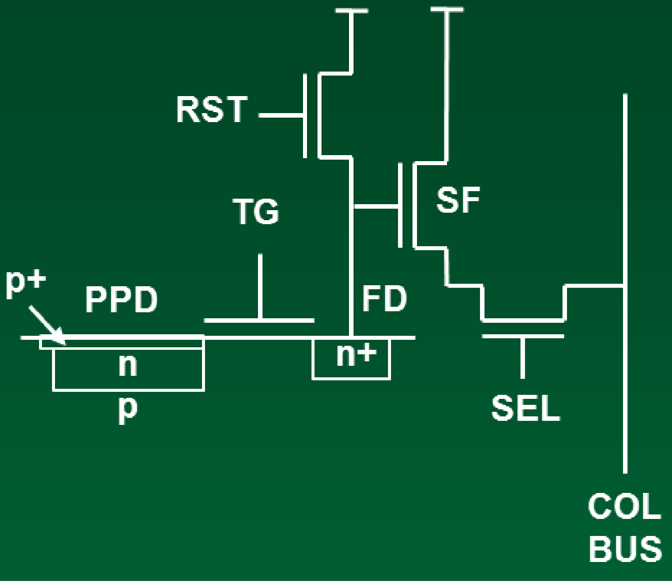
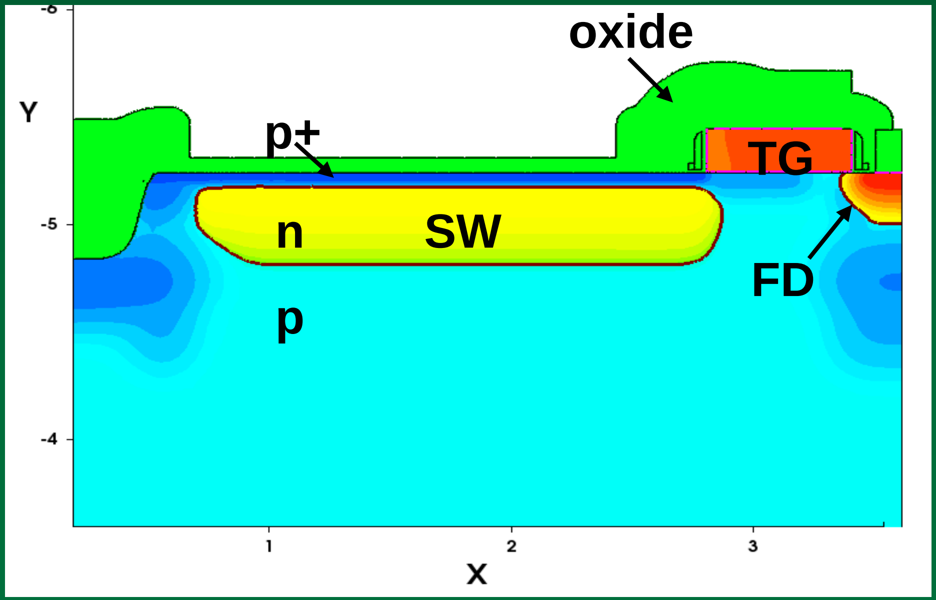
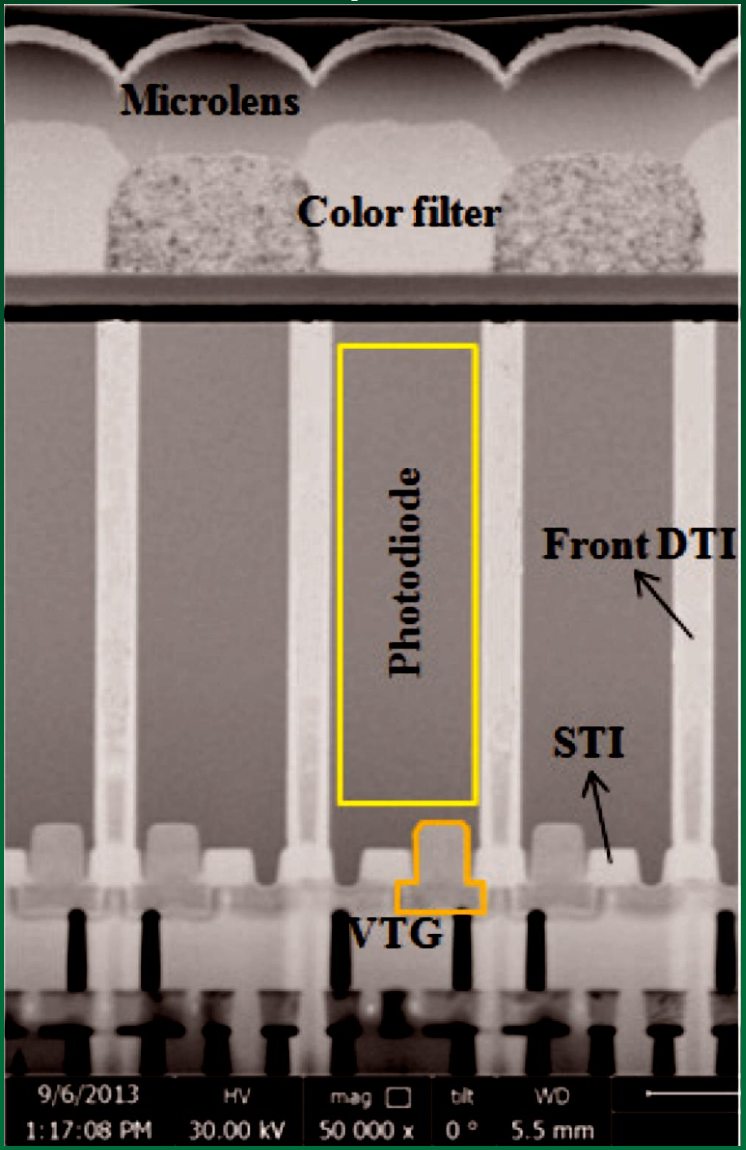
Pinned Photodiode Pixel





Samsung ISSCC 2013



E.R. Fossum and D. Hondongwa, A review of the pinned photodiode for CCD and CMOS image sensors, IEEE J. Electron Devices Society, vol 2(3) pp. 33-43 May 2014.

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Quanta Image Sensor

- Original goal for QIS was to take advantage of shrinking pixel size and make a very tiny, specialized pixel (“jot”) which could sense a single photoelectron.
- Jots would be readout by scanning at a high frame rate to avoid likelihood of multiple hits in the same jot and loss of accurate counting.
- Image pixels could be created by combining jot data over a local spatial and temporal region using image processing.
- The first proposed algorithm was the “digital film sensor” using a “grain” and “digital development” construct.

E.R. Fossum, *What to do with Sub-Diffraction-Limit (SDL) Pixels? – A Proposal for a Gigapixel Digital Film Sensor (DFS),* Proc. Of the 2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Karuizawa, Japan, June 2005

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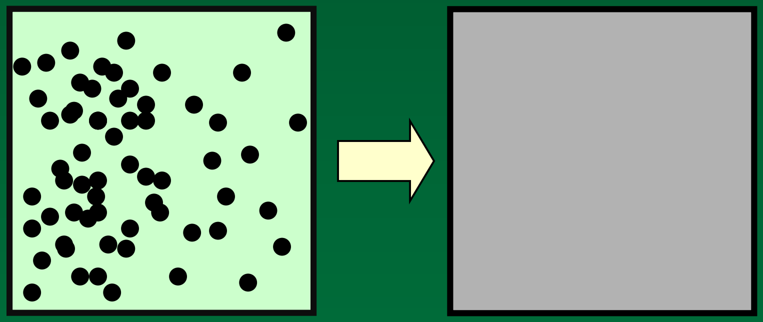
The Paradigm Shift

Current paradigm:

- We collect photons for a predetermined amount of time in a silicon “rainbucket” determined by physical size and capacity of silicon pixel.

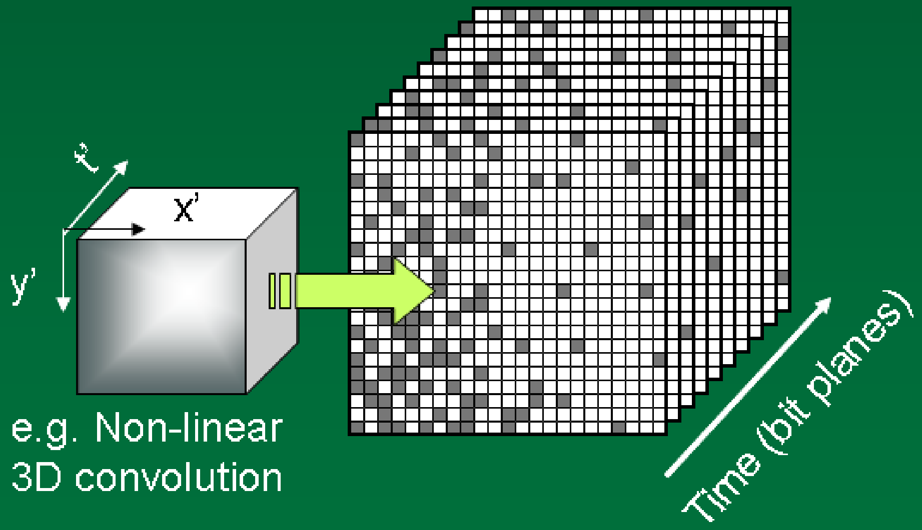
New QIS paradigm:

- Detect each photoelectron using jots, creating a binary bit plane for each time slice, and then digitally form image by digital convolution over X,Y, t



One sensor pixel

One image pixel



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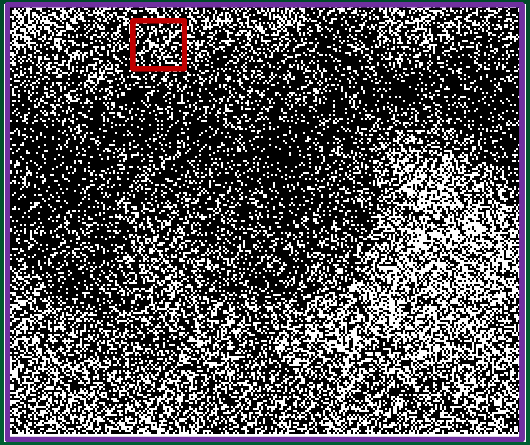
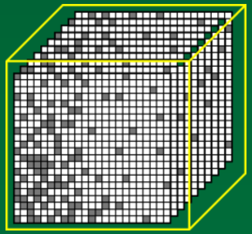
Pixels from Jots (Simulation)





Simplest

$$\sum_{X'Y't'} j(X,Y,t)$$

16x16x16 “cubicle”

$$0 \leq S \leq 4096$$

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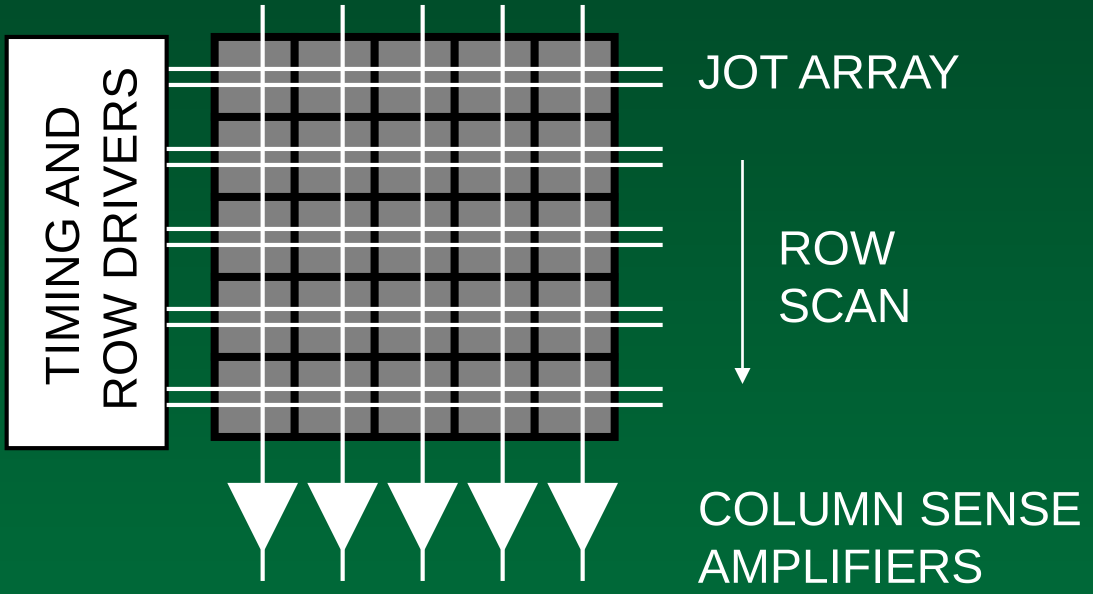
QIS Core Architecture



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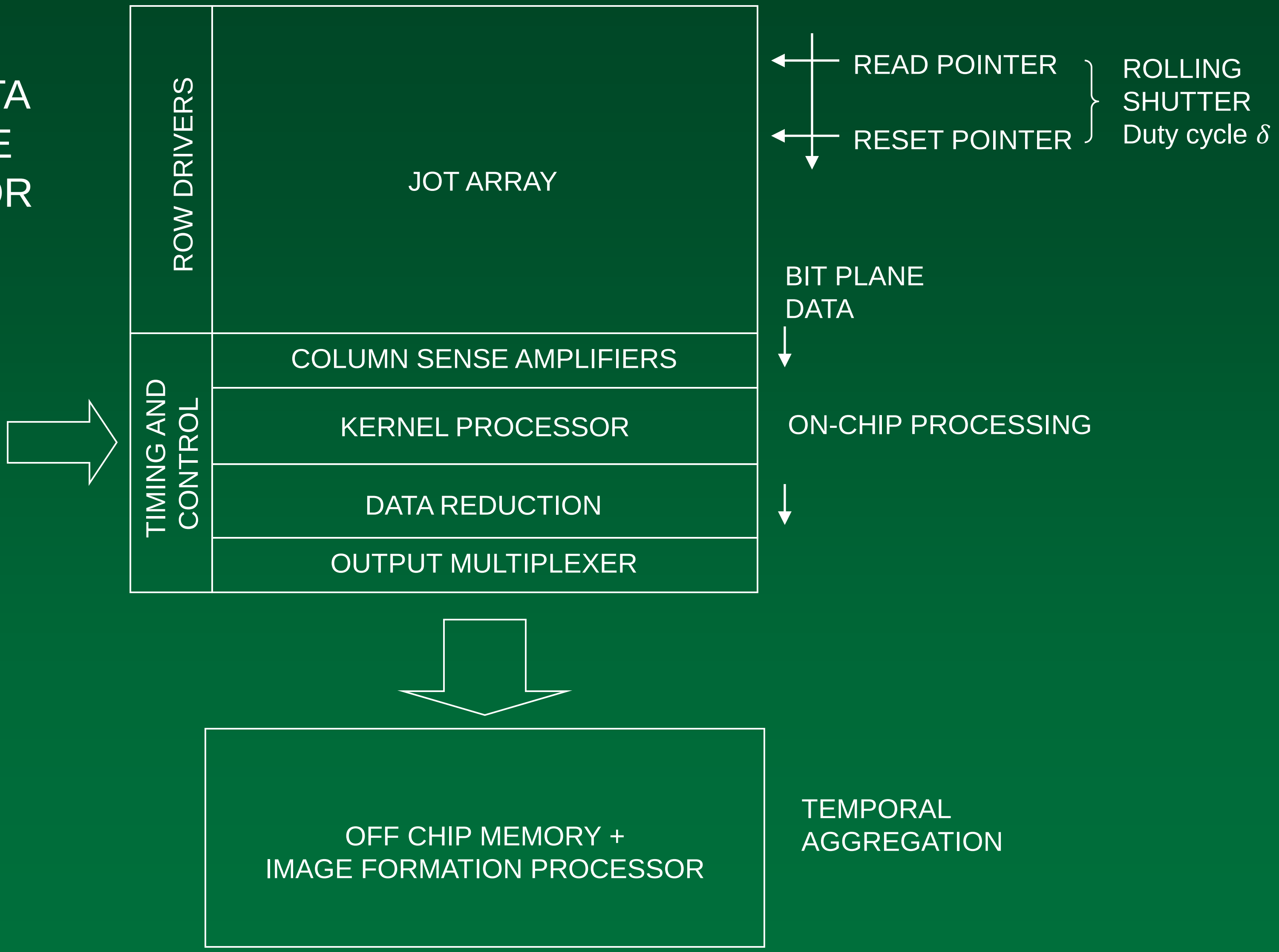
Possible Planar Architecture

QUANTA
IMAGE
SENSOR
(QIS)



ROW DRIVERS

JOT ARRAY

READ POINTER

RESET POINTER

ROLLING
SHUTTER
Duty cycle δ

BIT PLANE
DATA

TIMING AND
CONTROL

COLUMN SENSE AMPLIFIERS

KERNEL PROCESSOR

DATA REDUCTION

OUTPUT MULTIPLEXER

ON-CHIP
PROCESSOR
PROGRAM

ON-CHIP PROCESSING

OFF CHIP MEMORY +
IMAGE FORMATION PROCESSOR

TEMPORAL
AGGREGATION

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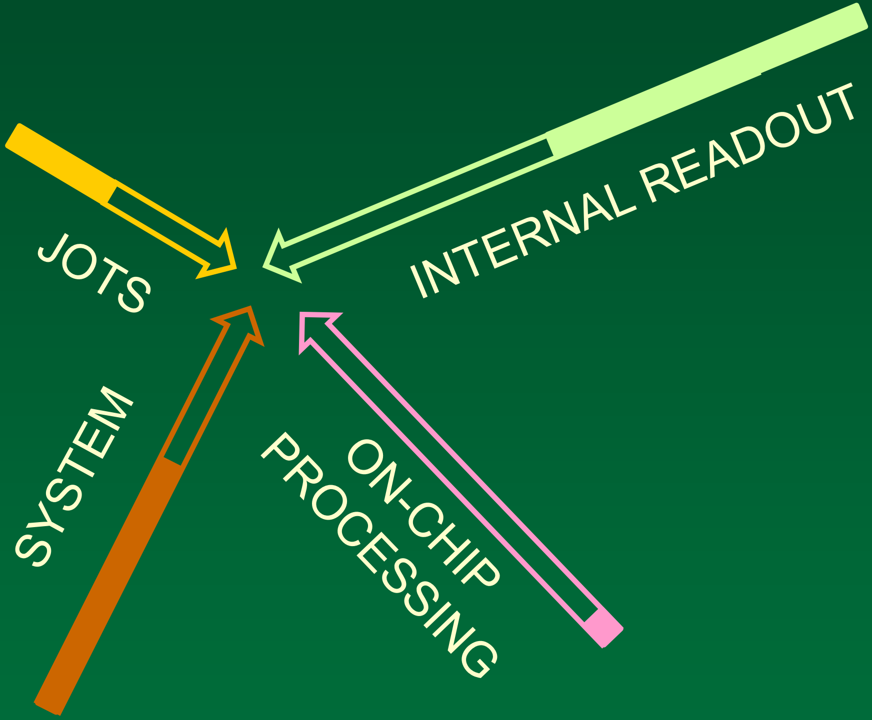
QIS implementation requires Devices, Circuits, and System

Strawman numbers

- <500 nm jot pitch
- Gigajot QIS (10^9 jots)
- 1000 fps
- 1 Tb/s data rate
- 1 Watt or less (<1pJ/b)


JOTS

INTERNAL READOUT

SYSTEM

ON-CHIP PROCESSING

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Features and Applications

- No read noise, high resolution visible photon counting
- Flexible post-capture trade between resolution and sensitivity
- Time-delay and integration in any track direction

- Low light level imaging
- Life science imaging
- Space imaging systems
- Photography
- Motion pictures
- Security
- Defense

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QIS Imaging Properties

E.R. Fossum, *Modeling the performance of single-bit and multi-bit quanta image sensors*, IEEE J. Electron Devices Society, vol.1(9) pp. 166-174 September 2013

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Flux Capacity

- What is the maximum photon flux that the QIS can handle (more or less)?
- At the flux capacity ϕ_{w1}, each jot, on the average, has received one photoelectron
- Let j = jot density, f_r = field readout rate, δ = shutter duty cycle, and $\bar{\gamma}$ = avg. QE

$$\phi_{w1} = jf_r/\delta\bar{\gamma}$$

- This drives <u>high jot density</u> and <u>fast readout</u>.
- Equivalency
  - 1.5 um pixel, 5000e- FWC, 1/15th sec = 33k e-/s/um^2
  - 0.2 um jot, 1 e- , 1000fps = 25k e-/s/um^2

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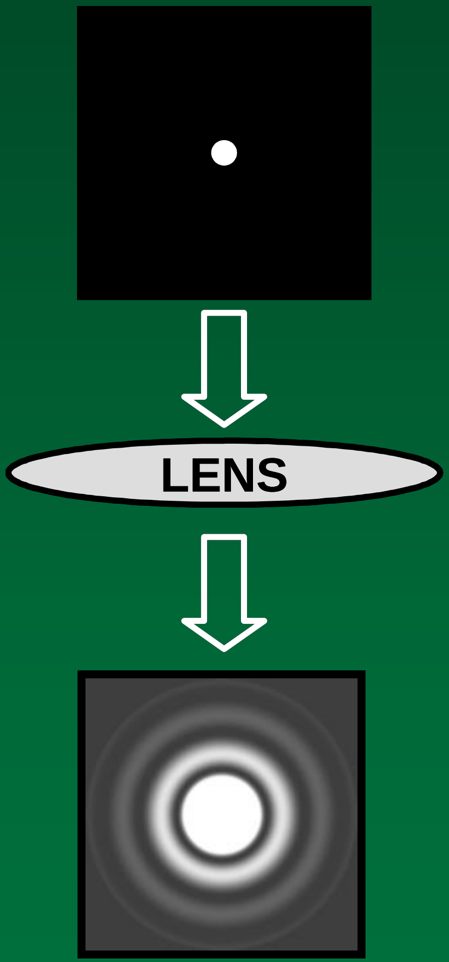
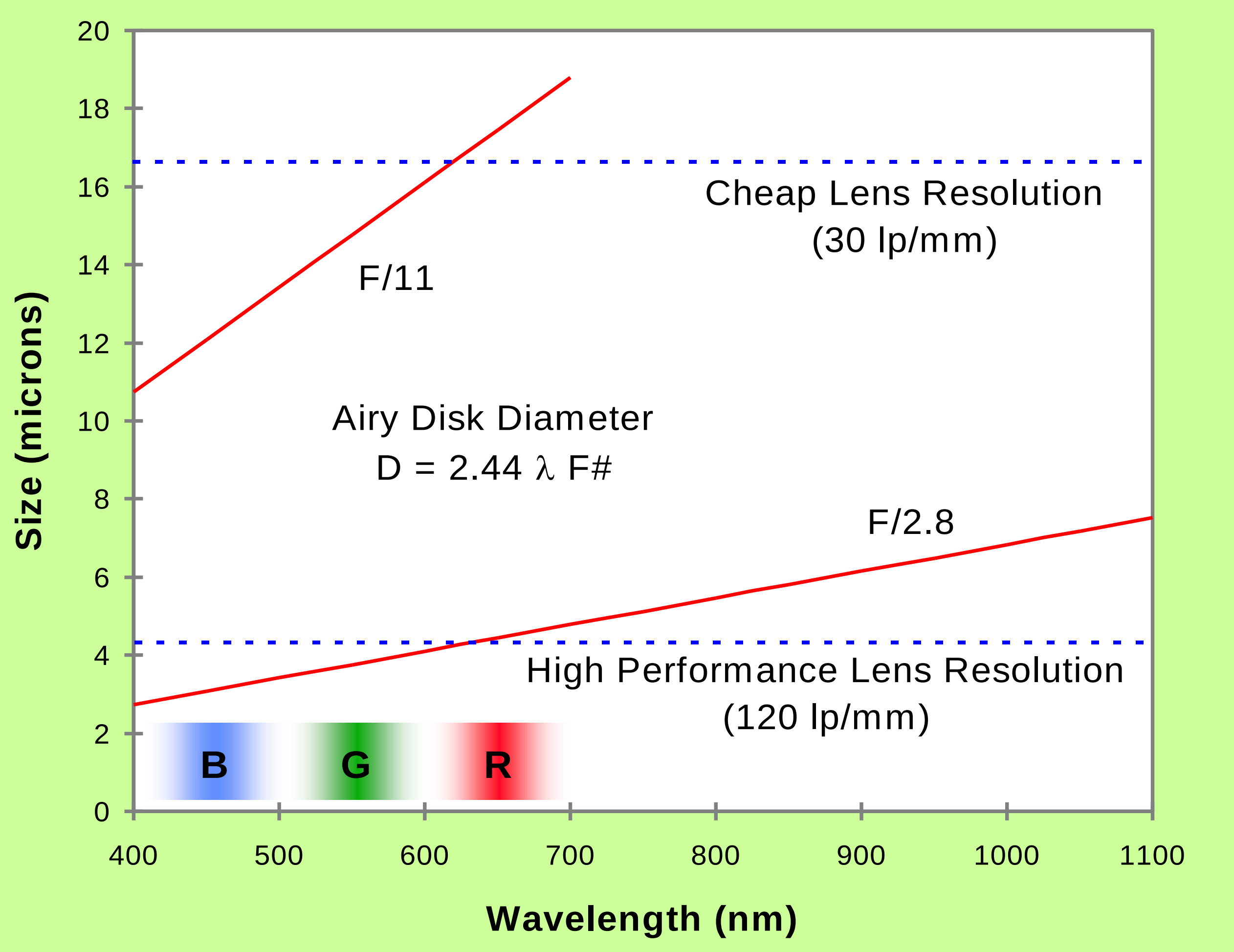
Diffraction Limit





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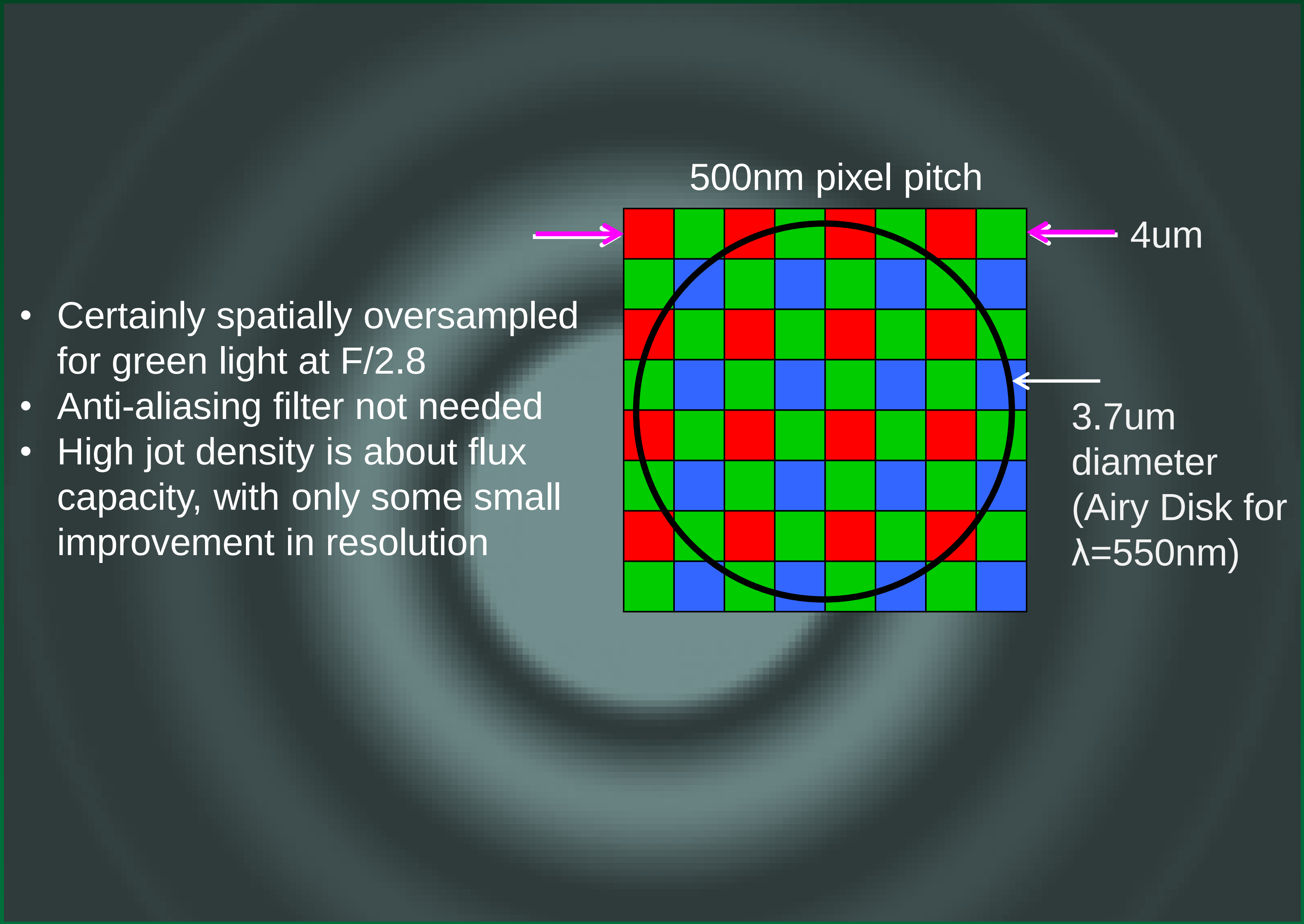
Sub-Diffraction Limit Pixels



- Certainly spatially oversampled for green light at F/2.8
- Anti-aliasing filter not needed
- High jot density is about flux capacity, with only some small improvement in resolution

500nm pixel pitch

4um

3.7um
diameter
(Airy Disk for
λ=550nm)

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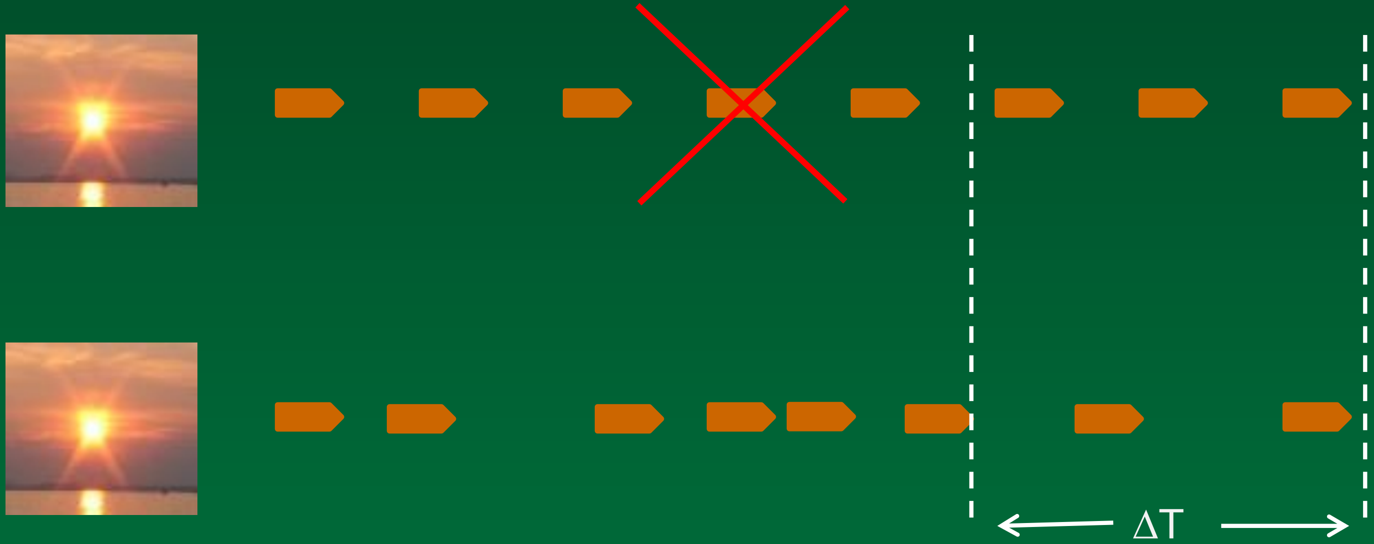
Photon Shot Noise

- Photon emission is a Poisson process. Stream of photons is NOT regularly spaced.



- Photon flux Φ characterized by Poisson statistics
- Variance $< (\Phi - <\Phi>)^2 > \sim \Phi$
- Noise $\sim \sqrt{\Phi}$ & SNR $\sim \sqrt{\Phi}$

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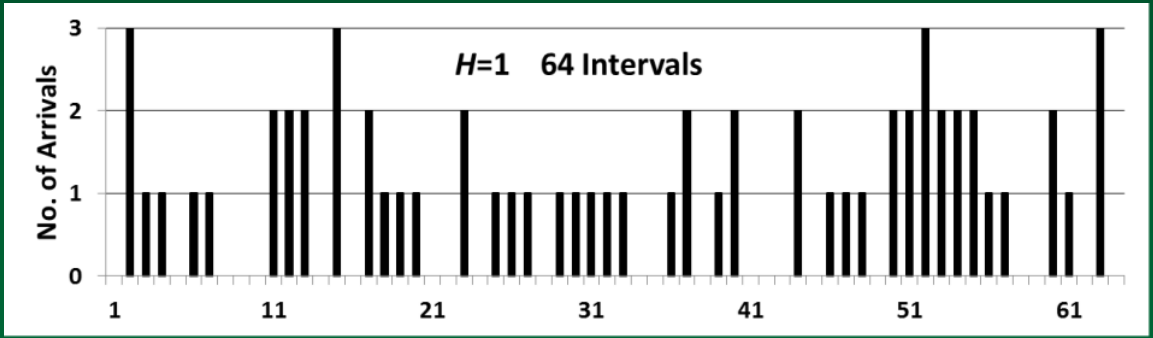
Photon and photoelectron arrival rate described by Poisson process

Define *quanta exposure* $H = \phi\,\tau$ $H = 1$ means expect 1 arrival on average.

Monte Carlo

Probability of k arrivals

$$P[k] = \frac{e^{-H}\,H^{k}}{k!}$$



For jot, only two states of interest

□ $P[0] = e^{-H}$

▨ $P[k>0] = 1 - P[0] = 1 - e^{-H}$

For ensemble of *M* jots, the expected number of 1's : $M_1 = M \cdot P[k>0]$

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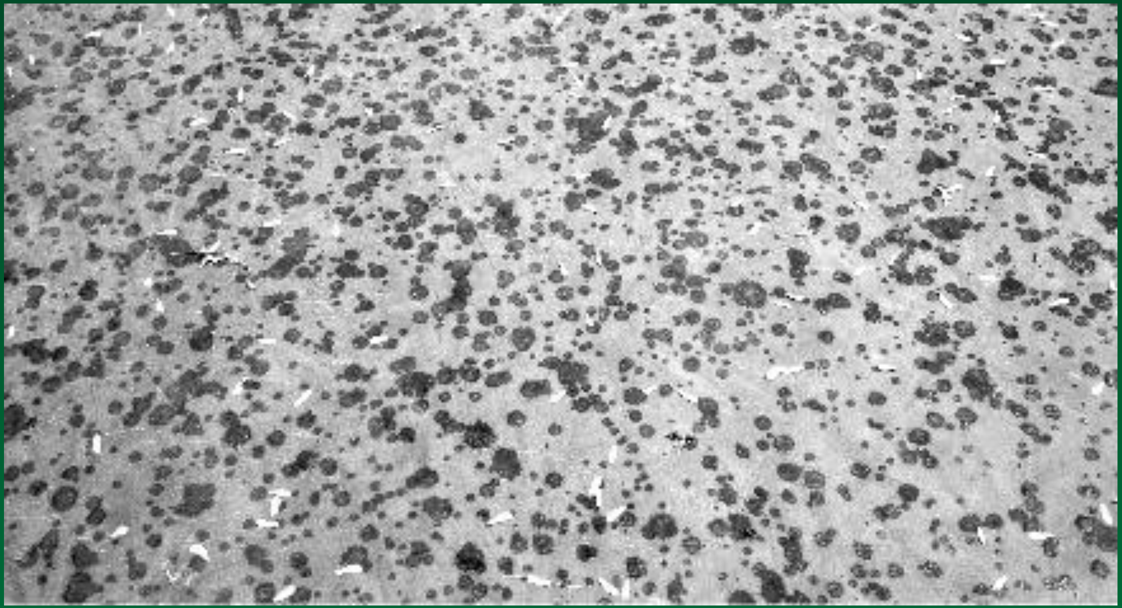
Raindrops on Ground



H~ 0.3 ?

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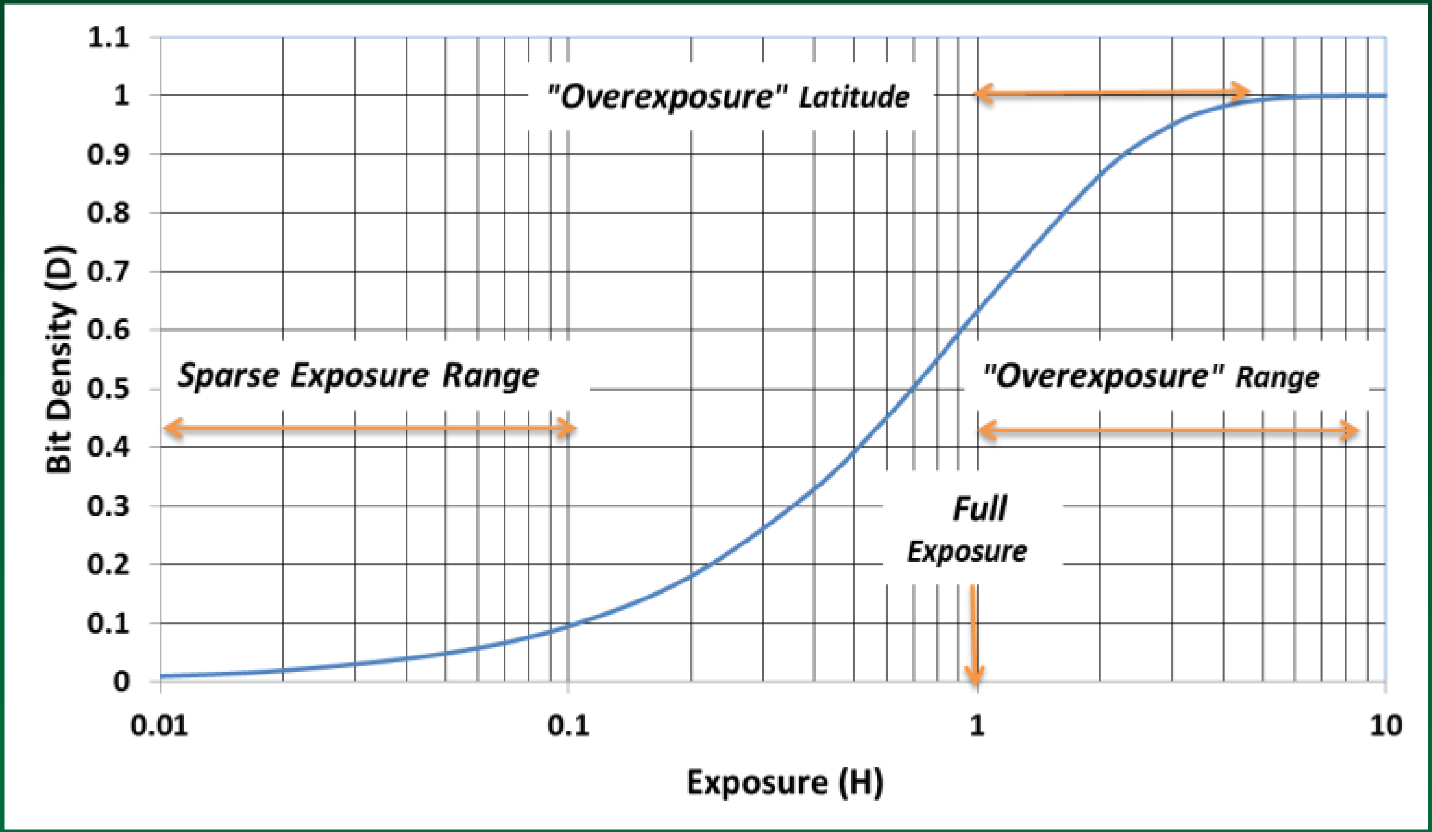
Bit Density

$$Bit\ Density\ D \triangleq \frac{M_1}{M} = 1 - e^{-H}$$



$$\underbrace{\hspace{4cm}}_{D \cong H \quad (\text{linear})}$$

Can determine H from measured D

$$\mathrm{H} = \ln\left[\frac{1}{1-D}\right]$$

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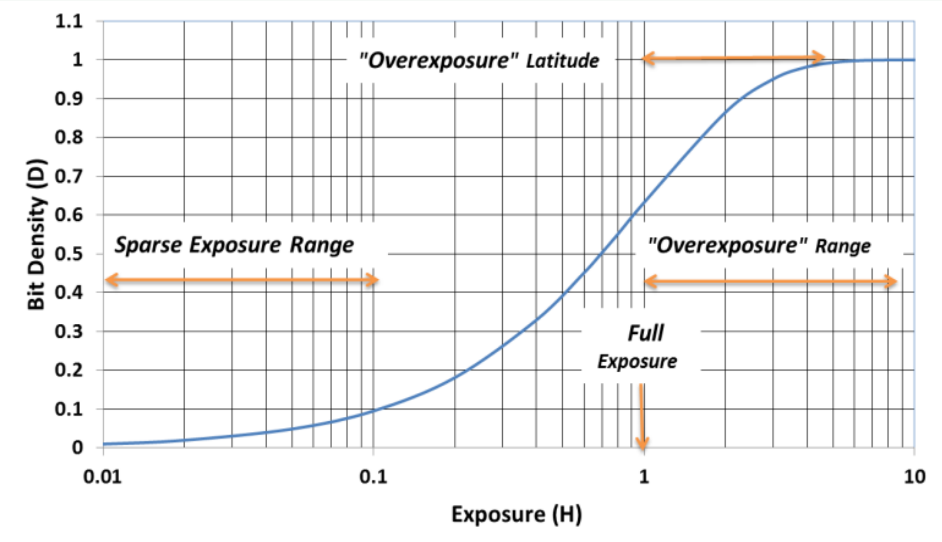
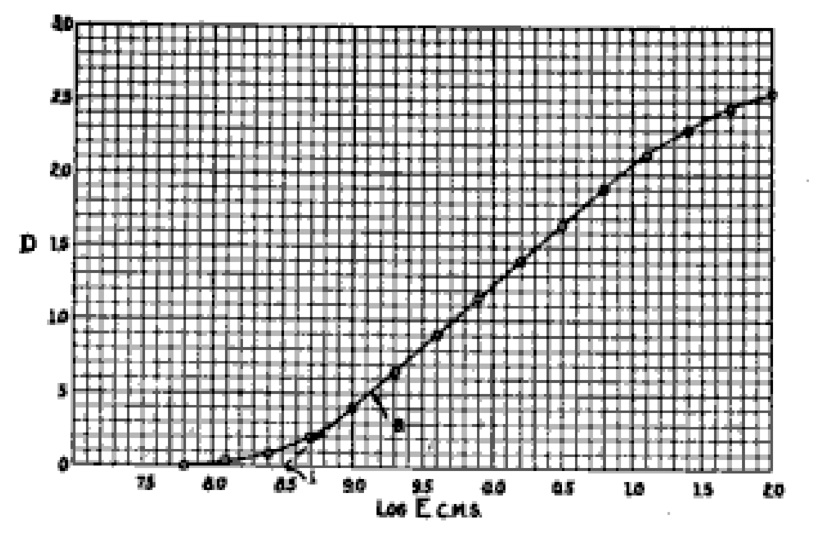
Film-like Exposure Characteristic

QIS D – log H

Film D – log H



Bit Density vs. Exposure



Film Density vs. Exposure
1890 Hurter and Driffield

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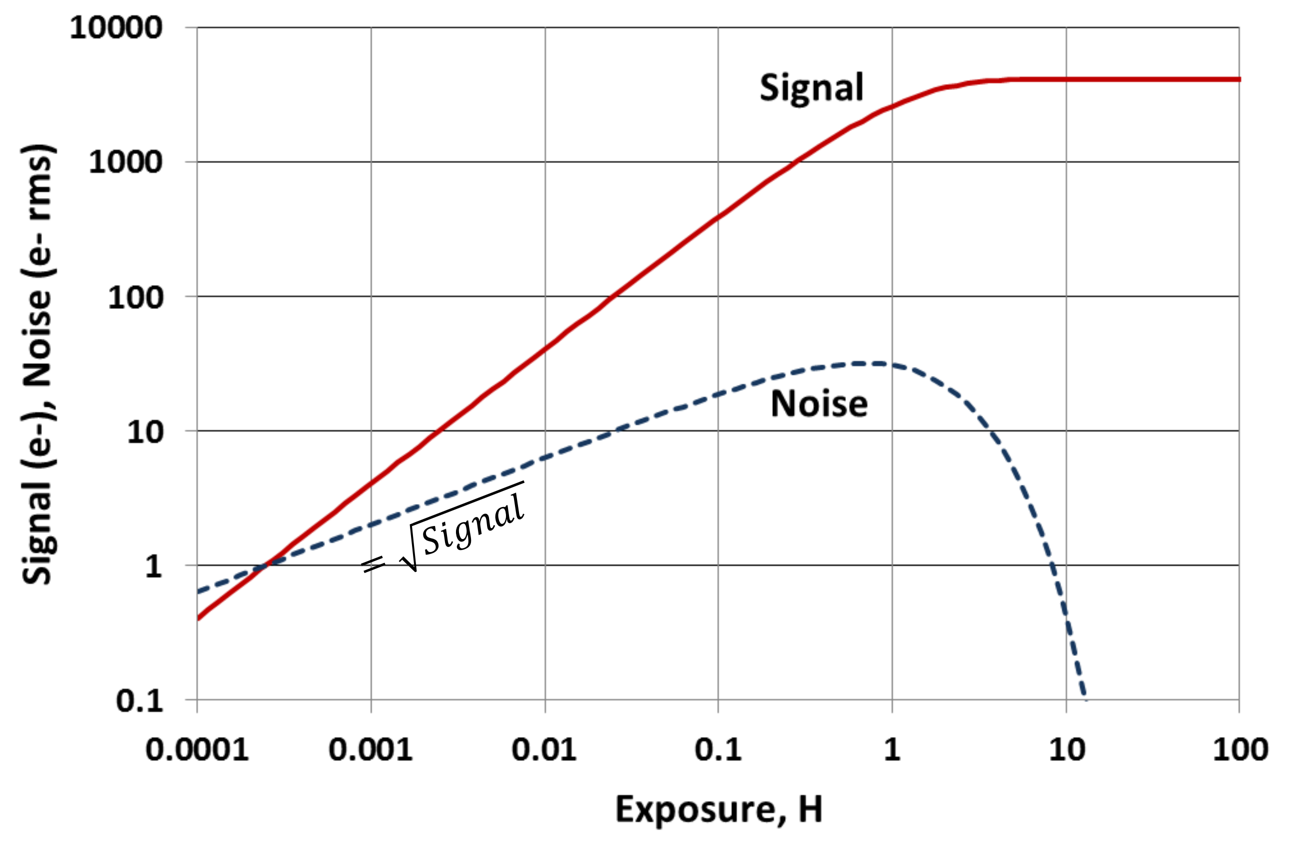
"Shot" Noise

Variance of a binomial distribution

$$\sigma_1{}^2 = M \cdot P[0] \cdot P[k > 0]$$



M=4096

SNR → ∞ ?

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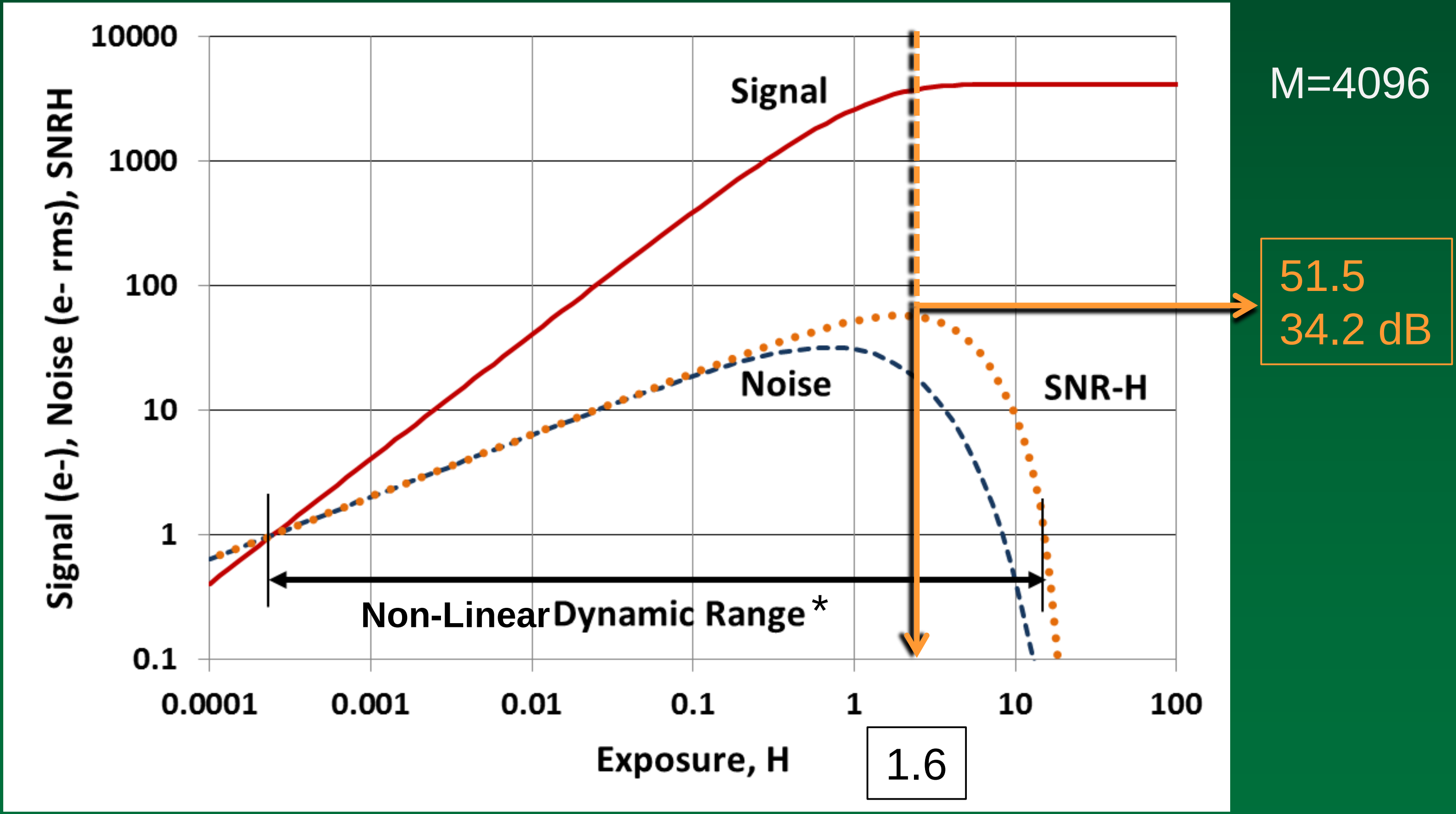
Exposure-Referred Noise

$$\sigma_H = \sigma_1 \frac{dH}{dM_1} \qquad SNR_H = \frac{H}{\sigma_H} = \sqrt{M}\frac{H}{\sqrt{e^H - 1}}$$



M=4096

*a new definition

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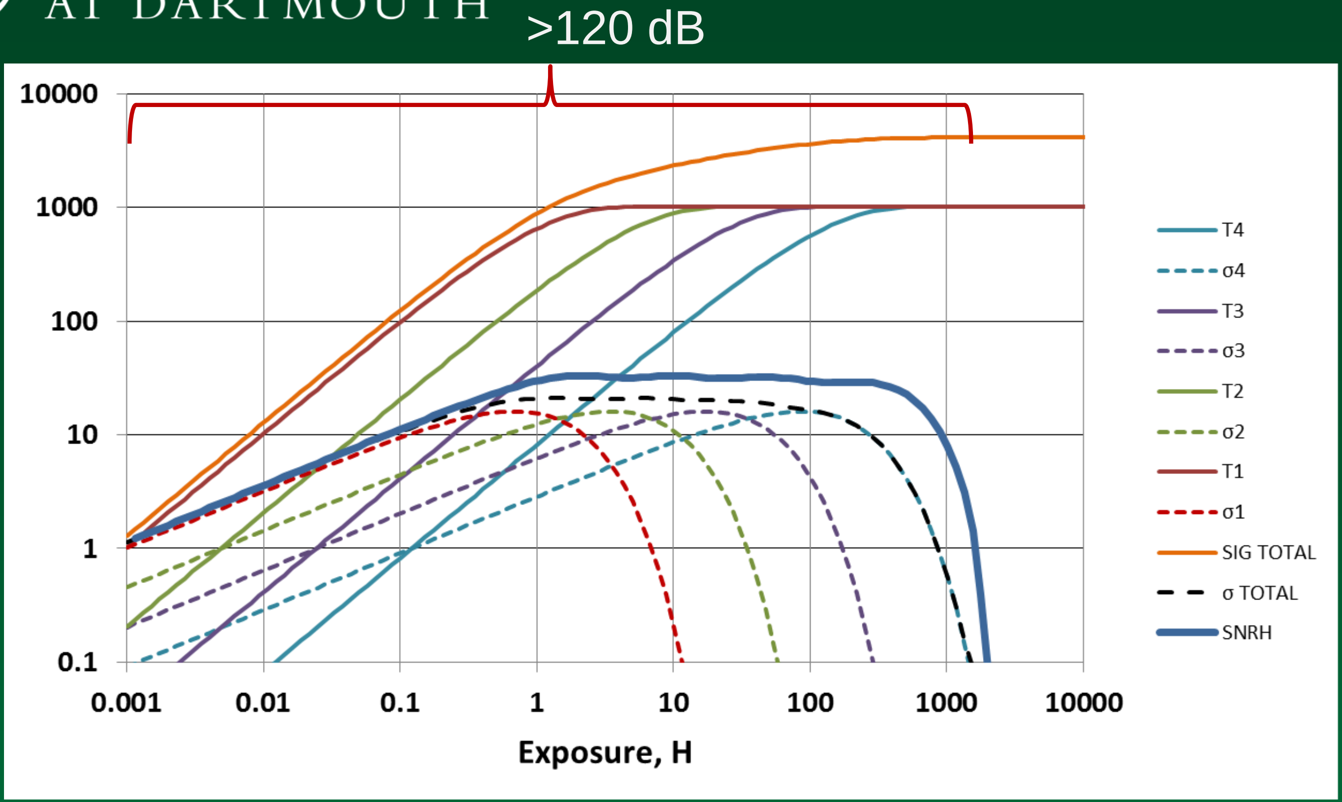
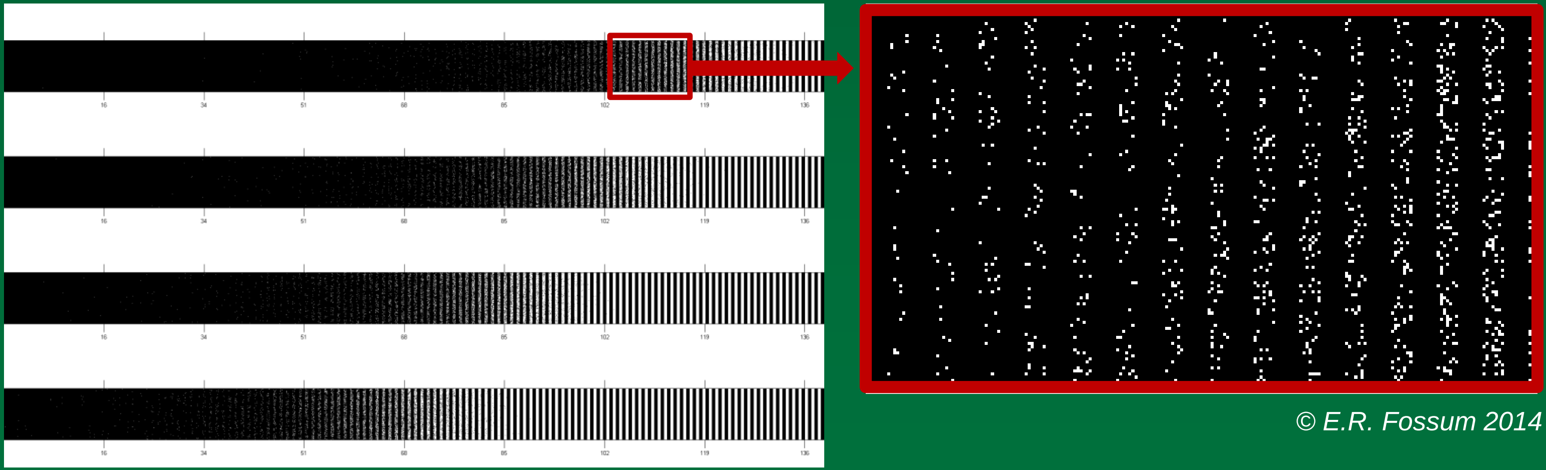
Increased Dynamic Range



Sum of 16 fields
4@ δ =1.0
4@ δ =0.2
4@ δ =0.04
4@ δ =0.008



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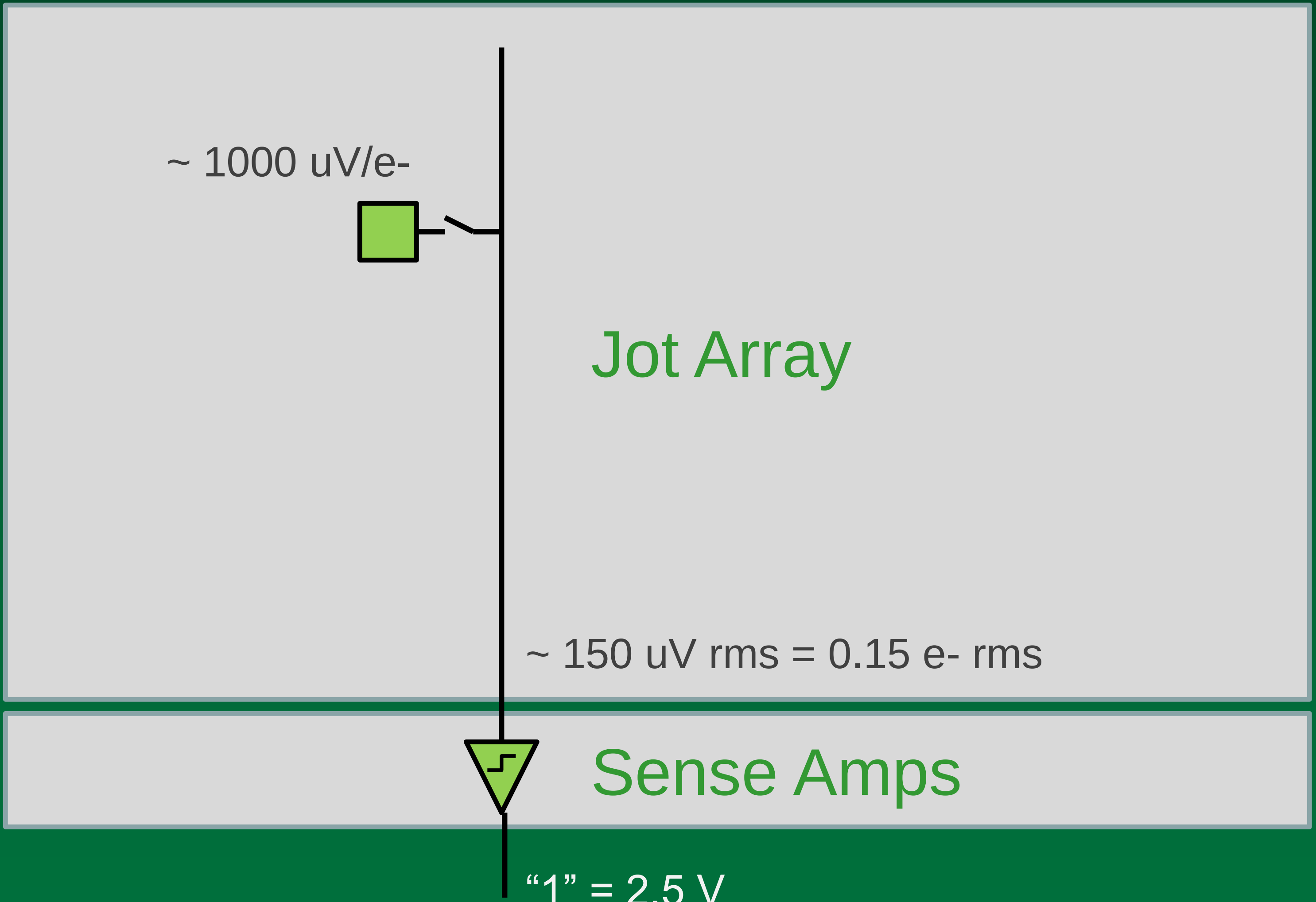
Readout Assumption for Read Noise



~ 1000 uV/e-

Jot Array

~ 150 uV rms = 0.15 e- rms

Sense Amps

“1” = 2.5 V

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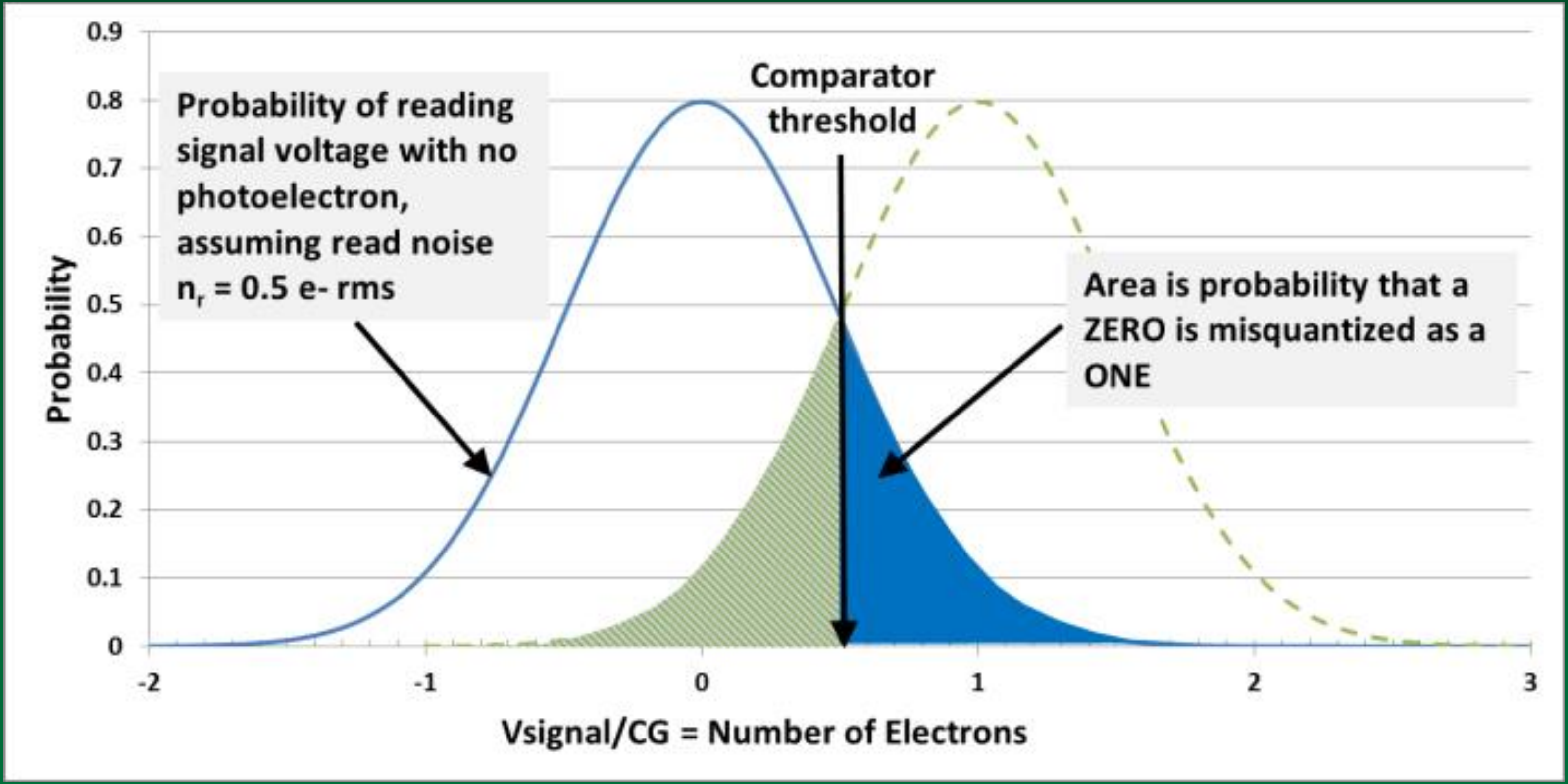
Read Noise and Bit Error Rate (BER)



Probability of reading signal voltage with no photoelectron, assuming read noise n_r = 0.5 e- rms

Comparator threshold

Area is probability that a ZERO is misquantized as a ONE

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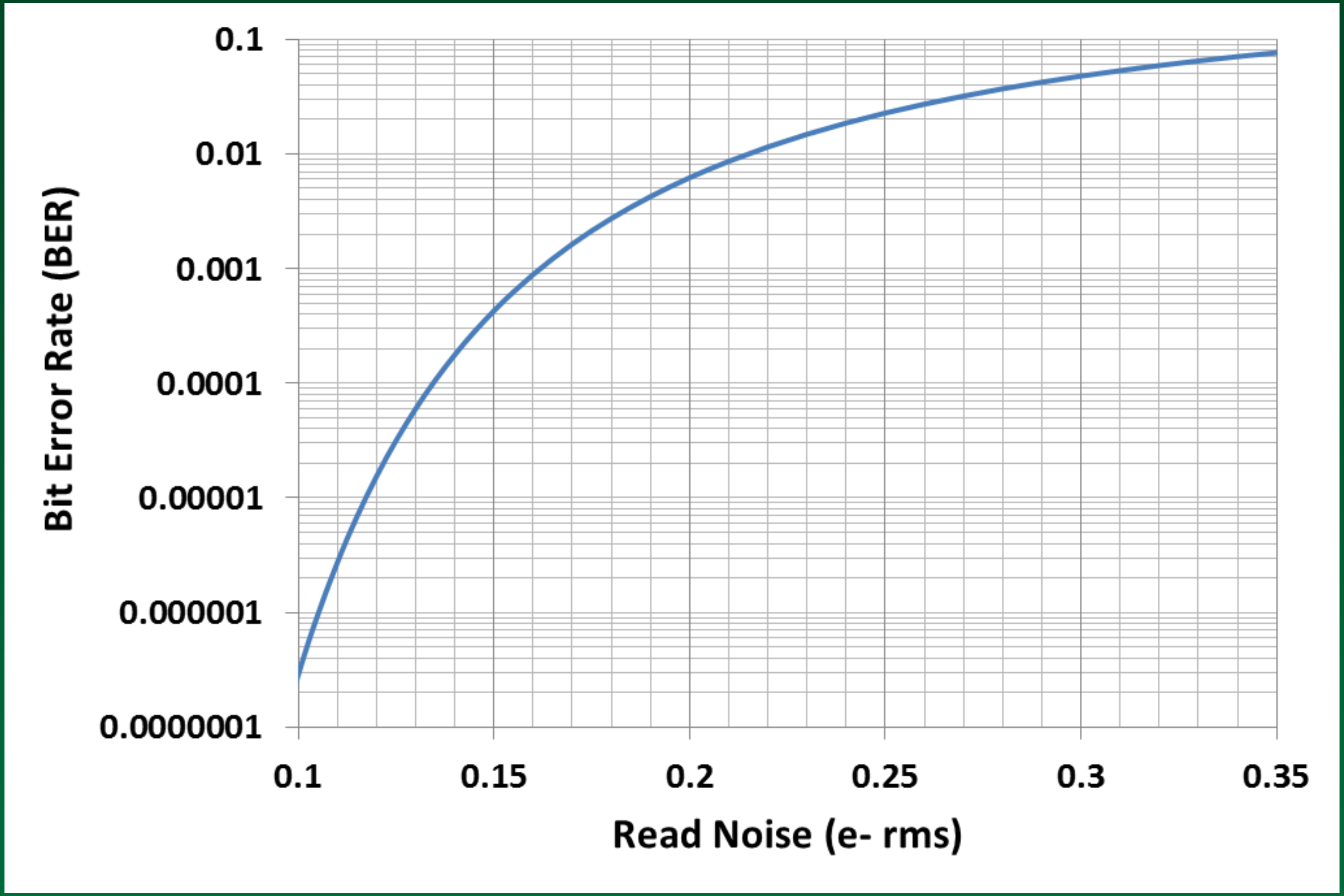
BER vs. Read Noise



$$BER = \frac{1}{2} erfc\left(\frac{1}{\sqrt{8 n_r}}\right)$$

What is an acceptable bit error rate?

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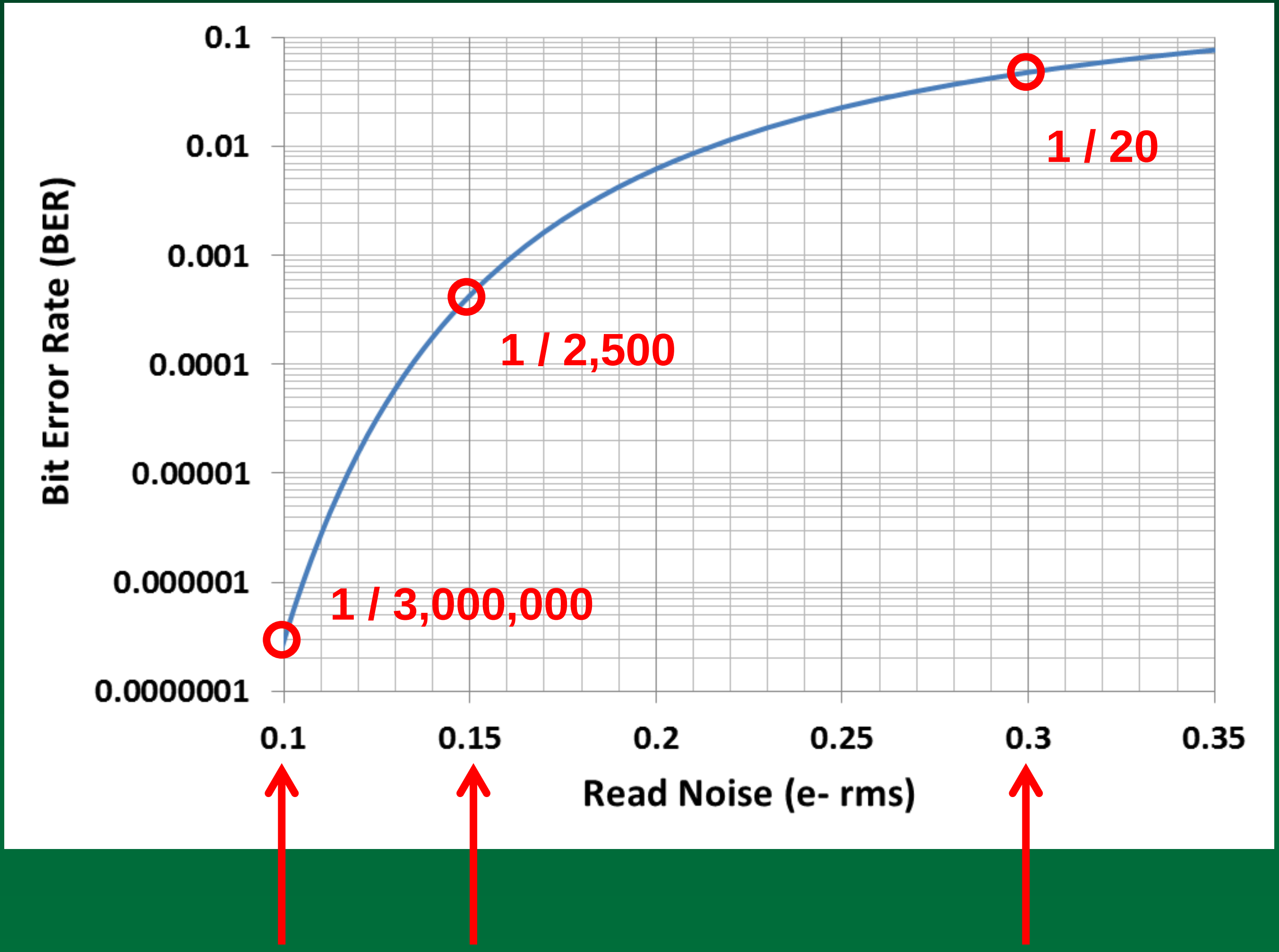
BER vs. Read Noise



Fossum 2011 WAG

Fossum 2013

Teranishi 2012

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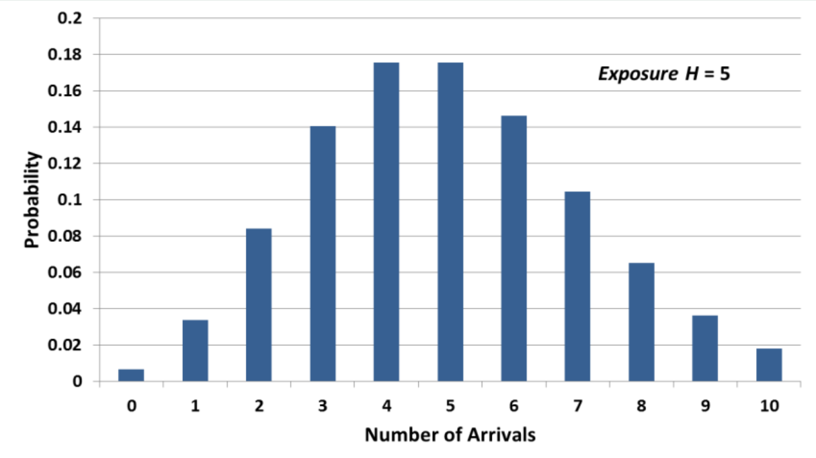
Shot Noise and Read Noise

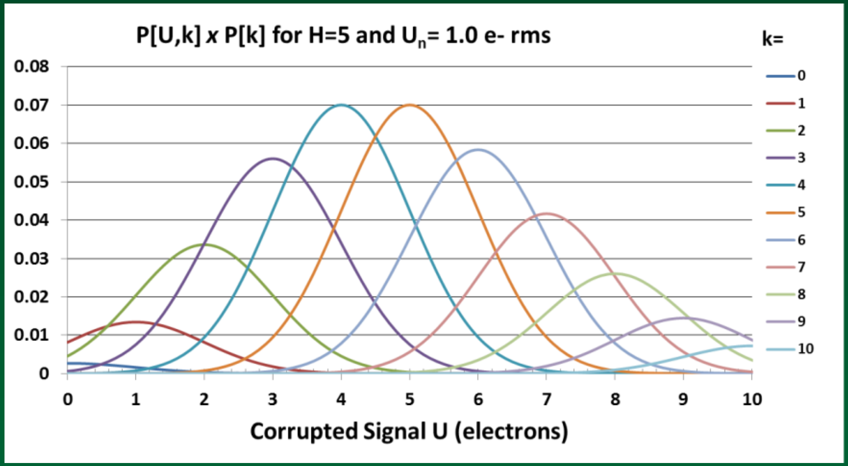
“Shot” Noise

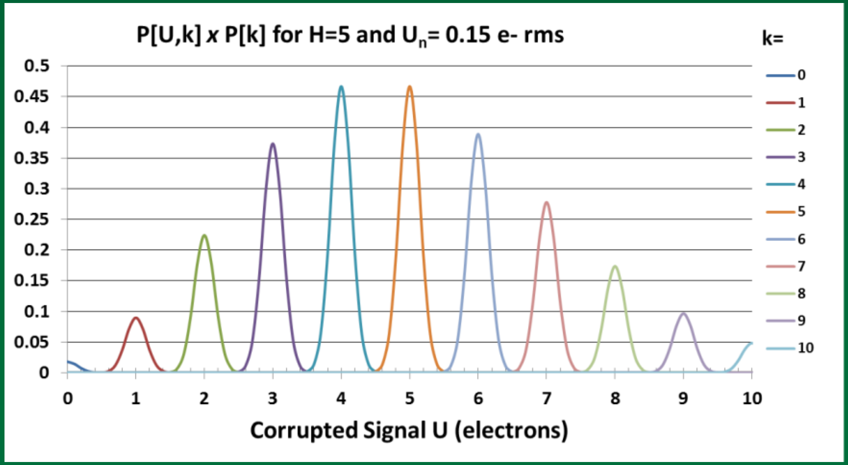
$$\sigma^2 = <k^2> - <k>^2$$

plus

Read Noise
(Gaussian model)







$$P[k] = \frac{e^{-H} H^k}{k!}$$

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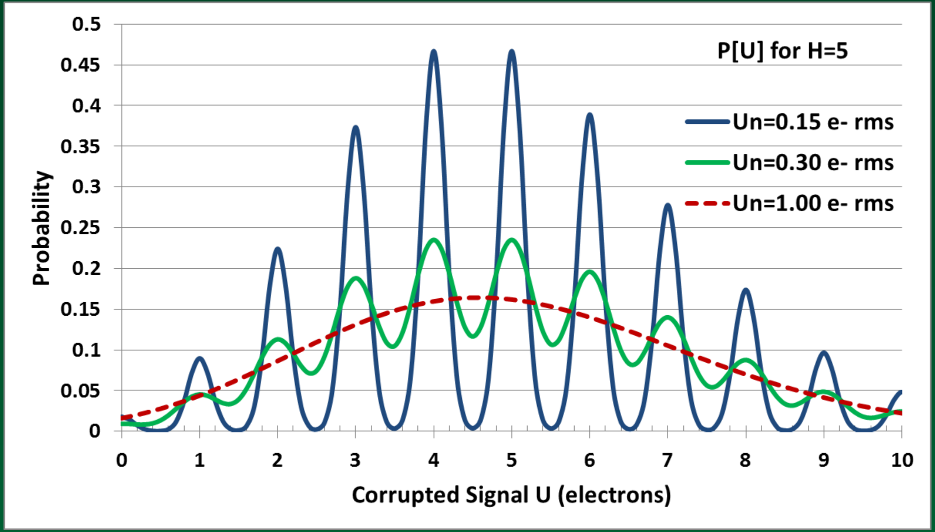
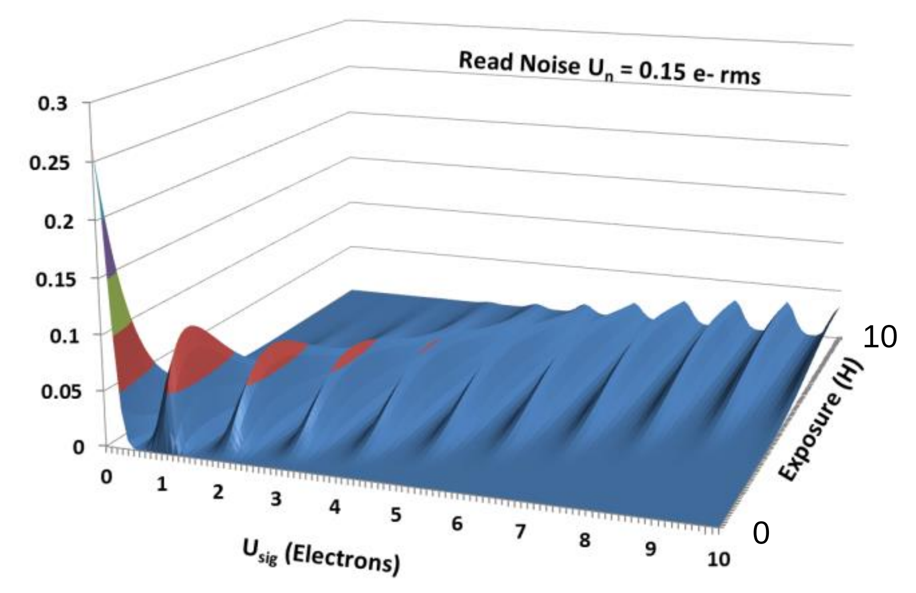
Effect of Read Noise on Photoelectron Counting for Multi-bit Pixel



Note “peak” for H=5 is not at 5 e-



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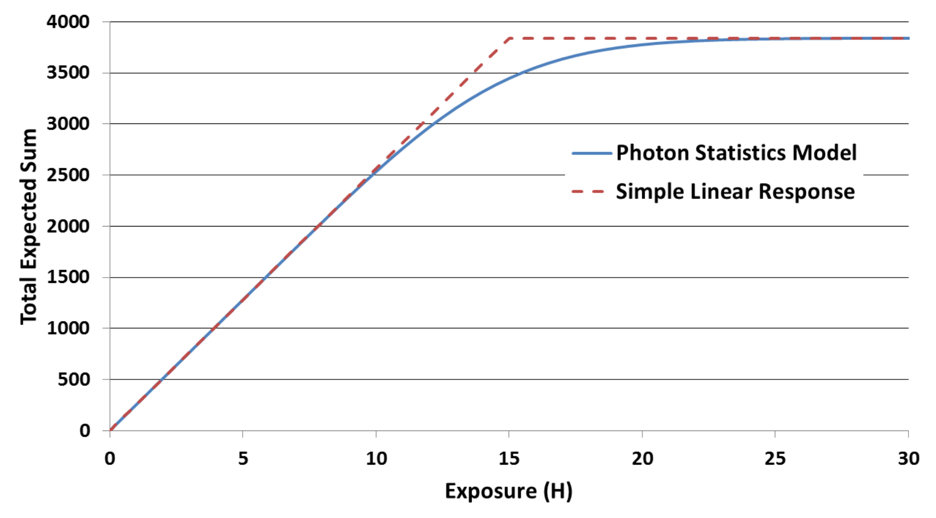
Multi-bit Pixels

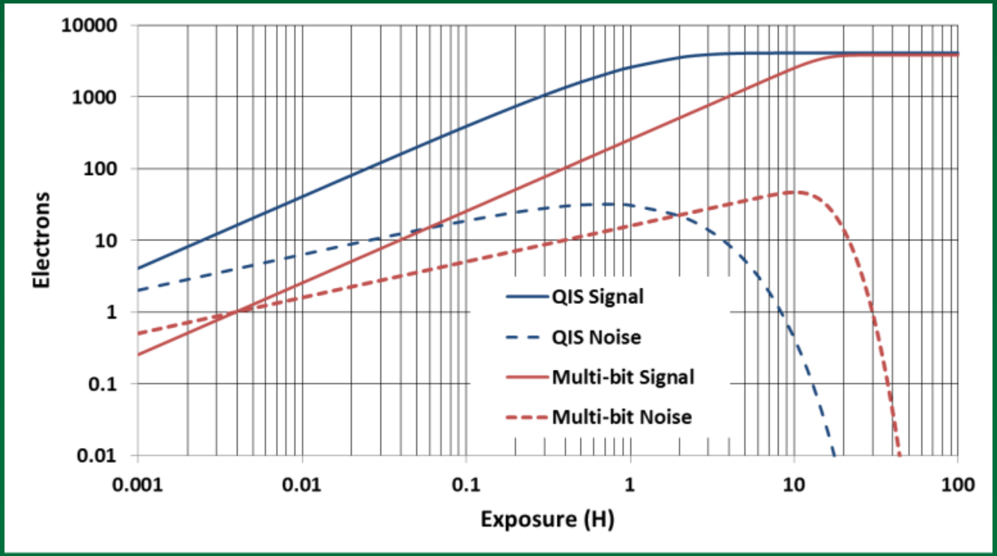
Counting low number of photoelectrons, e.g. 4b yields FW = 15 e-



Sum 4x4x16 = 256 pixels
Max = 15x256 = 3840

$$\phi_{wn} = j f_r (2^n - 1)/\delta\bar{\gamma}$$

1b v. 4b



QIS: M=4096
4b: M=273

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Jots

Jiaju Ma, Donald Hondongwa and E.R. Fossum

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Jot Device Considerations

General targets:

- 200 nm device in 22 nm process node (“10L”)
- High conversion gain > 1 mV/e- (per photoelectron)
- Small storage well capacity ~1-100 e-
- Complete reset for low noise
- Low active pixel transistor noise <150 uV rms
- Low dark current ~ 1 e-/s
- Not too difficult to fabricate in CIS line

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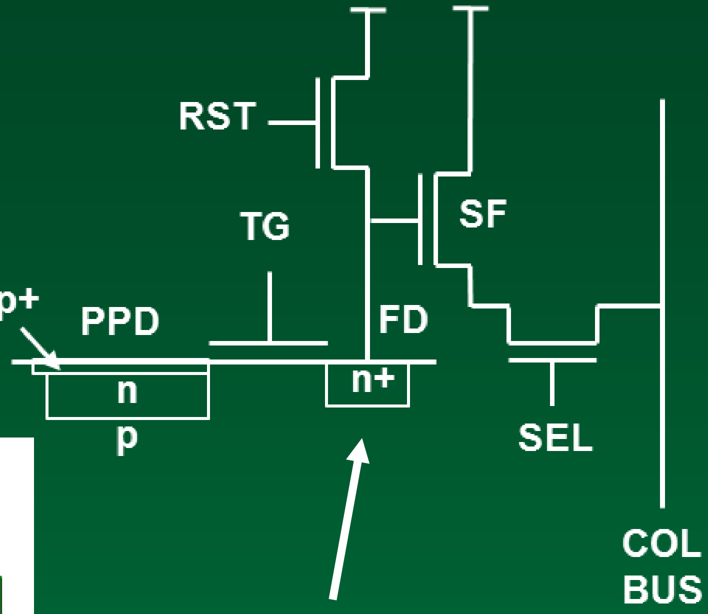
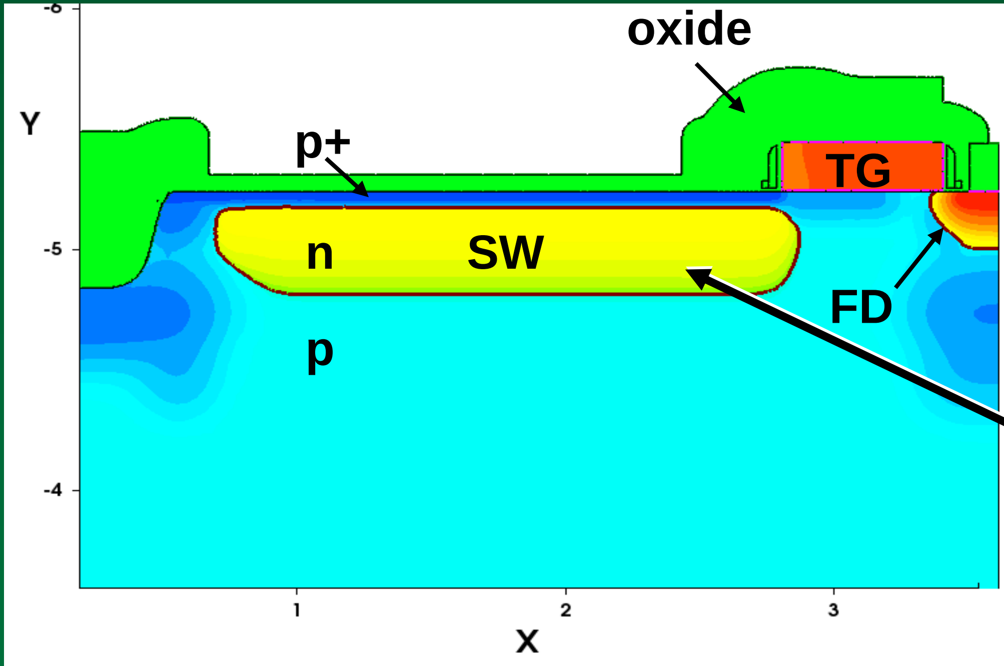
Pinned Photodiode Pixel



Typ. 50-100uV/e-



Typ. 3-5ke-/um^2

E.R. Fossum and D. Hondongwa, A review of the pinned photodiode for CCD and CMOS image sensors, IEEE J. Electron Devices Society, vol 2(3) pp. 33-43 May 2014.

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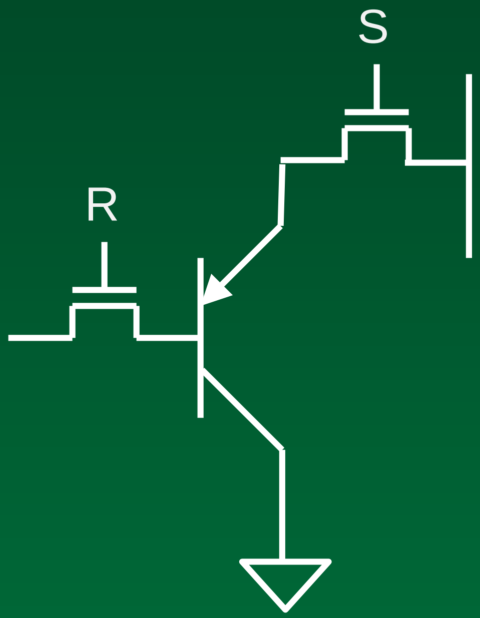
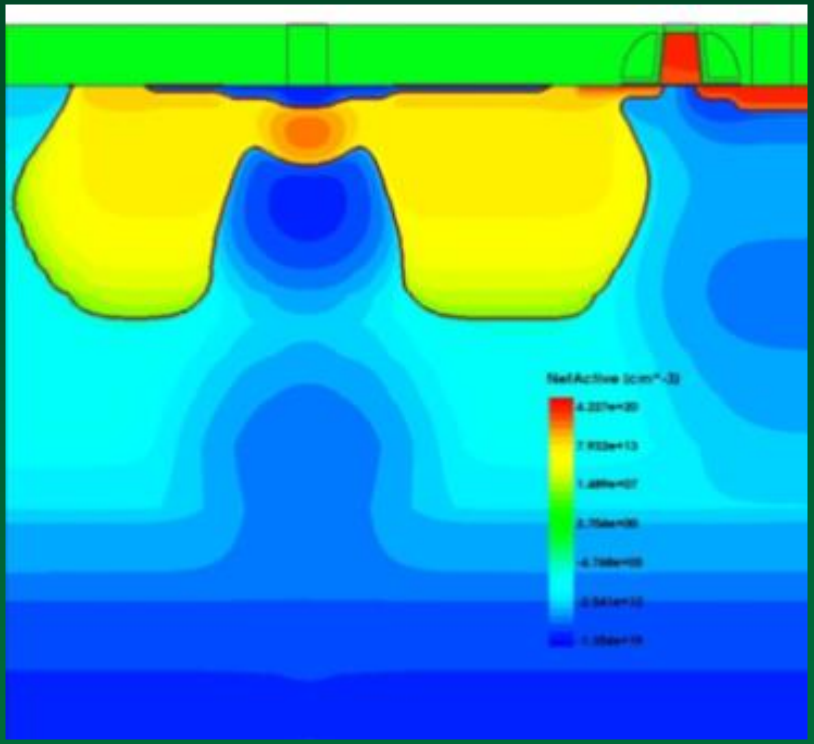
Bipolar Jot Concept





- CMOS APS but use pinning layer as emitter, storage well as base
- Complete reset of base using “TG”
- Emitter follower to reduce base-emitter cap

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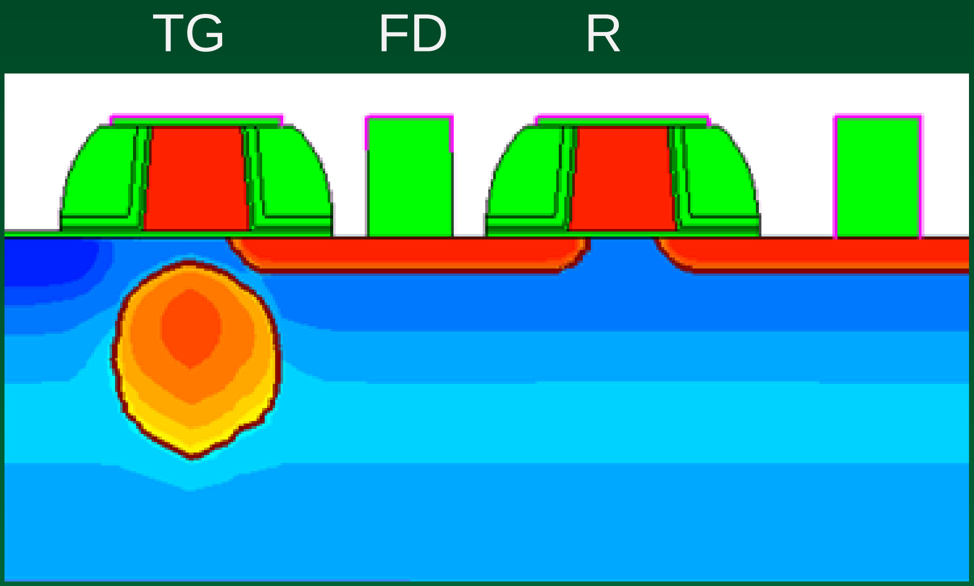
BSI CMOS APS Jot with Storage under Transfer Gate



Ma and Fossum 2013

- Low capacity storage gate makes barrier easier to overcome with low TG voltage
- Minimum FD size to increase conversion gain

Storage under transfer gate first proposed in
Back Illuminated Vertically Pinned Photodiode with in Depth Charge Storage, by J. Michelot, et al., 2011 IISW

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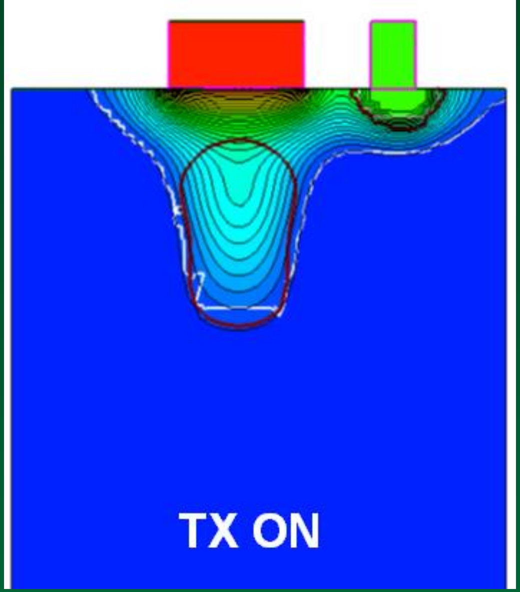
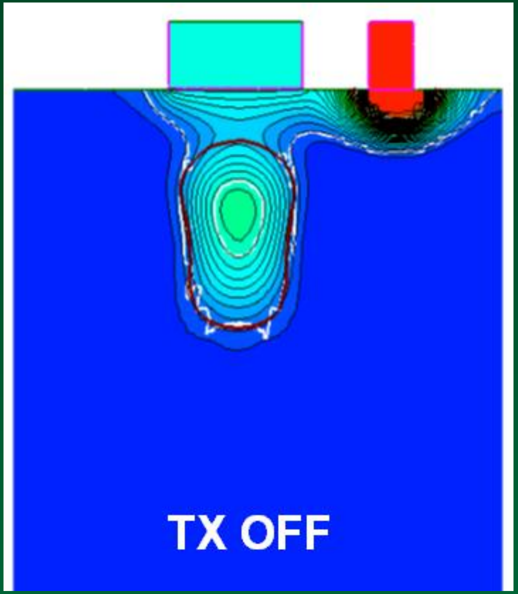
Pump-gate Jot Device with Distal FD to Increase Conversion Gain

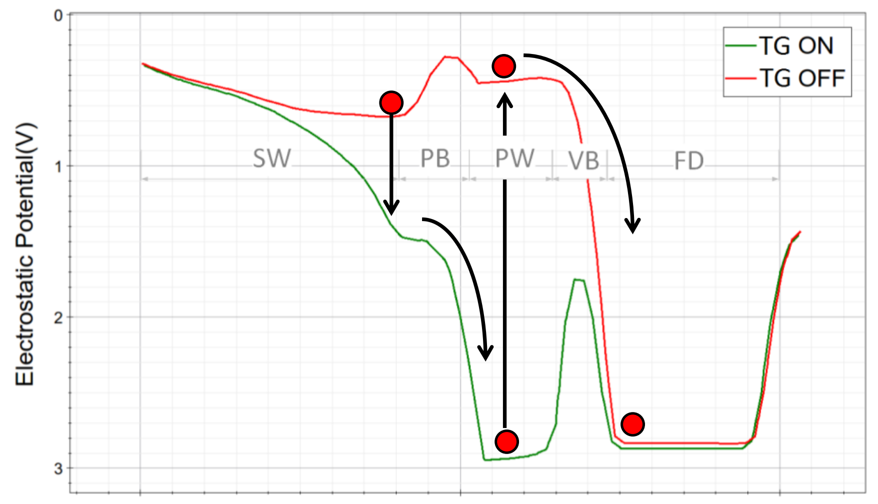


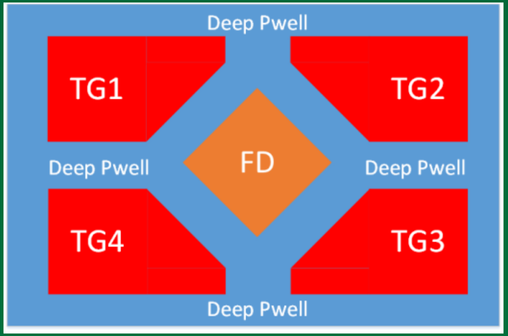


(Simulation)

- 65 nm node
- 1.4 um pitch
- 3.3 V operation
- 200 e- FW
- 480 uV/e-

Test array taped out Summer 2014 incl. shared readout





Ma and Fossum 2014 IEDM

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SEFET

Samsung

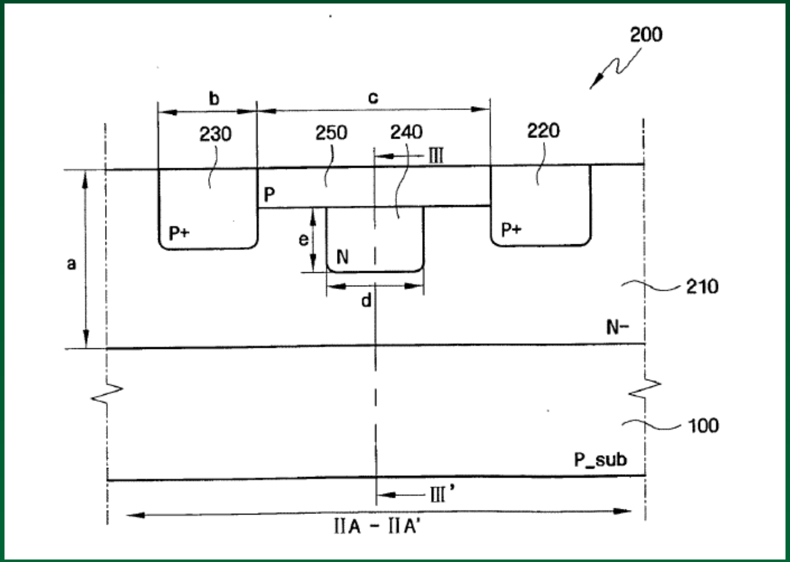
(19) **United States**

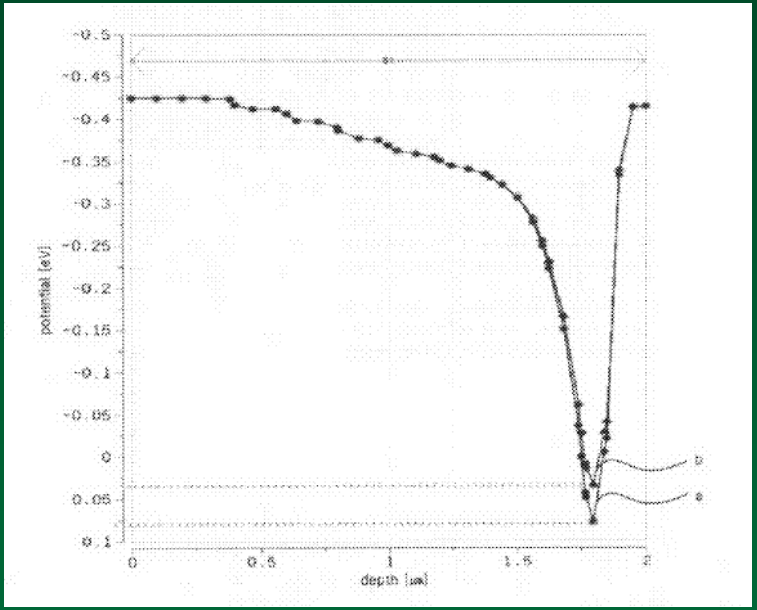
(12) **Patent Application Publication**

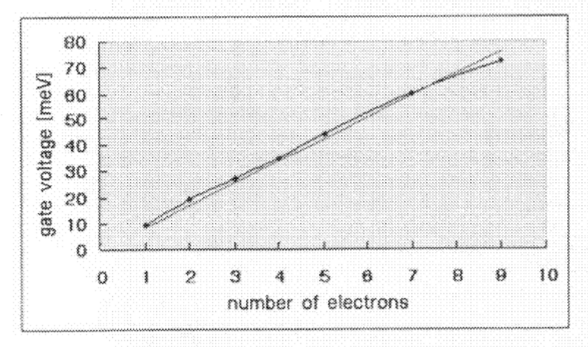
Fossum et al.

(10) **Pub. No.: US 2010/0320515 A1**

(43) **Pub. Date: Dec. 23, 2010**







Status:

- TCAD model only
- Shows about 5 mV/e- signal
- More work required

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SPAD Implementation of QIS
At Univ. Edinburgh

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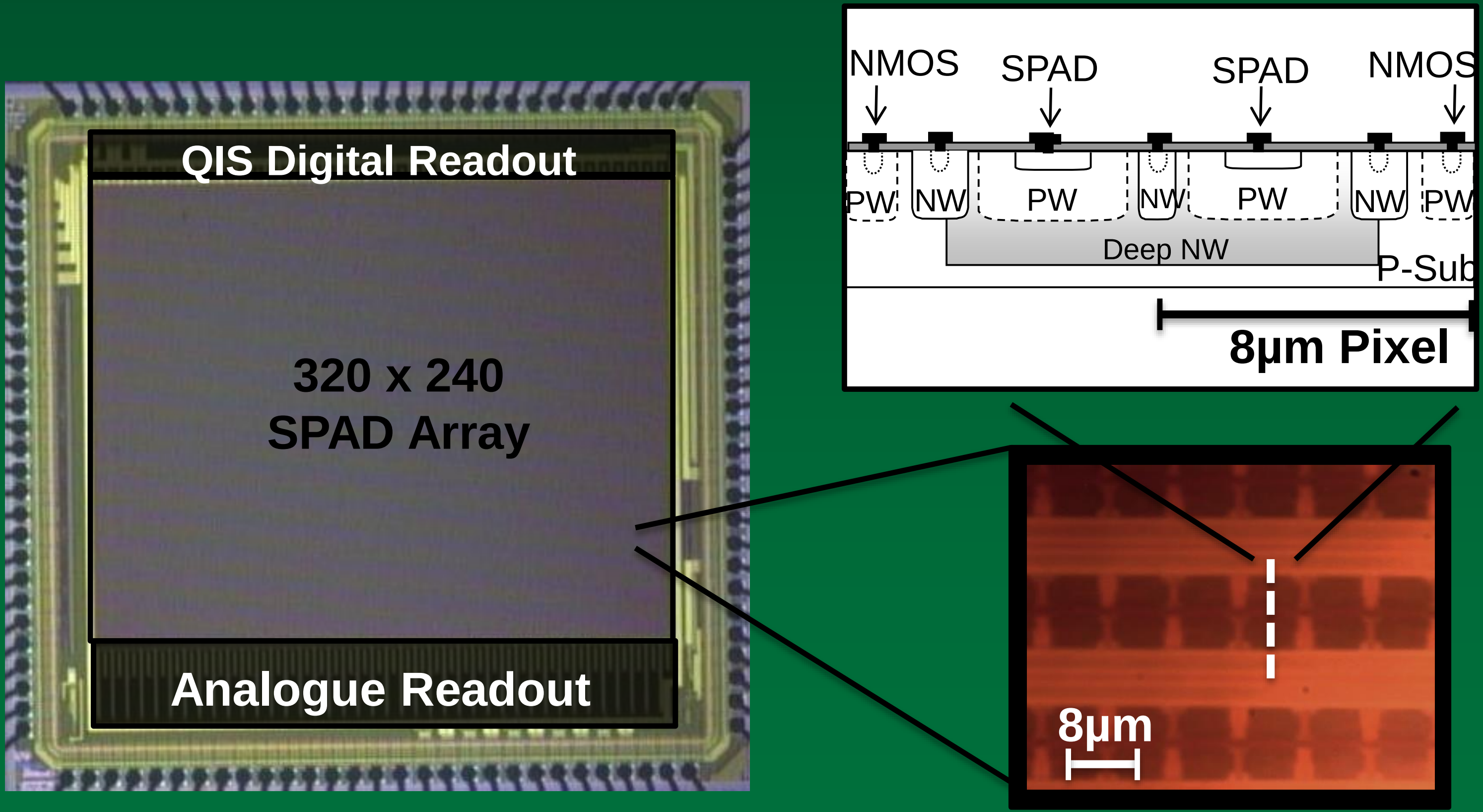
320x240 SPAD-based QIS

- Dutton et al. *IEEE VLSI Symposium* 2014
- University of Edinburgh & ST Microelectronics
- 8µm SPAD-based Pixel with 26.8% FF



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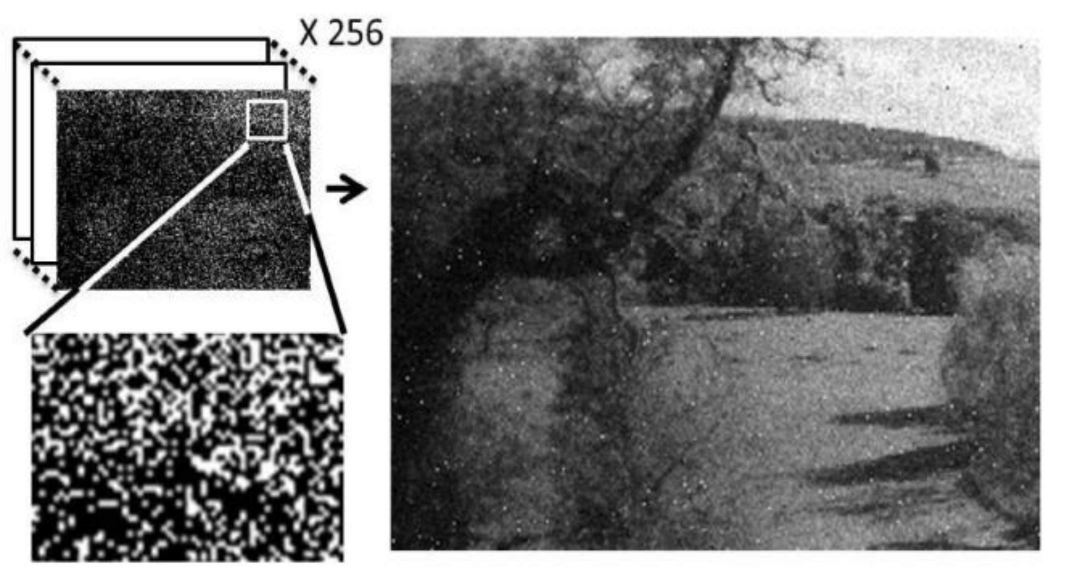
320x240 SPAD-based QIS

Dutton et al. *IEEE VLSI Symposium* 2014



5k FPS
Binary Frames

20 FPS 8b DR
(256 frames summed)

	SPAD-QIS	**Desired QIS**
Flux Capacity ϕ_{w1}	21 e-/s/um^2	20,000 e-/s/um^2
Energy/bit	166 pJ/b	<1 pJ/b

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THAYER SCHOOL OF
ENGINEERING
AT DARTMOUTH

Readout of Jot Signal to Digital Circuits

Saleh Masoodian, Arun Rao, Song Chen, Kofi Odame and E.R. Fossum

© E.R. Fossum 2014

Readout Signal Chain Strawman Design

General requirements:

- Need to scan 0.1-10 Gjots at 100-1000 fields per sec
- 8k – 80k jots per column → 0.8 – 80M jots/sec

Assumptions:

- 0.1 Gjot at 100 fps → 1Mjot/sec
- 1 mV/e- conversion gain
- 150 uV rms noise on column bus (0.15 e- rms)
- 0.18 um process
- Vdd = 1.8V

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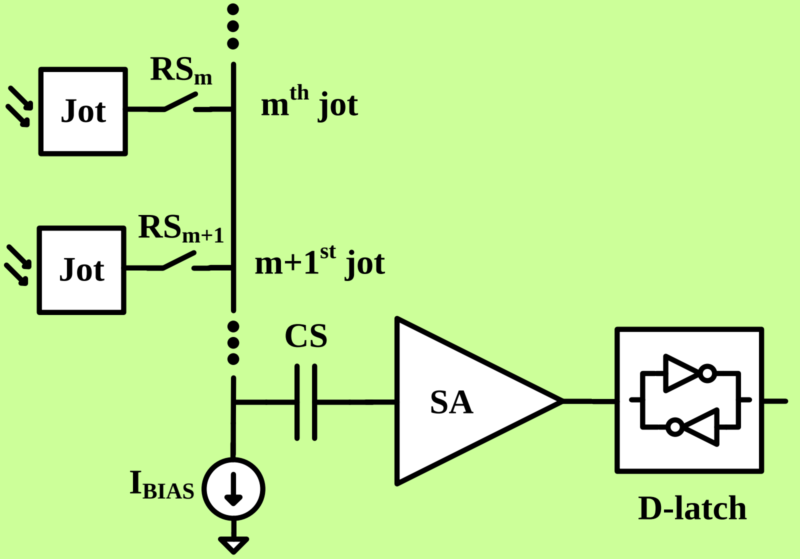
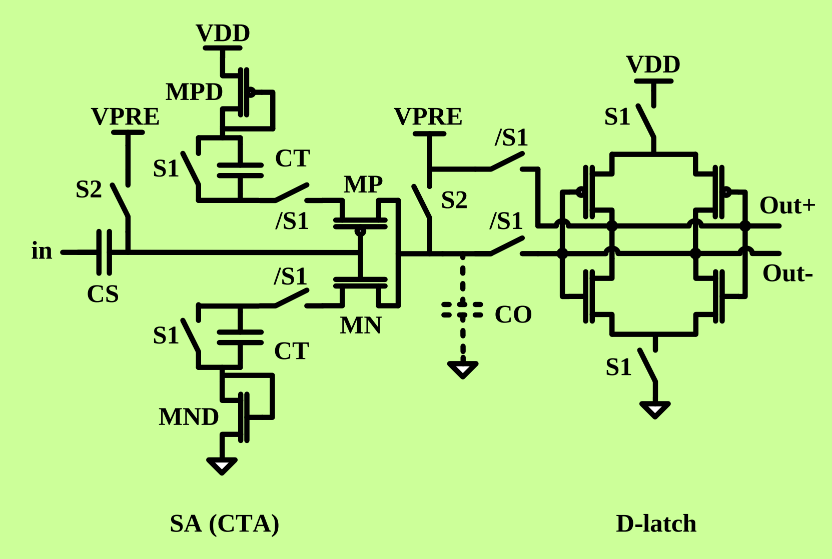
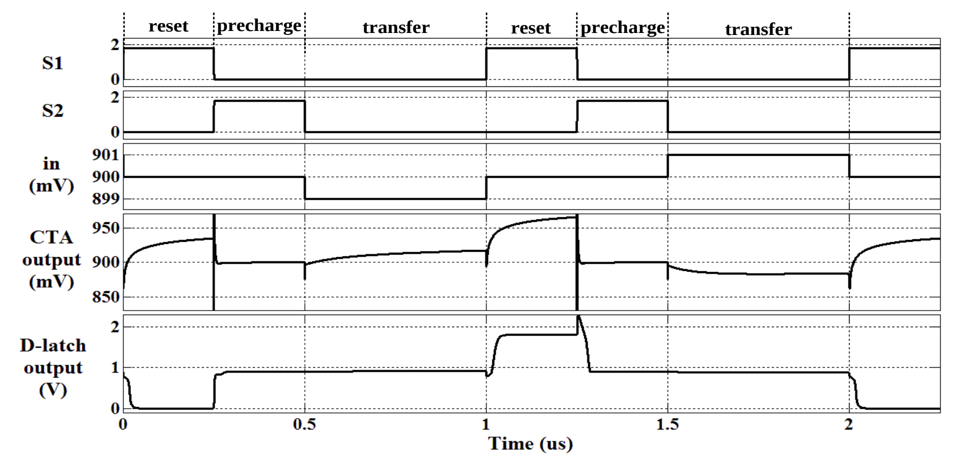
Low Power Sense Amp





- XFAB 0.18um
- Vdd 1.8V
- 1000”jot”/col
- Ibias ~ 1uA
- 1MSa/s
- Power 2uW
- Energy 2pJ/b



S. Masoodian, K. Odame, and E.R. Fossum, Low-power readout circuit for quanta image sensors, Electronics Letters, Vol. 50 No. 8 pp. 589–591 April 2014.

CTA adapted from Kotani et al. 1998

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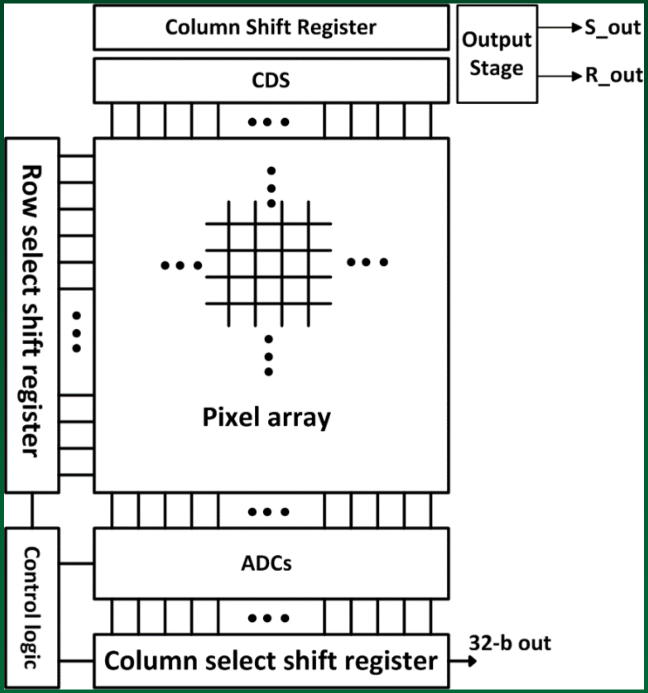
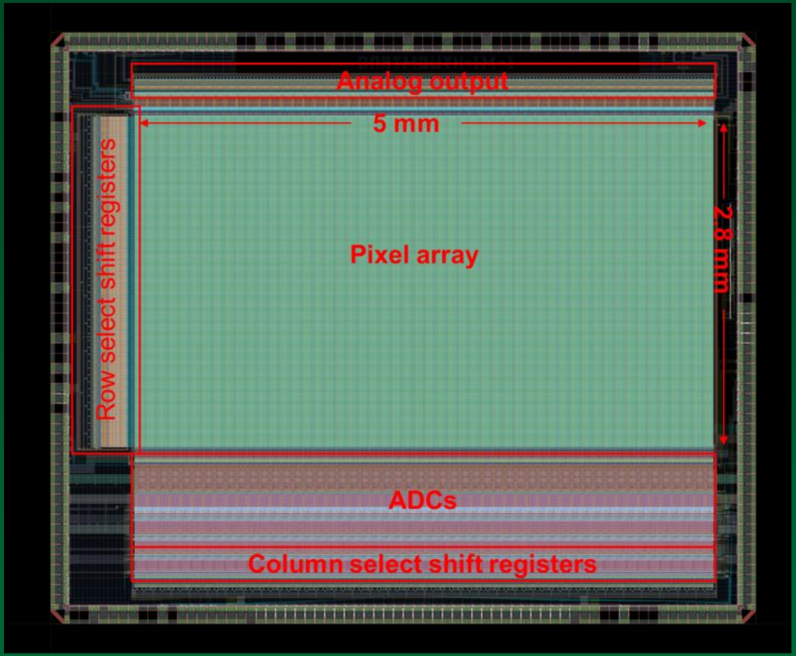
23mW 1000fps
1 Mpix binary image sensor





1 captured frame,≲5e-

- XFAB 0.18um 1.8V
- 1376(H) x 768(V) 3.6um 3T CDS
- 200uV/e- (sim)
- 768KSa/s
- 1 Gb/s data rate
- Whole chip incl. pads 23mW
- ADCs 5.6mW
- Energy 5.3pJ/b

Masoodian, Rao, Ma, Odame, Fossum 2014 unpublished

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65nm pathfinder for 1 Giga jot at 1000fps

- 1Gjot imager might be 42,000(H) x 24,000(V)
- Limited space for Dartmouth on multi-project chip on multiproject wafer so only 32 columns
- There are 24,000 pixels in each column.
- Power consumption per column is multiplied by 42,000 to get the power consumption of a 1Gjot imager.

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65nm pathfinder for 1 Giga jot at 1000fps

<table>
<tr><td>Process</td><td colspan="3">65nm, 1P5M</td></tr>
<tr><td>VDD</td><td colspan="3">1.2V (Analog), 2.5V (Array)</td></tr>
<tr><td>Pixel type</td><td colspan="3">4-shared PPD, 1.75T/pixel</td></tr>
<tr><td>Pixel pitch</td><td colspan="3">1.4um</td></tr>
<tr><td>Array</td><td colspan="3">32(H) X 24000(V)</td></tr>
<tr><td>Frame rate</td><td colspan="3">1000fps</td></tr>
<tr><td>Column noise</td><td colspan="3">< 150uV</td></tr>
<tr><td>ADC sampling rate</td><td colspan="3">24MSa/s</td></tr>
<tr><td>ADC input referred offset</td><td colspan="3"><500uV</td></tr>
<tr><td>Output data rate</td><td colspan="3">32 (output pins) X 24 Mb/s</td></tr>
<tr><td rowspan="3">Estimated Power (Binary imager)
0.6 pJ/b</td><td></td><td>One column</td><td>1Gjot
(42K column)</td></tr>
<tr><td>Array</td><td>50uW</td><td>2.1W</td></tr>
<tr><td>ADC</td><td>15uW</td><td>0.63W</td></tr>
</table>

Taped out July 2014

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Single Bit v. Multi-bit

Single Bit

- Each jot produces 1 bit
- 1 bit ADC
- For same flux capacity, need higher frame rate readout
- Conceptual simplicity
- Easier on chip digital electronics

Multi-bit

- Each jot produces n bits
- n-bit ADC
- For same flux capacity, lower relative frame rate $1/2^{(n-1)}$
- Like current CMOS APS but low FW capacity and high conversion gain

*S, Chen, A. Ceballos, E.R. Fossum, 2013 IISW

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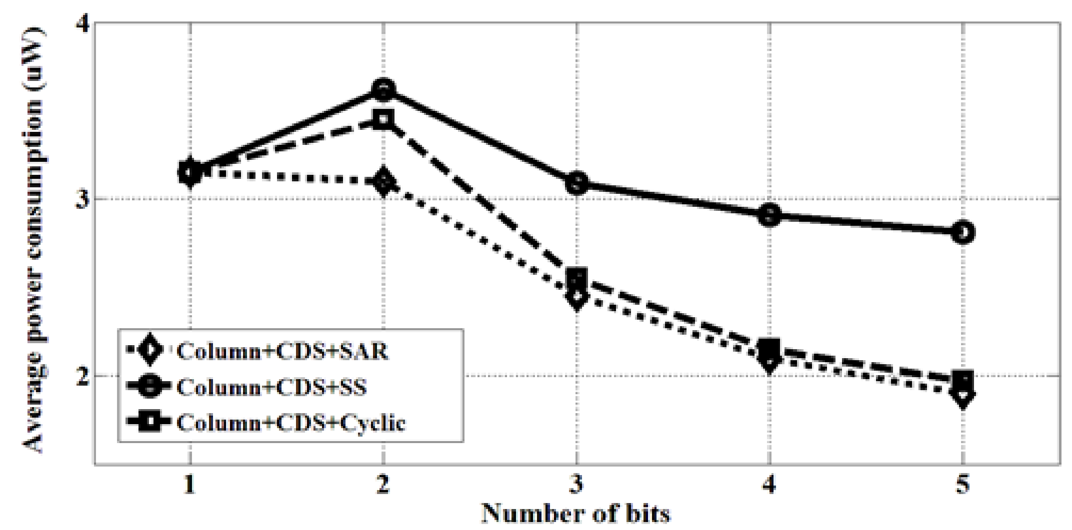
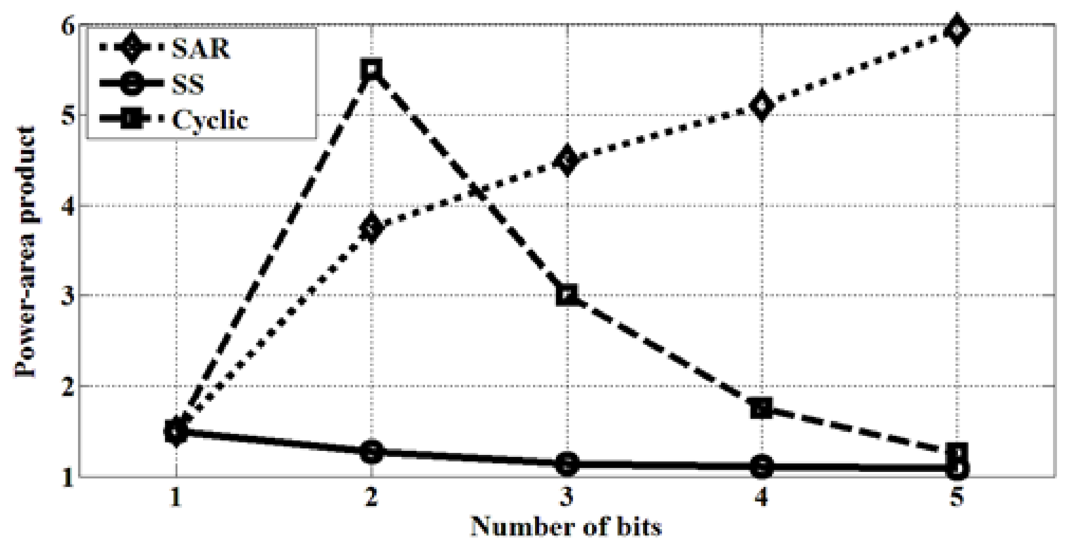
Single Bit v. Multi-bit Power Comparison (Constant Flux Capacity)





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Transforming the Jot Data Cube into Images

Rachel Zizza, Yue Song and E.R. Fossum

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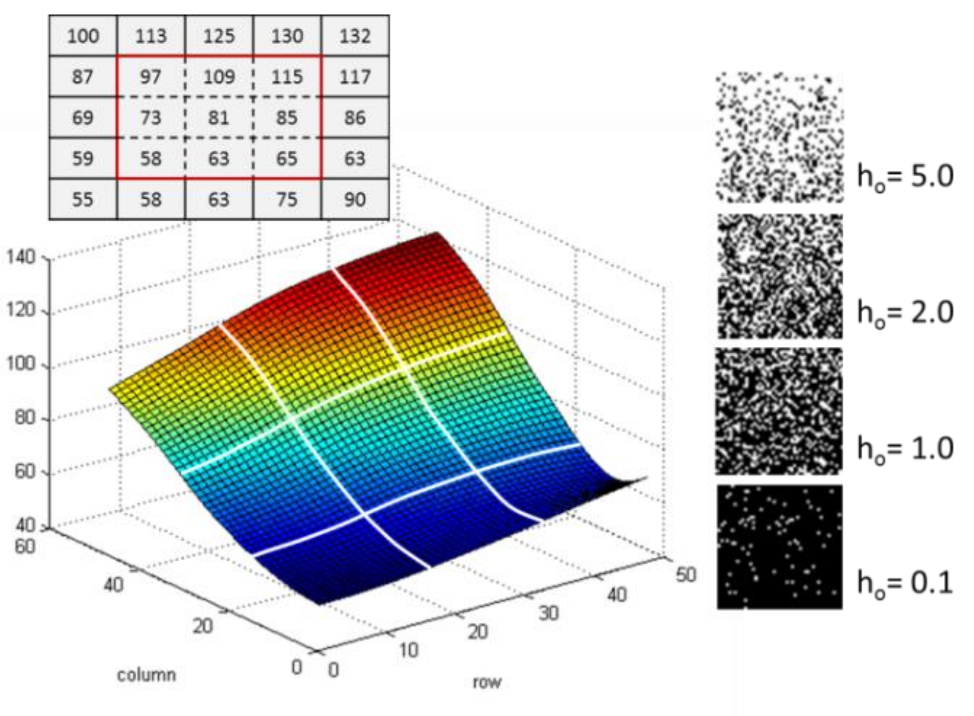
End to End System Simulation

Input Image
256x256 8b = 0.5 Mb

→ 4096x4096 1b x 16 fields = 256 Mb



100	113	125	130	132
87	97	109	115	117
69	73	81	85	86
59	58	63	65	63
55	58	63	75	90

$$H = \frac{S_H h_o}{255}$$

Output Image
1024x1024 8b

in this example

1 pixel = Σ 4x4x16 jots

$$SNR \leq \sqrt{256}$$

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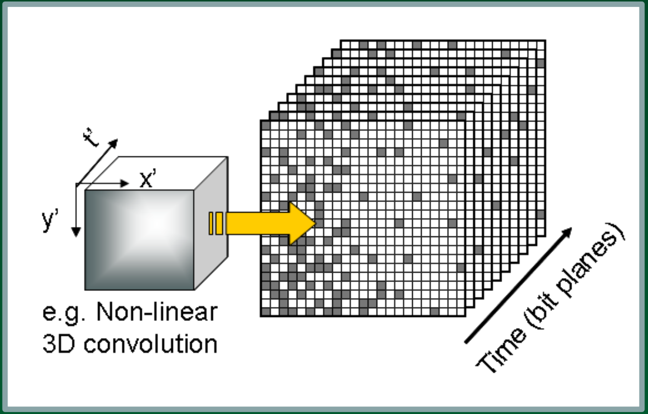
Convolution

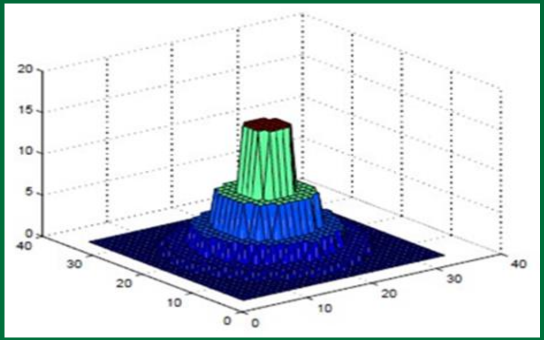


2D Examples:

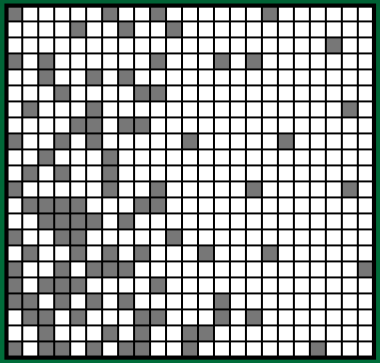
Binary valued filter

1	1	1	1
1	1	1	1
1	1	1	1
1	1	1	1

Binary-weighted filter

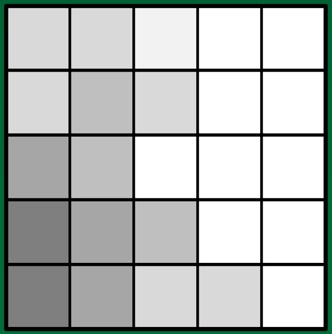


*



jot data

Down sample



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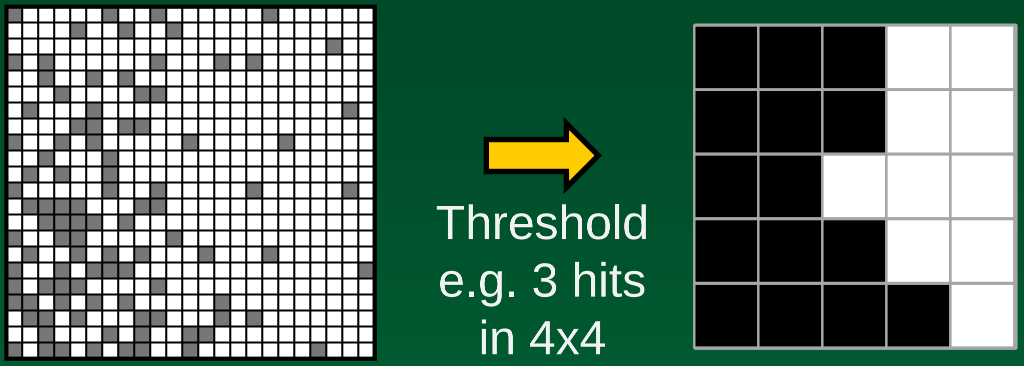
Digital Film Sensor Algorithm



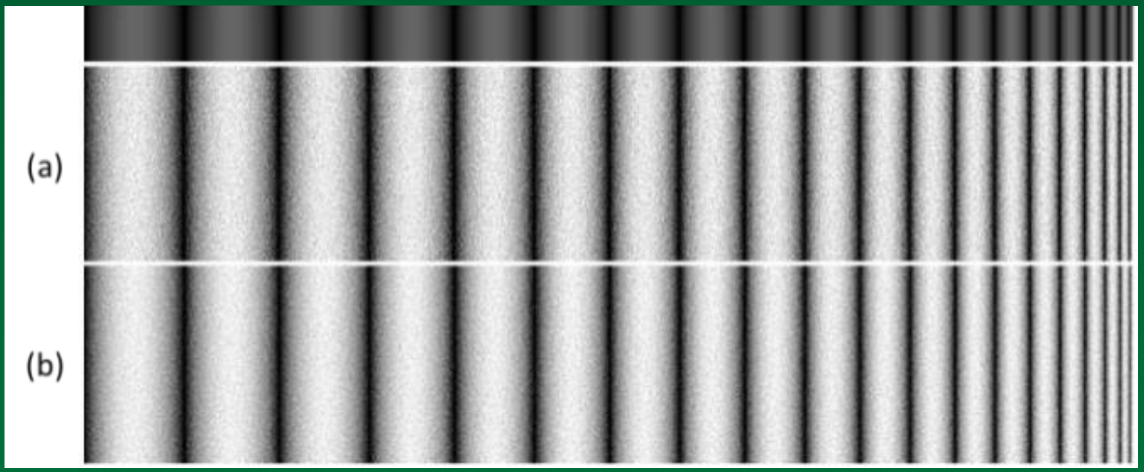
Threshold
e.g. 3 hits
in 4x4

“gain”

Synthetic input image

After DFS development

Plus filter with dynamic kernel size



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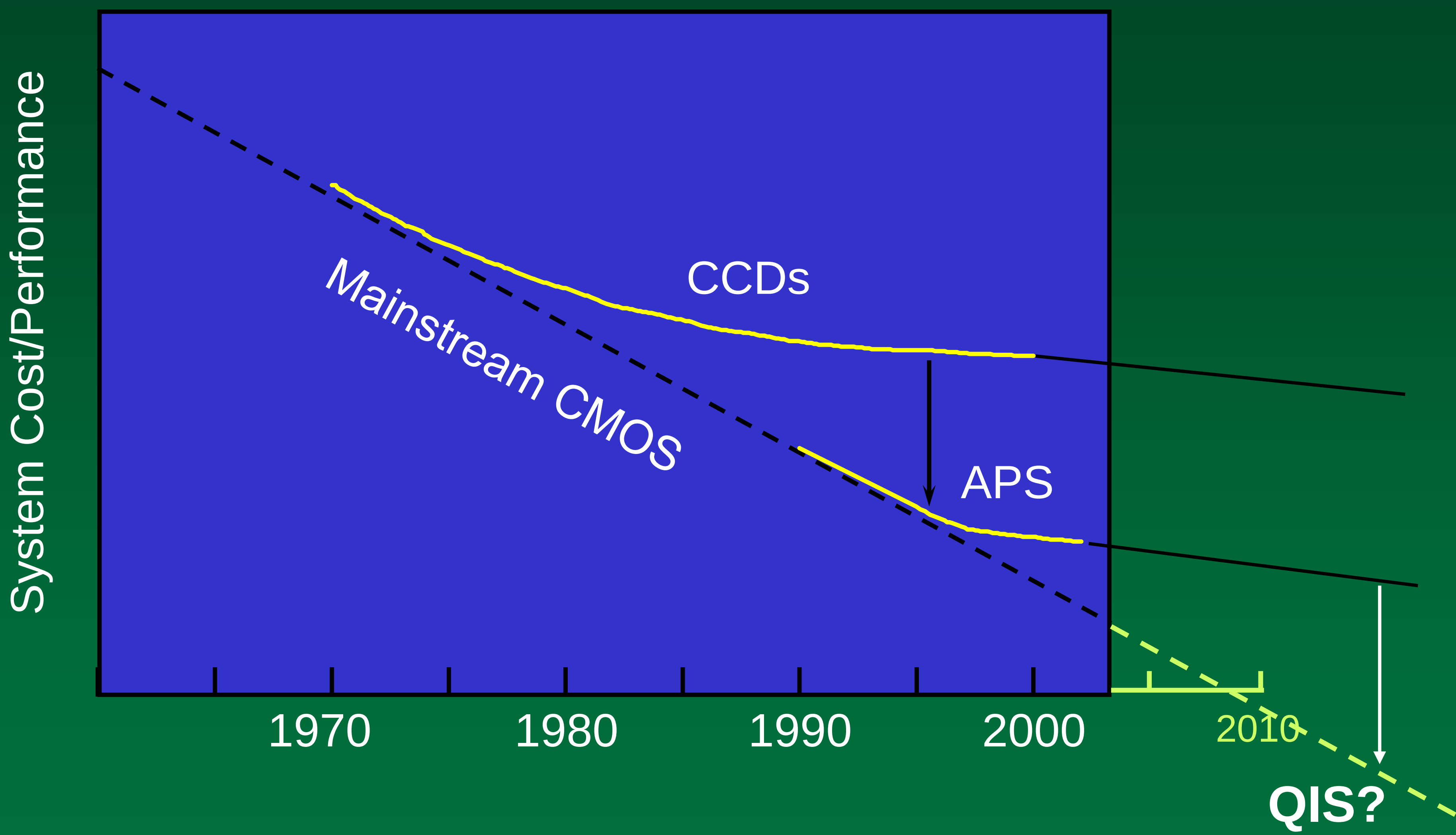
THAYER SCHOOL OF ENGINEERING AT DARTMOUTH

From the Late 1990's



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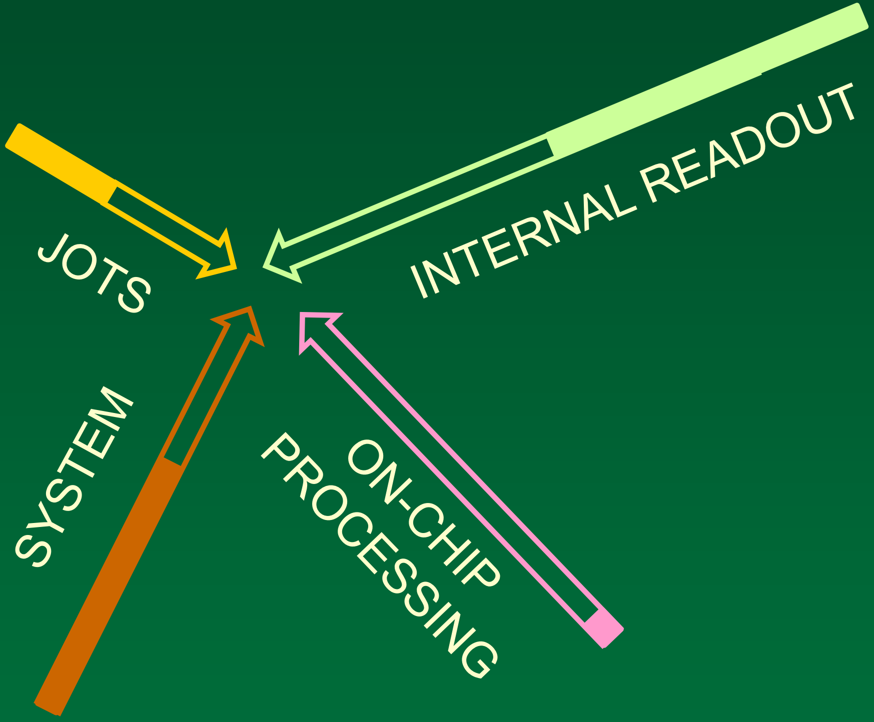
QIS implementation requires Devices, Circuits, and System

Strawman numbers

- <500 nm jot pitch
- Gigajot QIS (10^9 jots)
- 1000 fps
- 1 Tb/s data rate
- 1 Watt or less (<1pJ/b)



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Summary

- In July 2011, concept but no funding, no lab, no students
- Good progress in understanding response v. exposure, SNR, DR, etc. using photon statistics
- Progress made on realizing Quanta Image Sensor using mainstream processes
- 2-1/2 years support of Rambus (thanks Rambus!)
- Students up to speed and making great headway
- Challenges don’t look as challenging
- Lots of work still to do!

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