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Vertical Fiber Coupling for High-Density Optical Interconnection

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Abstract

A GaAs/AlGaAs fiber-optic interconnect structure for high-density applications is discussed. The vertical approach, which employs reactive-ion-etched cavities to couple fibers to the semiconductor substrate, permits interconnect arrays with densities up to 1600 sites/cm^2. Factors affecting the applicability of the fiber coupler and the achievable packing density are considered.

1. Introduction

The use of optical fibers for data transmission is most prevalent in telecommunications, where single fibers interconnect discrete laser-detector pairs operating at very high data rates. In this application, coupling between the optical fiber and the semiconductor is achieved with the aid of multi-component assemblies which are typically larger than the device chips themselves. Applications requiring the connection of several fibers to a single chip are now being explored, spurring the development of coupling techniques that are more real-estate efficient than those used in telecommunications.[1,2] Motivations for coupling many fibers to a single chip include a desire for interconnect redundancy, a demand for greater off-chip communication capacity, and the necessities of signal routing within computers. Parallel optical computing, for example, calls for propagation of multiple data streams between successive planes of logic elements, and will have a great need for 2-D optical-interconnect arrays. This paper describes a coupling technique which addresses that need by facilitating multi-fiber connection to the interior of a GaAs/AlGaAs optoelectronic integrated circuit (OEIC). Because dense optical interconnection involving detector arrays is a more likely near-term prospect than that involving sources, the context will be primarily that of fiber-detector coupling.

Optical signals may be brought onto an OEIC by propagation through free-space or through monolithically integrated waveguides, as well as by fiber-optics. Free-space interconnection schemes suffer from line-of-sight limitations and the need for precision placement of device chips and/or holographic steering elements. Waveguide interconnection schemes require two coupling interfaces for each detector: between the external light source and the waveguide, and between the waveguide and the active device. Coupling at the device interface is typically carried out by thin film gratings or tapers. At the external interface, the coupling problem usually becomes one of fiber-to-waveguide attachment. This is usually addressed with Si V-groove microassemblies, using a hybrid method originally developed for fiber-optic array splicing.[3] A center-to-center spacing of 250 μm can be obtained, along with a mean excess insertion loss of 0.35 dB/channel.[4]

The Si V-groove positioning technique is also used for lateral fiber coupling to optoelectronic device arrays, and connection of as many as 12 fibers to a single chip has been demonstrated.[1] For such

applications, a beveled fiber termination is needed to reflect the signal perpendicular to the optical axis and into the detector, typically introducing 1 dB loss. Lateral fiber coupling limits the placement and overall number of optical interconnects, as it utilizes only the chip periphery. However, because it is compatible with the planar packaging technology used today for high-speed integrated circuits, it is the most extensively developed multi-fiber connection technique.

A vertical fiber coupling approach, in which the fiber axis is normal to the semiconductor surface, permits a greater number of interconnects to be addressed to a single chip because it utilizes the chip interior. Furthermore, lossless illumination of planar photodetectors by unmodified optical fibers is only possible using a vertical fiber interconnection. This paper focuses on the capabilities and limitations of a specific vertical fiber coupling technique, with particular attention to its range of applicability, and to factors affecting the achievable interconnect packing density.

2. Fabrication Overview

Methods for vertical fiber coupling to Si- and GaAs-based photodetectors have recently been developed, and the details of the semiconductor fabrication processes used have been presented elsewhere.[5-7] The techniques involve vertical insertion of optical fibers into frontside and backside cavities etched in the respective semiconductor substrates. The backside GaAs coupler, shown schematically in Fig. 1, is superior in terms of responsivity, projected speed, and crosstalk. Its fabrication process is outlined below, and the effects that processing limitations will have on its general applicability are examined.

Photodetectors were fabricated using a standard metal liftoff process, in epitaxial layers grown by metalorganic vapor phase epitaxy (MOVPE). The layers consisted of 0.4 μm n-GaAs (FET active layer), 1 μm undoped GaAs, and 4 μm undoped $Al_{0.35}Ga_{0.65}As$, and the substrate was semi-insulating GaAs. The detectors used were metal-semiconductor-metal (MSM) diodes and photosensitive metal-semiconductor field effect transistors (MESFETs). These detectors were selected because of their ease of fabrication and as a demonstration of the compatibility of the coupling structure with standard GaAs circuitry. Following the frontside device processing sequence, fiber coupling cavities are etched from the backside of the wafer to the epitaxial detector sites.

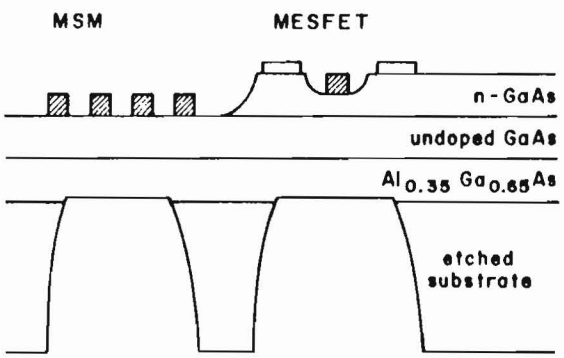

Fig. 1. Schematic cross-section of GaAs fiber-optic coupler.

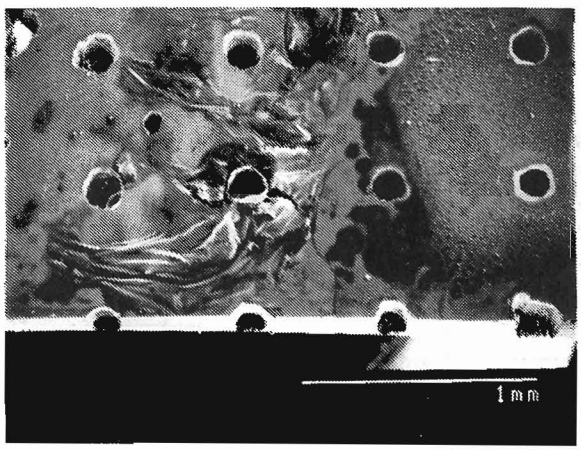

Fig. 2. Scanning electron micrograph of an array of fiber-coupling cavities in GaAs.

An etched cavity is needed for backside illumination of the detectors because the GaAs substrate is opaque, and because complete removal of the substrate would leave a membrane too thin for handling. Reactive ion etching (RIE) is used to form the cavity since it permits a higher packing density of cavity-coupled interconnection sites than wet etching. To obtain efficient transmission of the optical signal

from the fiber end-face to the epitaxial detector region, an absorption-free surface without excessive roughness must result from the etching process. Insertion of an AlGaAs window/stop-etch layer is the best way to obtain this, due to its large bandgap ($E_g \simeq 1.8$ eV) and low etch rate (60 nm/min) in the CCl_2F_2 RIE process. The necessity of including an AlGaAs layer represents the primary limitation on the applicability of the fiber-optic coupler, in its present form.

Few restrictions are placed on the composition of the epitaxial structure, other than inclusion of the AlGaAs stop-etch layer, so a broad range of circuit types can be addressed by optical interconnects using this approach. The active layers may be grown by any epitaxial technique, and must remain unaffected by the AlGaAs growth on the substrate. The first design iteration called for an AlGaAs thickness of 4 μm, to provide insurance against possible nonuniformities in cavity etch rates across a sample. Early MBE-grown batches exhibited defects attributable to poor quality growth initiating in the thick AlGaAs layer. The MOVPE wafers, however, have always shown excellent characteristics. For the next set of wafers, the uniformity of the selective etching process will permit a 50% reduction in the stop-etch layer thickness. The remaining layers may be optimized for combined optical and electronic performance. There are many heterostructure devices which are compatible with an AlGaAs buffer layer, and there have been reports that large bandgap buffer layers may lead to improved MESFET performance.[8] The prototype detector structure shown in Fig. 1 is in fact similar to that of the inverted high electron mobility transistor (HEMT), a high-performance device holding several advantages over the conventional HEMT.[9] Finally, optical modulator and source structures can also be fabricated in the (Al,Ga)As multilayers (although they present a more difficult packaging challenge).

A key aspect of the processing sequence for vertical fiber interconnects is the decoupling of the back- and front-surface fabrication (i.e., the special steps for cavity formation are performed after the completion of the frontside device processing sequence). Thus, existing circuits can be retrofit for fiber-optic interconnection in a few short steps: deposition and patterning of an RIE-resistant mask on the back surface, etching of cavities through the substrate to the sites targeted for optical signal injection, and fiber packaging (a process which is appended to the die attachment and wire bonding sequence). The retrofit capability may lead to early applications of the backside GaAs fiber coupler as a means of adding optical inputs to pre-designed circuitry.

3. Interconnect Density: Capabilities and Comparisons

An estimate of the maximum achievable packing density for fiber-optic interconnection using the backside cavity approach can be derived from certain characteristics of the fabrication process. The RIE process used in cavity formation employs a relatively high pressure (40 mTorr), in order to simultaneously realize a high GaAs etch rate (> 2 μm/min) and a large material selectivity (> 30). This reduces the directionality of the etch, resulting in a lateral to vertical etch rate ratio of 1:10, and a typical 5-10° tilt of the sloped cavity sidewalls away from vertical. To permit the endface of a standard fiber (125 μm outer diameter) to be positioned close to the epitaxial photodetector, the circular opening on the backside of the wafer must be 175 μm in diameter. Leaving an additional distance of 75 μm for structural integrity yields a center-to-center cavity spacing (pitch) of 250 μm. An estimate of the achievable packing density for cavity-coupled fiber-optic interconnection is therefore one site per $(250\ \mu m)^2$, or 1600 sites/cm^2. This is close to the largest maximum theoretical value for standard optical fibers (7900/cm^2 - obtained for a hexagonal-close-packed bundle of bare fibers). Extensive RIE experiments involving groups of 2-3 etched cavities have confirmed the feasibility of placing a small number of couplers on a 250 μm pitch, but an additional set of experiments must be done to determine whether a GaAs substrate can support a more extensive array. This is likely, since a large array of cavities on 500 μm centers has been fabricated without difficulty, as shown in Fig. 2.

The estimated packing density of 1600 sites/cm^2, or 4 sites per mm for a linear array, is remarkably close to that of several state-of-the-art interconnect technologies, both electrical and optical. Conventional wire bonds, laterally coupled optical fibers, and solder bumps[10] all have packing density limits near this value. Assuming a 250 μm pitch in each case, the maximum number of coupling sites per

chip, and hence the net off-chip communication capacity, was calculated for each interconnect technique. Single-channel bandwidths of 1 GHz and 100 MHz were assumed for the optical and electrical signals, respectively. The results of the calculation are shown in Fig. 3, where the maximum communication capacity offered by each technique is plotted as a function of chip size. Note that two-dimensional interconnect arrays permit significantly higher throughput, since their total capacity increases in proportion to chip area rather than circumference.

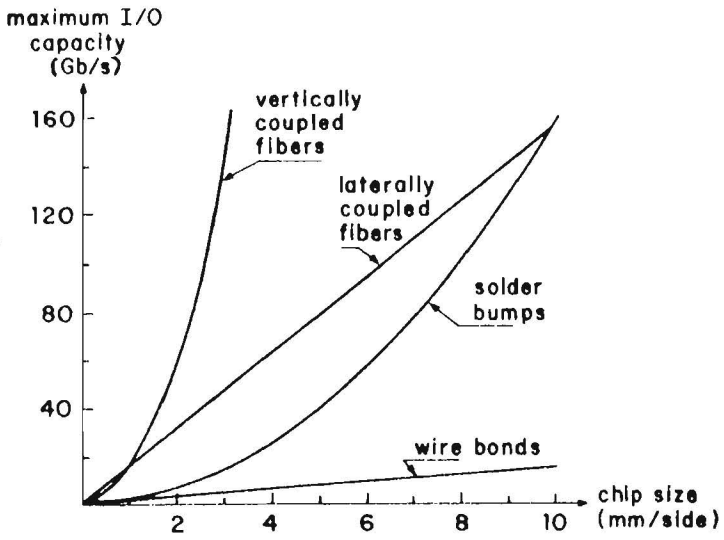

Fig. 3. Maximum off-chip communication capacity for several interconnection techniques. A pitch of 250 μm is assumed for both planar and linear arrays.

Because any given circuit is likely to require electrical as well as optical interconnections, the complementarity of the interconnect techniques is an important issue. Use of solder bumps, which offers the greatest total electrical communication capacity, precludes both conventional wire bonding and lateral fiber coupling, because they require access to the front surface of the chip. In addition, wire bonds and laterally coupled fibers require the same connection sites - those on the periphery of the chip's front surface. The vertical fiber coupler is the only method that does not compete for real-estate with the other types of interconnection. This is a consequence of the backside fiber approach, which also presents fewer difficulties with regard to the front-surface device layout. For example, both of the electrical interconnect techniques require contact areas on the order of $(100\ \mu m)^2$ to be entirely covered with metallization, whereas the chip area required by a photodetector for a single-mode fiber is ideally just the footprint of the core. Some MSM photodiodes used in demonstrating the vertical fiber coupler employed 16 μm X 16 μm active regions.

4. Packaging Considerations

The above estimate of interconnect density for cavity-coupled fibers is only dependent on characteristics of the semiconductor fabrication process. It does not account for possible limitations due to packaging considerations. However, because the alignment tolerance and estimated pitch are no smaller than those already used in lateral fiber coupling, it is expected that practical packaging techniques for coupling to arrays of such density can be devised.

Development of packaging procedures for the vertical fiber coupler is at a very early stage. One question involves the extent to which the cavity should be relied upon to position and anchor the fiber. When a suitable external alignment assembly is provided, the backside cavity will be needed only as a transparent window through the substrate. The external microassembly for fiber positioning must in this case be precisely machined and stably aligned to the semiconductor substrate. A stack of silicon V-

grooves might serve as the positioning fixture for a 2-D fiber array, but its opacity and extended vertical profile could prove inconvenient. In addition, V-groove techniques inhibit the flexible layout of interconnection sites by requiring them to be grouped in linear arrays. Silicon micromachining with excimer lasers, as demonstrated at Columbia,[11] can also be used to form a customized 2-D array of via holes for fiber positioning. Because the opacity of the silicon substrate would complicate alignment and assembly, a similarly micromachined transparent glass holder would be better suited to this application.

A generic method for aligning and fixing a two dimensional fiber array with respect to a detector array is illustrated in Fig. 4. It addresses several problems inherent in one-fiber-at-a-time attachment schemes, such as long assembly times and mechanical difficulties associated with sequentially epoxying a number of closely spaced fibers. Another problem it addresses, unique to the backside coupling structure, arises from the fragility of the epitaxial diaphragm supporting the GaAs photodetectors. This diaphragm is susceptible to breakage if the fiber is inserted too far into the coupling cavity. To date, fiber tapering and tight cavity dimensions, in conjunction with a UV-cured adhesive applied to the back surface of the wafer, have been used to hold the fibers in place. This measure is not acceptable as a long-term solution, and an additional fixture, as indicated in Fig. 4, is probably necessary to ensure mechanical stability. The fixture positions the fibers accurately in all three dimensions, preventing breakage of the diaphragm as well as lateral misalignment.

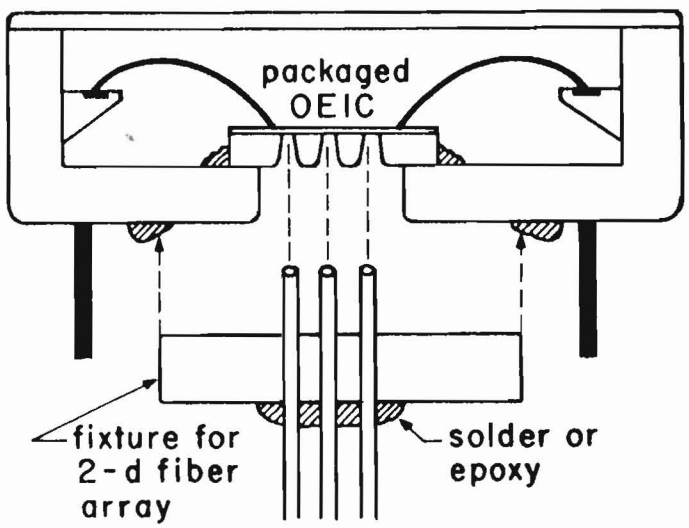

Fig. 4. Schematic diagram of a packaged device accomodating backside fiber-optic interconnects.

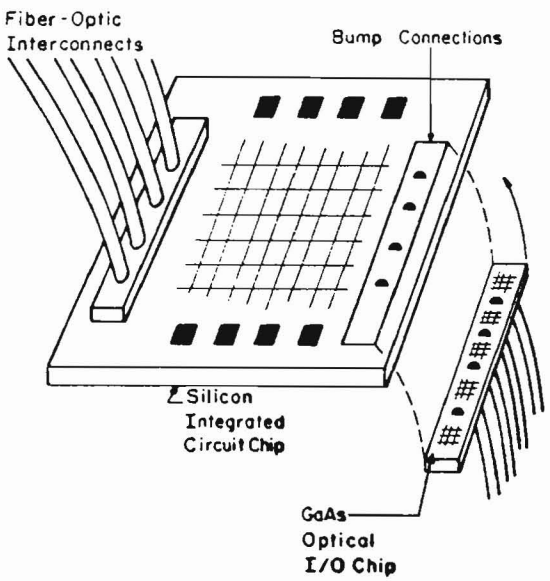

Fig. 5. Depiction of a multi-chip GaAs-on-Si approach for VLSI optical interconnects.

5. Discussion

As noted above, a cavity-coupled fiber-optic interconnect can only be realized in GaAs OEIC structures containing an AlGaAs stop-etch layer. For example, connection to all-implanted GaAs digital IC's is not possible, because no technique has been developed for etching vertical cavities in bulk GaAs samples and terminating the etch cleanly a few microns from the front surface. However, this sort of limitation is not as severe as one might initially suspect, as a consideration of specific optical interconnection

scenarios readily shows. Consider the case of board-level optical interconnection: here, a relatively small number of chips are needed for high-speed optical I/O and for multiplexing received signals to the lower-speed processing circuits. This function is best performed by (Al,Ga)As heterostructure devices capable of fast operation and efficient optical detection; these devices will require epitaxial growth runs, which opens the door for the inclusion of an AlGaAs stop-etch layer.

Another question of applicabilty has to do with the optical interconnection of Si circuitry. Because of the prevalence of silicon VLSI in computers, widespread use of the GaAs fiber coupler for optical interconnection applications may depend on hybrid approaches. Multi-chip integration, with both semiconductor substrates embedded in a common potting material,[12] has been proposed as a means of realizing electrical interconnection between a Si VLSI circuit and a GaAs optical I/O chip. Epitaxial growth of GaAs on silicon,[13] which possesses the advantage of monolithic integration, is an alternative approach which is currently receiving much attention. Another approach, illustrated in Fig. 5, could employ solder bumps to make electrical connection between the GaAs and silicon chips.

6. Conclusion

A vertical fiber coupling technique allowing optical interconnection to devices located in the interior of a GaAs/AlGaAs integrated circuit has been discussed. Its chief advantage over lateral coupling techniques is an ability to address high-density 2-D arrays, which is essential for future applications in optical computing. Fabrication of fiber-optic interconnect arrays with densities greater than 10^3 channels/cm^2 may be possible using the backside-cavity vertical fiber coupler. Realization of the full potential of this integrated coupling structure, and of vertical fiber coupling in general, will come only with the development of specialized optoelectronic packages.

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