A 1.25-inch 60-Frames/s 8.3-M-Pixel Digital-Output CMOS Image Sensor

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***Abstract*—The ultrahigh-definition television (UDTV) camera system requires an image sensor having four times higher resolution and two times higher frame rate than the conventional HDTV systems. Also, an image sensor with a small optical format and low power consumption is required for practical UDTV camera systems. To respond to these requirements, we have developed an 8.3-M-pixel digital-output CMOS active pixel sensor (APS) for the UDTV application. It features an optical format of 1.25 inch, low power consumption of less than 600 mW at dark, while reproducing a low-noise, 60-frames/s progressive scan image. The image sensor is equipped with 1920 on-chip 10-bit analog-to-digital converters and outputs digital data stream through 16 parallel output ports. Design considerations to reproduce a low-noise, high-resolution image at high frame rate of 60 fps are described. Implementation and experimental results of the 8.3-M-pixel CMOS APS are presented.**

***Index Terms*—Active pixel sensor, CMOS image sensor, HDTV, parallel architecture.**

I. Introduction

WITH SATELLITE digital broadcasting using a 2-million-pixel High-Definition Television (HDTV) format, and digital cinemas being reduced to practical use, a 4 k $\times$ 2 k format is considered as the next-generation format [1], [2]. Technology developments toward the ultrahigh-definition image capture have thus been actively performed [3]–[6]. Examples of ultrahigh-resolution image sensors, of which resolution exceeds the HDTV standard, include a 2.5-inch optical format CCD image sensor with 4080 (H) $\times$ 2040 (V) pixels [3], [6] and a 35-mm optics compatible CMOS image sensor with 3840 (H) $\times$ 2160 (V) pixels [4], operating in a progressive scanning mode at 60 frames/s and at 30 fps, respectively. Due to the large format sizes of these sensors, it was difficult to realize compact camera systems. Also, a CCD-based camera head consumes power of greater than 10 W per channel. Lowering the sensor power consumption would offer a significant benefit. It simplifies camera-head design and prevents the heat generation inside a camera head, and thus can avoid an unnecessary increase of temperature.

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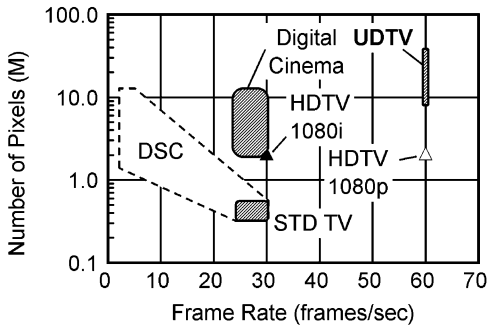

Fig. 1. Distribution of image sensor formats for video applications. Note that our sensor is positioned at 60 fps and 8 M-pixels.

A data rate exceeding 500 MHz, that is 8 times higher than that of the HDTV, is required to achieve a 60-fps operation with a pixel count of over 8 million pixels. The image sensors cited above have parallel analog output ports to realize this effective data rate. For example, the CCD sensor [3] has 16 parallel output ports, each operating at 37.125 MHz. However, this analog approach complicates analog processing circuits in a camera head. A full digital output scheme could alleviate this difficulty. Therefore, a smaller format sensor with lower power consumption and full digital interface is highly demanded.

In order to respond to this demand, we have developed a 1.25-inch, 8.3-M-pixel digital-output CMOS image sensor, which can operate at 60 fps in a progressive scanning mode. The sensor specification matches the standard Real-time HRI-01 [1] that was proposed by ITU (International Telecommunication Unit) for next-generation extremely high-resolution motion pictures in 1995.

Fig. 1 shows how each imaging application is mapped as a function of the frame rate and the number of pixels. The developed sensor covers most of the imaging applications, including UltraHigh Definition TV (UDTV) and digital cinema applications.

In this paper, design considerations to realize a large-format high-resolution high-frame-rate digital-output CMOS image sensor are described in Section II. Implementation of the image sensor is presented in Section III, followed by descriptions of characterization results in Section IV.

II. Design Considerations

A. Choice of Optical Format

Previous sensors had relatively large pixel sizes (8.4 μm [3], [6], 7.5 μm [4]), which required a large lens, thus making it difficult to realize a compact and lightweight camera system.

Also, the large die sizes require a stitching technique to fabricate the devices, where multiple photolithography processes using several reticle sets are needed.

We selected a 1.25-inch optical format so that the die size of the chip fits into the standard reticle window of 20 mm × 20 mm, while attempting to design a pixel as large as possible from an optical performance point of view. In order to fit the imaging array having 8.3 M (3840(H) × 2160 (V)) pixels to the 1.25-inch format, a pixel size of 4.2 μm was chosen [7], [8].

B. Digital Output Versus Analog Output

It is obvious that a full digital interface eliminates complexity associated with designing analog front-end circuits. In particular, the benefit gains more in case the sensor having a multiple output ports to obtain sufficient effective data rate. In addition, the digital output scheme could have an advantage in power consumption over the analog output counterpart as described below. Assuming the digital output buffer has sufficient driving capability, the power consumed by digital output pads $P_{\mathrm{dig\_out}}$ is given by

$$P_{\mathrm{dig\_out}} = \sum_{i=1}^{N_{\mathrm{bit}}} \alpha_i \cdot C_L \cdot V_{\mathrm{DD}}^2 \cdot f_{\mathrm{data}} \tag{1}$$

where N_{bit} is the number of ADC bits, α_i is the transition probability for the ith bit for a given illumination level, C_L is the load capacitance, V_{DD} is the digital power supply voltage, and f_{data} is the effective data rate. On the other hand, the power consumed by an analog output buffer is represented by

$$P_{\mathrm{ana\_out}} = \frac{1}{T}\int_0^T V_{\mathrm{AA}} \cdot i_{\mathrm{AA}}(t) \cdot dt \tag{2}$$

where V_{AA} is the analog power supply voltage, i_{AA} is a current flowing through V_{AA}, and T is the time period, most likely a frame time, respectively. If we consider an average value of the output current over the frame time, (2) is rewritten as

$$P_{\mathrm{ana\_out}} = V_{\mathrm{AA}} \cdot I_{\mathrm{AA}}(\Delta f) \tag{3}$$

where the average current I_{AA} is a function of Δf, which is the required frequency bandwidth for the output buffer. Assuming a single-pole buffer, the frequency bandwidth is given by

$$\Delta f = \frac{g_m}{2\pi C_L}. \tag{4}$$

With a formula of the transconductance g_m of a MOS transistor of

$$g_m = \sqrt{2\mu \cdot C_{\mathrm{OX}} \cdot (W/L) \cdot I_{\mathrm{AA}}} \tag{5}$$

where μ denotes the mobility, C_{OX} the gate capacitance per unit area, W the width and L the length of a primary transistor in the buffer. From (4) and (5), one can obtain

$$I_{\mathrm{AA}}(\Delta f) = \frac{2(\pi C_L)^2}{\mu \cdot C_{\mathrm{OX}}} \cdot \frac{\Delta f^2}{(W/L)}. \tag{6}$$

It is seen in (6) that the required current is proportional to the square of the frequency bandwidth. Comparing (1) and (2) with other equations, it is concluded that the digital output scheme consumes less than the analog output scheme in the case of

$$f_{\mathrm{data}} > \frac{\alpha \cdot N_{\mathrm{bit}} \cdot \mu \cdot C_{\mathrm{OX}} \cdot (W/L) \cdot V}{2\pi^2 \cdot m^2 \cdot C_L} \tag{7}$$

where $V = V_{\mathrm{DD}} = V_{\mathrm{AA}}$, α is an effective transition probability [see (1)], and m is a factor that relates the frequency bandwidth Δf and the data rate f_{data} ($\Delta f = m \cdot f_{\mathrm{data}}$). An example illustrating the relationship (7) is shown in Fig. 2, where the identical capacitive loads (C_L) for both cases are assumed. From the figure, it is shown that power consumption of the digital approach is lower than that of the analog counterpart when the data rate greater than a few tens of MHz is required.

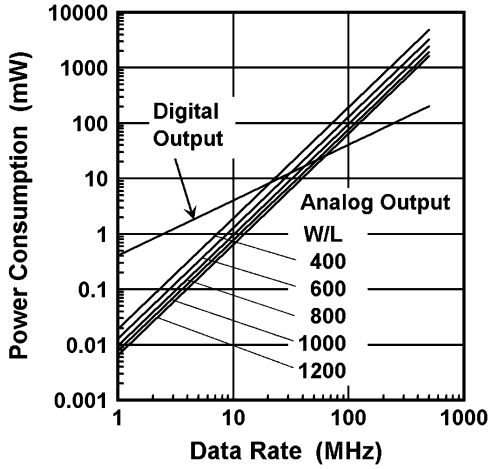

Fig. 2. Power consumption of output buffers as a function of data rate. Parameters: $V = 3.3$ V, $C_L = 15$ pF, $\mu \cdot C_{\mathrm{ox}} = 60\ \mu$A/V^2, $m = 4, \alpha = 0.25, N_{\mathrm{bit}} = 10$. For analog buffers, $(W/L) = 400,\ 600,\ 800,\ 1000, 1200$.

C. Rationale of Column Parallel On-Chip Analog-to-Digital Conversion

In this subsection, power consumption and noise of two architectures of CMOS image sensors with on-chip analog-to-digital converters (ADCs) are analyzed: one is with only one ADC (called the "serial ADC" type) and the other with column parallel ADCs, where an ADC is placed in each column and where all ADCs operate in parallel. The serial ADC operates at a pixel output rate, while each ADC in the column parallel architecture operates at the row rate. Let us take an image sensor, having $N_H \times N_V$ pixels and operating at FR frames/s.

1) Power Consumption: Conversion rates for the serial and column-parallel approaches are approximately given by

$$f_{\mathrm{CONV\_S}} = N_H \cdot N_V \cdot FR \quad [\mathrm{Hz}] \tag{8}$$

$$f_{\mathrm{CONV\_CP}} = \frac{1}{1H} = N_V \cdot FR \quad [\mathrm{Hz}] \tag{9}$$

where $f_{\mathrm{CONV\_S}}, f_{\mathrm{CONV\_CP}}$, and 1 H denote the conversion rates of the serial and column-parallel architectures and the row time, respectively. Assuming a CMOS operational transconductance amplifier (OTA) is used in an ADC, the impact of the conversion rates on the power consumption is analyzed. The gain bandwidth (GBW) of the CMOS OTA is given by

$$\mathrm{GBW} \propto \frac{g_m}{C_L} \tag{10}$$

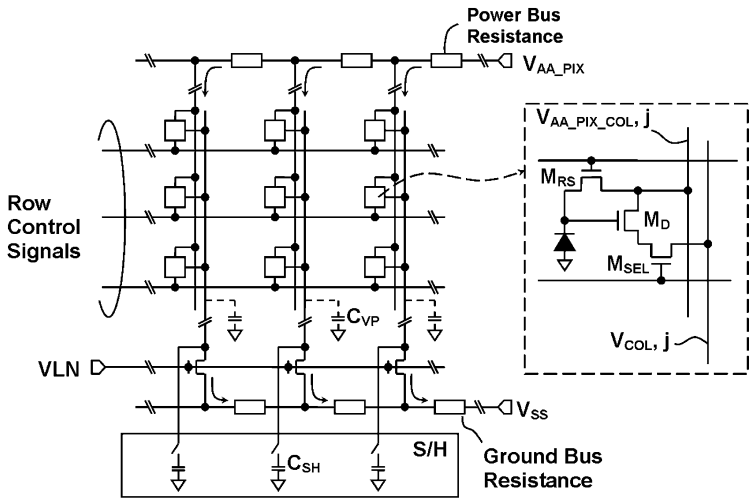

Fig. 3. Imaging array architecture of a CMOS image sensor.

where g_m and C_L are the transconductance given by (5), and the effective load capacitance, respectively. Now, as the bias current $I_{\rm bias}$ increases to obtain the required GBW that is determined from the conversion rate $f_{\rm CONV}$, so must $\mu C_{\rm OX}(W/L)$, in order to keep the same effective gate-source voltage $V_{\rm GT}$. Therefore, (10) is rewritten as

$$\mathrm{GBW} \propto \frac{I_{\rm bias}}{V_{\rm GT} \cdot C_L} \tag{11}$$

and thus $I_{\rm bias}$ goes up linearly with GBW, which yields identical power consumption for both architectures from (8) and (9), since GBW is proportional to $f_{\rm CONV}$ and there are N_H ADCs operating in parallel in the column-parallel architecture.

However, when we consider the parasitic capacitance at the input node of an OTA, the bias requirements in the serial ADC architecture become much greater, since the feedback factor of the amplifier degrades due to a larger input transistor and much larger parasitic capacitance connecting to the input node of the OTA. In addition, increasing W/L further in the serial ADC approach may be limited at a certain practical point, which in turn makes g_m proportional to $\sqrt{I_{\rm bias}}$. In this case, $I_{\rm bias}$ goes up with $(\mathrm{GBW})^2$ and thus the column-parallel approach is expected to provide lower power consumption.

2) Noise: In the switched capacitor circuit, the sampling process folds the noise from the high-frequency region to the frequency region below the sampling frequency. Amplifier thermal noise $n_{\rm amp}$ is proportional to GBW/g_m and the noise after sampling is given by

$$n_{\rm amp}^2 \propto \frac{\mathrm{GBW}}{g_m} \propto \frac{g_m}{C_L} \cdot \frac{1}{g_m} \propto \frac{1}{C_L}. \tag{12}$$

The kTC noise associated with a sample-and-hold operation has the same relationship as (12). Thus, noise level is independent of the sampling rate and the noise levels in both architectures are expected to be the same. However, it is very difficult to apply noise cancellation techniques to high-speed signal chains that would be used in the serial ADC architecture.

3) Conclusion: Although, in reality, different types of ADC should be considered to match the requirements and/or constraints of each architecture, it can be concluded from the discussions above that the column parallel architecture is expected to provide/yield both lower power consumption and lower noise levels than those of the serial ADC architecture, when the same ADC topology is used for both architectures.

D. Large Array Effect

If a large-format array is built based on the architecture shown in Fig. 3, a problem would occur due to the $I \cdot R$ drop along the power and ground lines. When a row is selected for readout, the pixel bias currents flow from $V_{\rm AA\_PIX}$ to $V_{\rm SS}$. During this readout period, voltages along the $V_{\rm SS}$ line cannot remain at the ground level due to parasitic resistance.

The bias current is given by

$$\begin{aligned} I_{{\rm BIAS},i} &= \frac{1}{2} \cdot \mu \cdot C_{\rm OX} \cdot \frac{W}{L} \cdot (V_{{\rm GS},i} - V_{\rm TH})^2 \\ &= \frac{1}{2} \cdot \mu \cdot C_{\rm OX} \cdot \frac{W}{L} \cdot (V_{\rm LN} - V_{{\rm SS\_COL},i} - V_{\rm TH})^2 \end{aligned} \tag{13}$$

where $V_{{\rm GS},i}$ is the gate-source voltage for the ith load transistor, MLD, $V_{{\rm SS\_COL},i}$ is the $V_{\rm SS}$ voltage at the column i, and $V_{\rm TH}$ is the threshold voltage. Thus, as the $V_{{\rm SS\_COL},i}$ rise due to the parasitic resistance on the ground line, the bias current decreases. The output voltage change due to the raised $V_{\rm SS}$ is approximately given by

$$\Delta V_{\rm OUT} = \sqrt{\frac{(W/L)_{\rm LD}}{(W/L)_D}} \cdot \Delta V_{\rm SS} \tag{14}$$

where $\Delta V_{\rm SS}$ is the voltage change on the $V_{\rm SS}$ line. This output voltage change could be suppressed by the correlated double sampling (CDS). The main concern is that the decreased bias currents due to the reduced effective $V_{\rm GS}$ of $\mathrm{M_{LD}}$ may result in variations in time constant for charging and discharging a

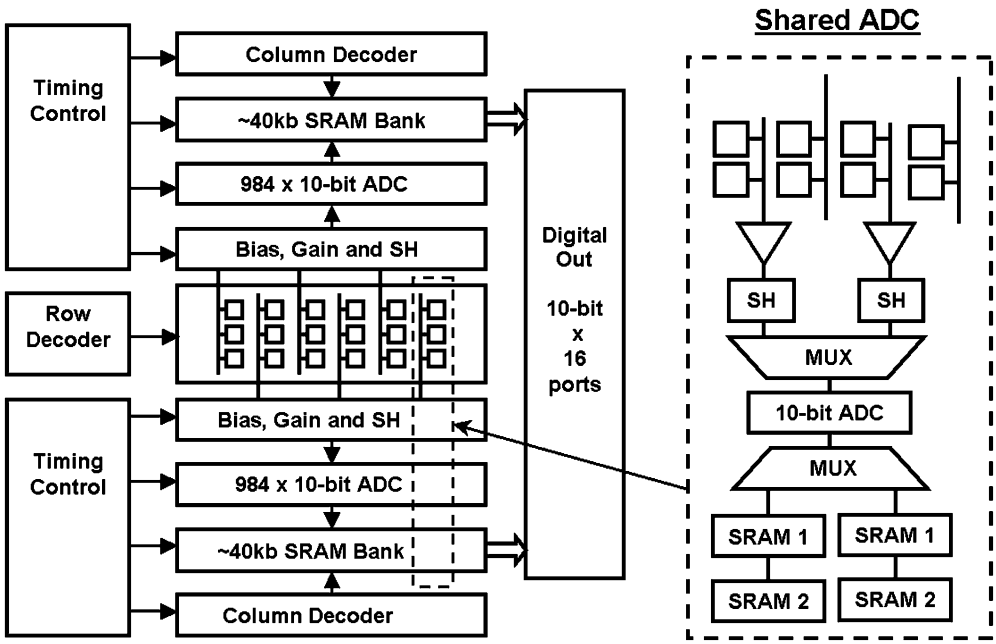

Fig. 4. Internal bock diagram of 8-M-pixel UDTV image sensor having a shared ADC architecture. Pixel pitch is 4.2 μm. Layout pitches of amplifier/sample-and-hold and ADC are 8.2 μm and 16.8 μm, respectively.

sample-and-hold capacitor $C_{\rm SH}$. The time constant of charging the sample-and-hold capacitor is approximately given by

$$\tau = \frac{C_{\rm SH} + C_{\rm COL}}{g_m} = \frac{C_{\rm SH} + C_{\rm COL}}{\sqrt{2\mu \cdot C_{\rm OX} \cdot (W/L)_D \cdot I_{\rm BIAS}}} \quad (15)$$

where $C_{\rm COL}$ is a parasitic capacitance on a column line. Thus, a resulting voltage on the hold capacitor may change when the pulsewidth of the sample-and-hold pulse is comparable to the time constant. This may happen since a higher resolution image sensor requires narrower pulse widths to obtain a given frame rate.

Another concern is the source follower gain variation due to the variation in bias currents.

The same mechanism of the voltage change applies to the $V_{\rm AA}$ line. However, it affects the output voltage little since the driver transistor $\rm M_D$ operates in its saturation region and thus the drain voltage has minimal affect on the drain current. The contribution from a change of $V_{\rm AA}$ to the pixel follower output is approximated as

$$\frac{\Delta V_{\rm OUT}}{\Delta V_{\rm AA}} \sim 1/(1 + g_m \cdot r_{\rm DS}) \quad (16)$$

where $r_{\rm DS}$ is the drain-source resistance of $\rm M_D$. A value of $(1 + g_m \cdot r_{\rm DS})$ is several tens to hundreds in a pixel source follower circuit, thus an output change $\Delta V_{\rm OUT}$ due to the $V_{\rm AA}$ degradation can be neglected.

On the other hand, a possible problem with the voltage change on the $V_{\rm AA}$ line is associated with the photodiode reset operation. In case of the "hard reset" where the reset transistor $\rm M_{RS}$ operates in its linear region, a local $V_{\rm RS}$ voltage is sampled on the photodiode capacitance. Thus, the initial photodiode voltages on a row will/may not be identical. In addition, if the $V_{\rm AA\_PIX}$ line is contaminated by noise, that noise is sampled on a photodiode.

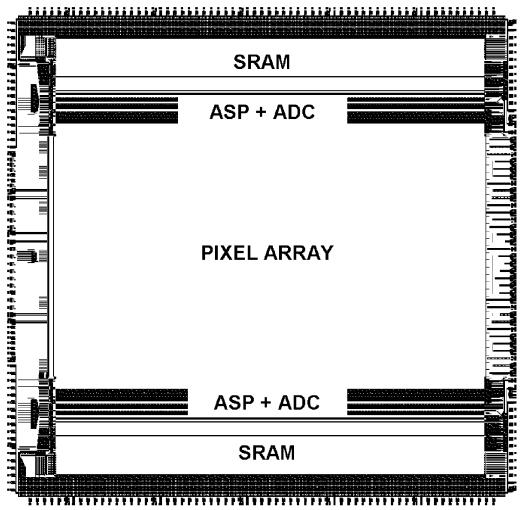

Fig. 5. Chip layout.

These issues associated with the power drop and the ground bounce need to be addressed in designing high-performance large-format CMOS image sensors.

E. I/O Pins and Package

Large spike currents could flow when column parallel circuits have a simultaneous transition from one state to the other, which introduces fluctuations on bias/reference voltages. Among the bias/reference voltages, of biggest concern is the primary reference voltage to the column parallel ADCs and analog $V_{\rm DD}$. In order to stabilize the possible fluctuations on bias/reference voltages, it is preferable that each of several important bias/reference voltages has a multiple number of pads. In addition, placing several decoupling capacitors as close as possible to the bonding pads for the above-mentioned bias/reference voltages could help.

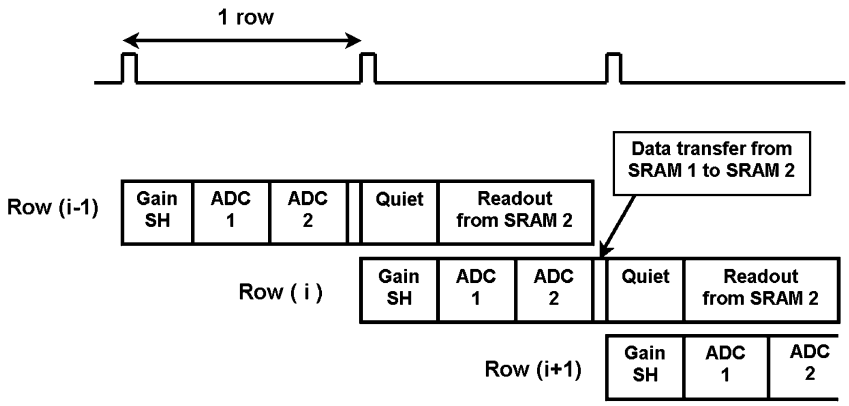

Fig. 6. Operation sequence for row cycles.

III. Implementation

A. Overall Architecture

A UDTV system [7], [8] requires 8.3 million pixels, 60 fps operation in the progressive scanning mode, which translates to approximately 500 MHz pixel readout rate. In order to eliminate the difficulty of handling analog signals with such a wide frequency bandwidth, ADCs are implemented on-chip. The on-chip analog-to-digital (A/D) conversion scheme also offers a possibility of lower power consumption than an analog-output scheme as described in Section II-B. A block diagram of the UDTV sensor and a layout plot are shown in Figs. 4 and 5, respectively. A sensor architecture with column-parallel successive-approximation 10-bit ADCs, column-parallel 2 SRAM banks [9], and 16 parallel output ports was adopted to achieve the high throughput of over 5 Gb/s. The total number of pixels is 3936×2196, with the effective number of pixels being 3840×2160. Although the sensor reported in [9] achieved 9.75 Gb/s, with a 7.0 μm pixel and master clock frequency of 66 MHz, which exceeds the data throughput of 5.2 Gb/s for this UDTV application, the smaller pixel size of 4.2 μm and the larger number of pixels required us to implement several improvements and customization. These include a newly designed smaller pixel, a sufficient number of optical black pixels to obtain precise black level clamp, implementation of a column-gain stage, a shared-ADC scheme with sample-and-hold circuits, operational timing modification for low-noise performance, noise-robust bias circuits, and careful bus routing for high-quality image reproduction. One 10-bit ADC is shared by two columns and the column parallel signal processors are split into two banks, each having 984 ADCs at the top and bottom of the array. This architecture allows the imaging array to be located at the center of the chip.

Fig. 6 shows a row timing diagram. The one row time is approximately 7.5 μs. Following the column-analog gain stage, which is activated at the beginning of a row time, a signal voltage and an offset voltage after the pixel reset are sampled and held ("Gain & SH"). These two samples are used to suppress pixel-wise FPN. The gaining and the sample-and-hold operations are performed in parallel for all columns. No data readout is performed during this period to avoid potential digital noise interference, since this analog processing period is critical to obtain low-noise performance.

Two A/D conversion cycles ("ADC1" and "ADC2") follow in the remaining period since one ADC is shared by two columns as shown in Fig. 4. The digital data is sequentially sampled into the front-end memory SRAM 1 as soon as it is available from the ADC during digitization, and is shifted into the back-end memory SRAM 2 for readout when the digitization is complete. The back-end memory SRAM 2 is read out differentially using on-chip sense-amplifiers to output a digital data stream. This configuration permits the readout of the previous row data during the "ADC" periods. The timing control circuits generate all the required pulses from four input pulses, namely, a master clock, a frame trigger, a row trigger, and a shutter trigger. Several test modes were also implemented.

B. Pixel

The 4.2-μm pixel consists of a deep n-well/p-substrate photodiode with on-chip microlens and three transistors, namely a driver transistor $\mathrm{M_D}$, a reset transistor $\mathrm{M_{RS}}$, and a row select transistor $\mathrm{M_{SEL}}$, as shown in Fig. 3. The fill factor of the photodiode without the microlens is about 40%. In order to obtain high-precision optical black level clamp, optical black pixels with a light shield, consisting of a metal layer and black filter material, are implemented at the periphery of the effective pixel array.

C. Pixel Bias Circuits With Immunity From Power/Ground Noise

In order to avoid the possible shading and noise mixture from power supplies, we have implemented a bias stabilization scheme for the pixel bias voltage and for the bias current of a pixel source follower amplifier, as illustrated in Fig. 7.

As mentioned in Section II, when $V_{\mathrm{AA\_PIX}}$ fluctuates temporary, a photodiode latches the deviation as a temporal noise. It is well known that the noise associated with pixel power supply can be suppressed by using a photodiode soft reset [10], where the reset transistor $\mathrm{M_{RS}}$ operates in its subthreshold region. However, the soft reset has a drawback of image lag that causes a significant problem in high-end video systems. A fill-and-spill operation, where the hard reset and the soft reset are performed sequentially, improves the image-lag but it needs an additional operation for the pixel readout period and makes it difficult to achieve the 60 frames/s over 2000 rows. Accordingly, we chose

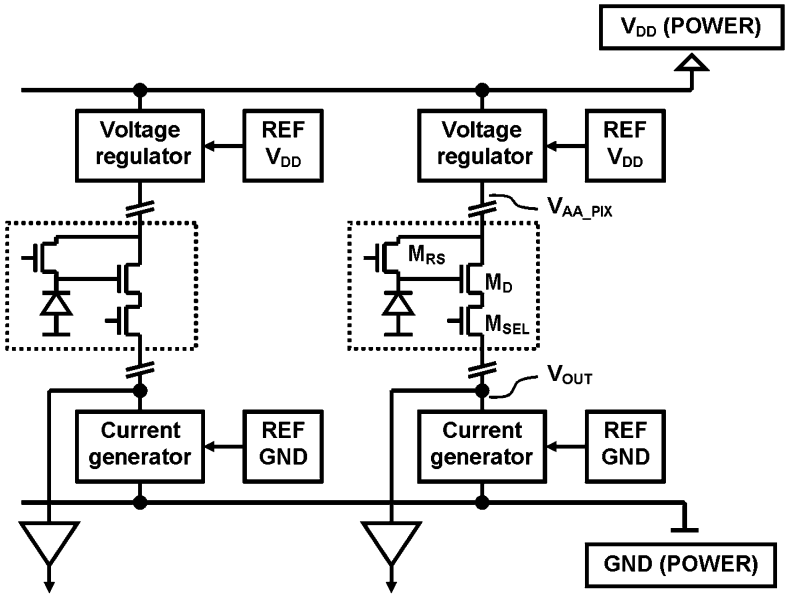

Fig. 7. Block diagram of bias stabilization scheme.

the hard reset operation to realize low image lag and fast pixel operation. It requires a clean pixel power supply voltage and we achieved this with the bias configuration, as shown in Fig. 7.

A voltage regulator is implemented in each column that supplies pixel power voltage $V_{\mathrm{AA\_PIX}}$ that is referenced to a reference voltage $\mathrm{REFV_{DD}}$. The $\mathrm{REFV_{DD}}$ is kept quiet without any use for power supply (no current draw), and thus the voltage regulators can supply a stable and uniform pixel power voltage to each pixel. In order to perform the photodiode hard reset, $V_{\mathrm{AA\_PIX}}$ supplied from the regulator is set to approximately 200 mV lower than $V_{\mathrm{DD}} - V_{\mathrm{TH}}(\mathrm{M_{RS}})$ so that $\mathrm{M_{RS}}$ operates in its linear mode.

A Similar method is also used in a pixel bias current generator configuration. A current generator is implemented in each column. The current generator supplies a bias current referencing to a reference ground REFGND that is isolated from the noisy power GND bus. The pixel bias current is set at 15 μA to drive a large parasitic capacitance on the vertical signal line. Multiplied by the number of column parallel circuits of 1968 in each top and bottom readout block, the total pixel bias current consumed in each block is then 29.5 mA during the pixel readout. The bias current flows through the ground bus line that is more than 16.5 mm (4.2 μm $\times$ 3936) long. When the ground line is grounded at both ends of the array, a voltage increase at the center of the ground bus line is given by

$$\Delta V_{\mathrm{GND}} \sim \rho_{\mathrm{GND}} I_B L_{\mathrm{GND}} / (8 W_{\mathrm{GND}}) \tag{17}$$

where L_{GND} and W_{GND} are the wire length and width of the ground bus line, respectively, ρ_{GND} is the metal sheet resistance, and I_B is the total bias current. With $L_{\mathrm{GND}} = 16.6$ mm, $W_{\mathrm{GND}} = 100$ μm, $I_B = 29.5$ mA, and $\rho_{\mathrm{GND}} = 0.1\ \Omega \cdot$ sq., the peak voltage increase is estimated to be about 60 mV. If the bias current generator refers to the power ground voltage and the common bias voltage V_{LN}, the resulting bias current decreases by 3–6 μA, assuming $\mathrm{g_m}$ for the bias transistor of 50–100 μA/V.

On the other hand, much more uniform bias currents can be obtained by referring to the reference ground (REFGND) as shown in Fig. 7, which means that the proposed scheme is immune from the ground bounce. In addition to the common/power noise rejection and the immunity from spatial voltage deviation, another benefit from the scheme is isolation between columns. Since individual voltage/bias generators are implemented in each column, an identical pixel operation is guaranteed, which avoids a possible noise coupling between columns through common/power nodes.

D. Column Amplifier

Prior to the ADCs, an analog gain stage, which uses a capacitive feedback inverter amplifier with five gain settings $(\times 0.7, \times 1.0, \times 1.3, \times 2.0, \times 4.0)$, is employed. The gain is defined as a total analog gain from the photodiode to the ADC inputs. At the lowest gain of 0.7, an ADC input window of 750 mV covers a full linear output range of the pixel source follower. The individual regulation scheme described in the pixel bias circuit above is also introduced in the column amplifier circuit. Fixed-pattern noise (FPN) generated in each pixel and the column analog signal chain is suppressed before the A/D conversion.

E. Analog-to-Digital Converter

The column parallel ADC is based on a charge redistribution successive approximation (SA) ADC [11], which requires only N conversion steps for N-bit resolution, thus suitable for high-speed operation. A binary-scaled capacitor bank is equipped for signal (consisting of light dependent signal and an offset) and a capacitor which value is close to the sum of the binary-scaled capacitors is equipped for the offset signal. A comparator compares these two values in the successive approximation procedures and generates digital codes. A comparator offset voltage can be suppressed by using a calibration capacitor digital-to-analog converter. The automatic calibration routine is run for

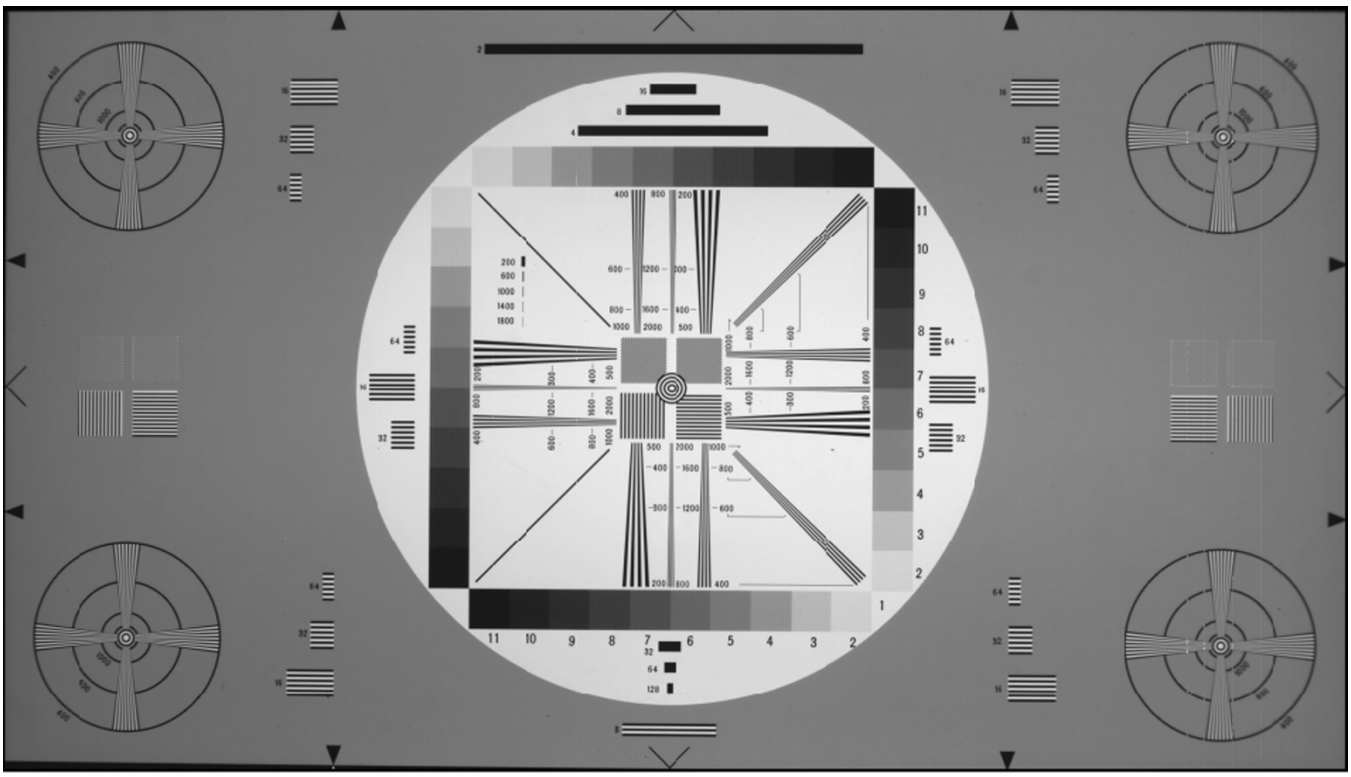

Fig. 8. Full output image.

every frame to compensate for temperature drifting. Calibration values can also be manually written to and read from the ADCs through a dedicated serial interface. Details of the column parallel SA ADC are reported in [9].

In a column parallel A/D conversion, large spike currents could flow at a simultaneous transition of significant bits, for which larger binary-scaled capacitor is switched on or off. Therefore, on-chip decoupling capacitors are implemented for primary reference voltages for the ADCs. Off-chip decoupling capacitors are also used as described in Section II-E.

F. Digital Control

Three digital control signals control the sensor operation, namely, Frame_trigger, Row_trigger, and Shutter_trigger. These signals are fed to an on-chip timing generator, each triggering a frame sequence, a row sequence and electronic rolling shutter timing. The default operation is a 60-fps progressive scan. However, a 30-fps progressive scanning mode is also possible by adjusting the input timing of Frame_trigger and Row_trigger.

IV. PERFORMANCE

A. Sensitivity

At the column analog gain setting of 1.0 and the ADC input window of 750 mV, sensitivity with on-chip microlens is measured to be 4.2 k bits/lux-s (3.0 V/lux·s) using a 2700 K light source and an IR-cut filter of which cut-off wavelength is 650 nm. Conversion gain of 0.06 LSB/e^- is extracted from the photon shot noise measurement, which corresponds to 43 μV/e^- at the pixel electrode. Random noise and dynamic range are measured to be 2.5 $\mathrm{LSB_{rms}}$ and 52 dB, respectively. The random noise is equivalent to noise electrons of 42 e^-.

When analog gain is set at 0.7, random noise is measured to be 1.8 $\mathrm{LSB_{rms}}$ and dynamic range increases to 55 dB, which suggests the noise is determined by the pixel noise. The number of saturation signal charge is 25 000 e^-.

TABLE I
SUMMARY OF NOISE (gain $= 1.0$, 60 fps)

Noise			Value [rms LSB]
Temporal noise			2.46
Fixed pattern noise (FPN)			1.38
	Pixel FPN		0.75
	Row FPN		0.12
	Column FPN		1.15
		4 Column cycle	0.65
		Else	0.95

TABLE II
POWER CONSUMPTION ($V_{DD} = 3.3$ V, 60 fps)

	Value [mW]
Pixel V_{AA}	99
Bias Voltages	3
Analog V_{AA}	165
Digital V_{DD}	264
Interface (at dark)	66
Total	597

B. Noise

Both random noise (RN) and fixed pattern noise (FPN) are measured under dark conditions with the following procedure. First, the random noise component is removed by averaging

TABLE III
SPECIFICATION AND PERFORMANCE OF THE 8.3-M-pixel CMOS APS

Parameter	Value	Comments
Number of total pixels	3936 (H) × 2196 (V)	
Number of effective pixels	3840 (H) × 2160 (V)	8.3 M-pixels; 4 times the HDTV resolution
Pixel size	4.2 μm × 4.2 μm	NW/P-sub photodiode APS with on-chip microlens
Optical format	1.25-inch	Aspect ratio; 16:9
Die size	19.7 mm (H) × 19.1 mm (V)	No stitching is used
Conversion gain	0.06 LSB/electron	Output referred
	43 μV/electrons	at pixel sense node
Full well capacity	25,000 electrons	
Noise floor	42 electrons	
Dynamic range	55.0 dB	
Sensitivity	4200 bits/lux-sec	Output refereed 2700K light source, IR filter with cut-off wavelength of 650 nm
	3.0 V/lux-sec	at ADC input
Scanning	Progressive	
Frame rate	60 fps	
Output signal	10-bit digital 16 parallel output ports	
Output frequency	49.5 MHz	792 MHz (6.3 Gbps) total throughput
Electronic shutter	Electronic rolling shutter	
Process technology	0.25 μm double-poly, triple metal CMOS	
Supply voltage	3.3V	
Power consumption	597 mW	at dark
Package	262 pin PGA	

output data over 32 frames. With this data set, row-random FPN and column-random FPN are calculated by averaging 100 data over the vertical direction and over the horizontal direction, respectively. The pixel random FPN is then extracted by subtracting the row- and column-random FPN from the total FPN value. Due to the readout architecture shown in Fig. 4, two- and four-column cycle FPN were expected to appear. As summarized in Table I, the column random FPN is a dominant FPN component but a 4-column cycle FPN is not found to be significant. Also seen from Table I is that the pixel random FPN is sufficiently suppressed by on-chip FPN suppression circuit. The total FPN is less than the random noise level [13].

Temporal random noise is measured by subtracting the above mentioned FPN data from the original video signal. Since the reset-noise component is estimated to be 35 e^-_{rms}, the results suggest the random noise is dominated by the reset noise. It is confirmed that the effect of the bias stabilization circuits work well as no shading is detected.

C. Power Consumption

Power consumption [13] was measured to be less than 600 mW at dark, including the power consumed by output drivers when the sensor operates at 60 fps in a progressive scanning mode with master clock frequency of 49.5 MHz and 3.3-V supply. Table II summarizes the power consumption of each circuit block. The power consumed by the interface block includes those of input buffers for clocks, a timing generator, in addition to that of output buffers. When the sensor is at dark, it is 66 mW. When the sensor is illuminated, power consumed by the output buffers increases by approximately 200 mW because each data bit toggles more frequently. This value agrees well with (1), with $N_{\rm bit} = 10$ bit $\times 16$ ports, $f_{\rm data} = 32.67$ MHz (which is calculated with the master clock frequency of 49.5 MHz and data output duration ratio of 66%), transition probability $\alpha = 0.25$ and an effective load capacitance of 15 pF for each output.

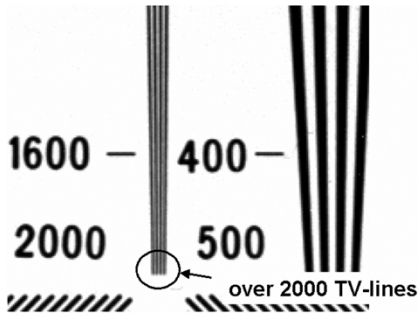

Fig. 9. Magnified image.

D. Reproduced Image

A prototype camera was designed and built to evaluate the 8.3-M-pixel CMOS image sensor. A reproduced image obtained from the 8.3-M-pixel UDTV sensor is shown in Fig. 8. The sensor operated in the progressive scanning mode at 60 fps, with column-amplifier gain of 1.0. No FPN is seen. A magnified image from a center portion is shown in Fig. 9. It is seen that a line spacing of 2000 TV lines is resolved.

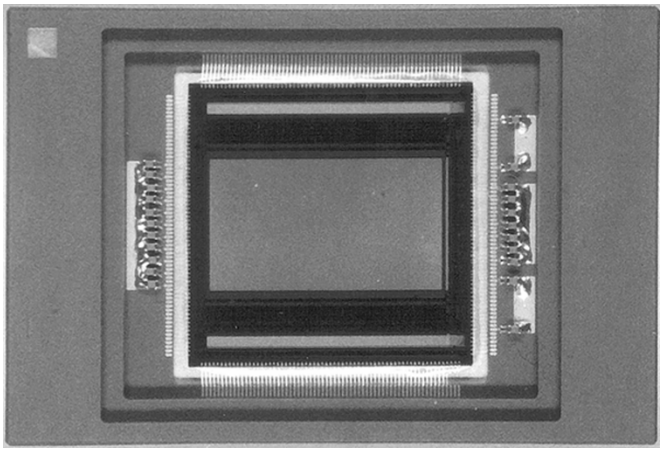

Fig. 10. Photograph of the image sensor in a 262-pin ceramic PGA package.

A photograph of the image sensor sample in a 262-pin ceramic PGA package is shown in Fig. 10. A custom package was designed and built, where several decoupling capacitors can be coupled to the critical bias/reference voltages mentioned in Section II-D at one end of a bonding wire on a bottom plate of the package cavity. This particular sensor sample is without the glass lid and the black filter for demonstration purposes.

Specifications and performance are summarized in Table III.

V. Conclusion

We have developed an 8.3-M-pixel digital-output CMOS APS for UDTV application. It features a small optical format of 1.25-inch, low power consumption of less than 600 mW at dark, while reproducing a low-noise, 60-frames/s progressive scan image. The digital output scheme with a column parallel on-chip ADC architecture permits much lower power consumption than the analog output scheme used in CCD image sensors. This advantage is enhanced as data rate increases. In addition, image quality will be improved in the near future by using a pinned photodiode, which features low read noise and low dark current. This image sensor will pave the way to future digital cinema systems and tele-medicine applications as well as UDTV systems.

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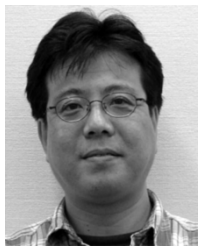

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