Two-dimensional electron gas charge-coupled devices (2DEG-CCDs)

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EXTENDED ABSTRACT[†]

The two-dimensional electron gas charge-coupled device (2DEG-CCD) structure is an outgrowth of recent advances in 2DEG-FET structures for digital logic circuitry and microwave devices. The 2DEG-FET structures, which are known by several acronyms such as HEMT, SDHT, TEGFET, HIGFET, and MODFET, utilize the abrupt heterointerface between two semiconductor materials and consequent conduction band discontinuity to confine electrons [1]. Due to confinement in the direction perpendicular to the interface, the resultant electron distribution is known as a two-dimensional electron gas. Because of the confinement dimensions and the low electron effective mass usually associated with group III-V materials, quantum mechanics plays an important role in broadening the spatial electron distribution and defining allowed energy states. However, quantum effects typically play a minor role in understanding device behavior at temperatures above 77 K. 2DEG-FET devices have several attributes which include very high mobility of the channel charge (typically in excess of 5,000 cm^2/V-sec at room temperature), high transconductance, and low voltage swing requirements.

The 2DEG structure is attractive for CCD applications for several reasons. First, the high low-field mobility and use of a semi-insulating substrate suggest very high speed device operation. Second, the charge-handling capabilty of the 2DEG-CCD structure is large compared with MESFET-type CCDs, and can exceed $1x10^{12}$ carriers/cm^2. Third, the lattice-matched heterointerface has a potentially lower interface trap density than the intrinsically mismatched silicon-silicon dioxide interface, as well as improved radiation hardness. Finally, the useful operating temperature of the 2DEG-CCD is expected to be lower than that of the silicon CCD. Other features of the 2DEG-CCD include fabrication compatibility with high-performance, low noise 2DEG-FET output circuitry and an anti-blooming gate structure.

The 2DEG-CCD differs considerably from MESFET-type GaAs CCDs, which have been shown to operate at frequencies up to 4 GHz with CTE of 0.999 at 1 GHz [2,3]. Unlike the 2DEG-CCD which is a surface-channel device, the MESFET-type CCD utilizes a buried, doped channel for charge confinement and transport. The Schottky gate is typically deposited directly on the GaAs, though an intermediate layer of AlGaAs has been shown to substantially reduce dark current [3,4]. Because of the buried-channel, the MESFET-type GaAs CCD typically has a charge handling capacity of the order of $1x10^{11}$ carriers/cm^2. Impurity and phonon scattering limits the carrier mobility and device speed. At low temperature, 1/f noise due to partial impurity freeze-out can limit device dynamic range.

The first fabricated CCDs which attempted to utilize the 2DEG structure were built at Rockwell [5]. However, the fabricated CCDs exhibited poor charge transfer efficiency at room temperature (0.98 at 6 KHz). Since a capacitive-gate structure with open inter-electrode gaps (1μm size) was used, the CTE would be expected to be non-optimal due to the formation of a potential trough in the inter-electrode gap region of the channel. As described by Milano [6], an improved structure for the 2DEG-CCD would be the resistive-gate configuration [7-9]. In this structure, a thin film resistive layer (e.g. 100 k$\Omega/\square$) is used to cover the entire channel region, and narrow metal electrodes are used to apply biases. The resistive-gate acts as a continuous voltage divider, leading to a continuously varying channel potential for an empty well. This eliminates the open gap problem and speeds charge transfer by inducing a lateral electric field component, as shown in fig. 1.

The first resistive-gate 2DEG-CCD was demonstrated by Song et al. [10]. This device showed a dramatic improvement in performance with a room temperature CTE of 0.999 in the frequency range of 10 MHz - 1 GHz.

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Performance below 10 MHz was limited by dark current caused by gate leakage. This dark current was later reduced by two orders of magnitude through the use of a planar-doped gate dielectric [11,12], thus achieving a CTE of 0.9997 in the frequency range 133 KHz - 1 GHz. In both cases, the upper frequency range was test station limited.

The 2DEG-CCD has a wide variety of applications. At the high frequency end of operation, the device is useful for high data rate transient recording (fast-in, slow-out structures), electro-optical signal processing including filtering, and video signal processing. Despite its appeal for high-frequency application, perhaps the greatest potential for the 2DEG-CCD is as a lower frequency imaging detector array multiplexer [13]. This is because of its higher charge handling capability compared to buried-channel silicon devices (without the interface trap noise associated with MOS surface-channel CCDs), and its compatibility with advanced IR detector materials and structures. When realized in the AlGaAs/GaAs system, monolithic image sensors may be possible using photosensitive multiple quantum well (MQW) layers, heterojunction internal photoemission (HIP) layers, or n-i-p-i layers [14]. When used in a hybridized structure, the multiplexer has a thermal expansion coefficient well matched to that of HgCdTe.

This presentation reviews the structure and operating principles of the 2DEG-CCD. Device design considerations for gate, dielectric, and channel material parameters are presented. The optimization of 2DEG-CCD performance parameters such as well capacity, dark current, and transfer efficiency is then discussed. Experimental results on AlGaAs/GaAs uniform-doped and planar-doped devices, as well as a two-phase device [15] are reviewed.

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