THERMIONIC-FIELD EMISSION IN AlGaAs/GaAs TWO-DIMENSIONAL ELECTRON GAS CHARGE-COUPLED DEVICES

J.-I. Song, D.V. Rossi, S. Xin, W.I. Wang, and E.R. Fossum

Department of Electrical Engineering

Columbia University

New York, NY 10027

ABSTRACT

Dark current in AlGaAs/GaAs two-dimensional electron gas charge-coupled devices (2DEG CCDs) is investigated both theoretically and experimentally. Measurement of the dark current for temperatures in the range 160 K to 360 K was performed and compared with the results of numerical modelling. It is found that thermionic-field emission of electrons from the gate to the channel is the dominant mechanism in uniformly-doped and planar-doped device structures. Good agreement between theory and experiment was obtained.

Metal-semiconductor field-effect transistor (MESFET)-type GaAs charge-coupled devices (CCDs) have demonstrated high charge transfer efficiency (CTE) at frequencies exceeding 1 GHz and are applicable to very high speed analog signal processing[1]. With the advent of new infrared detectors built from III-V materials by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD)[2], the potential integrability of the detector and III-V based CCDs has motivated the investigation of GaAs and related heterostructure CCDs for monolithic imaging detector array readout applications. Two-dimensional electron gas (2DEG) CCDs, an emerging technology, are expected to have several advantages over MESFET-type GaAs CCDs: a higher electron mobility at low electric field and temperature, a larger charge handling capacity, a low insertion loss, a reduced clock swing, and a fabrication compatibility with high speed, low noise 2DEG field-effect transistors (FETs) for output amplifiers and supporting digital circuitry.

Recently, the first resistive-gate (2DEG) CCD on a uniform-doped $Al_{0.3}Ga_{0.7}As/GaAs$ heterostructure was reported[3], and demonstrated high charge transfer efficiency (CTE of 0.9990) for clock frequencies between 13 MHz and 1 GHz at room temperature. Degradation of CTE and reduction of the output signal amplitude were observed for lower frequencies (for example, CTE of 0.98 at 1.5 MHz clock frequency), due to the anomalous accumulation of carriers in the CCD well, referred to as dark current. A thermally activated gate leakage current was believed to be the origin of the dark current since the CTE was improved by cooling the device and subsequent measurement of the gate leakage current showed that the total accumulation of the gate leakage current in the CCD potential well during the period of charge transfer was consistent with the maximum well capacity.

Extension of the low frequency operating range of the 2DEG CCD , which is directly related to the dark current, is important for infrared imaging detector array readout applications to allow long integration periods at low temperature, nominally 65 K. An understanding and reduction of dark current is also important for 2DEG-based dynamic memory devices and circuits. In this paper, reduction of the gate leakage current by more than two orders of magnitude through the use of a planar-doped structure is reported. The physical mechanism responsible for the dark current is shown to be thermionic field emission.

The material structure of the 2DEG CCD consists of, from bottom to top, a semi-insulating GaAs substrate, a GaAs/AlGaAs superlattice buffer, an 8000 Å thick undoped GaAs layer, a 30 Å thick undoped AlGaAs spacer layer, a planar-doped AlGaAs layer (4.5×10^{12} Si atoms/cm^2), a 350 Å thick undoped AlGaAs layer, and a 300 Å thick GaAs cap layer doped with $4 \times 10^{18}/cm^3$ Si atoms. After a 4000 Å deep mesa etch, AuGe ohmic contacts were formed and annealed at 425 C for 45 sec under a forming gas ambient. Using the AuGe ohmic pattern as a mask, the 300 Å GaAs cap layer and 100 Å of the AlGaAs layer were etched with a 1:1:1000, NH_4OH:H_2O_2:H_2O solution. A resistive layer (cermet) was e-beam evaporated on the CCD channel with an equal weight mixture of Cr and SiO powder sources[4], forming a Schottky contact to the underlying AlGaAs layer. The resistive layer was 3000 Å thick with a sheet resistance of 250 kΩ/□ . The first Cr and Au metallization was done by e-beam and thermal evaporations, respectively, to form finger electrodes on the resistive layer and gate electrodes for the output amplifier. The second Cr/Au metallization was used to connect finger electrodes with the same phase (using a 3500Å thick SiO as an inter-layer dielectric).

The CCD delay line is composed of 32 stages with a four-phase clocking scheme

(128 electrodes). The finger electrodes are 1 μm long, 100 μm wide and spaced by 4 μm. A source-follower (1 μm long, 100 μm wide gate) with the same size on-chip load and a dual-gate reset FET were used to read out the signal from the CCD channel.

Before operating the CCD delay line, basic device characterization was performed. The pinch-off voltage and transconductance of a 1 μm gate FET were -1 V and 100 mS/mm, respectively. The gate leakage current of the planar-doped structure was measured to be more than two orders of magnitude lower than that of a uniform-doped structure at room temperature. The CTE of this device is plotted in Fig. 1 in comparison with that of the uniform-doped CCD, which shows an extended low frequency limit by a similar factor as the gate leakage reduction. (Note that the test station limit was 1GHz.) The CTE was evaluated using the method of Brodersen, et al.[5].

To understand the low frequency limit of this device, various mechanisms of gate leakage current were considered and analyzed. It should be noted that in the depletion-mode CCD, electron transport from gate to channel is of concern, whereas in typical enhancement-mode 2DEG FETs, transport from channel to gate dominates gate leakage current. Calculation of thermionic emission (TE) current predicted current levels much lower than experimentally seen, so that other mechanisms such as thermionic-field emission (TFE)[6] or impurity-assisted tunneling were considered. In order to resolve the mechanisms, a numerical calculation was performed to calculate the TFE current. Since the gate leakage current of the CCD channel reaches a saturated maximum when the potential well is empty of signal charge, the modelled structure was assumed to be reverse-biased beyond the pinch-off voltage with the barrier shape shown in Fig. 2. The effective barrier is reduced by increased surface electric field leading to a qualitative understanding as to why the planar-doped structure, with lower surface electric field, has

lower gate leakage current compared to the uniform-doped structure. The tunneling probability for the barrier using the WKB approximation is,

$$T(E_Z) = \exp\{ \frac{-4\pi}{h} \int_{x_1}^{x_2} \{2m^*[qV(x) - E_Z)]\}^{1/2} dx\}, \quad (1)$$

where

$$V(x) = \phi_{Bn} - qN_s x/\epsilon_s - q/16\pi\epsilon_s x \quad (2)$$

and where E_Z is the electron energy associated the momentum normal to the interface, m^* is the tunneling effective mass ($0.080m_o$)[7], ϕ_{Bn} is the Cr/Au Schottky barrier height on $Al_{0.3}Ga_{0.7}As$ (0.935 V)[8], N_S is the planar-doping density ($4.5\times10^{12}/cm^2$) determined from the pinch-off voltage, and ϵ_S is the dielectric constant of $Al_{0.3}Ga_{0.7}As$ ($12.2\epsilon_0$). The TFE current density is,

$$J = \frac{1}{2} \int_0^{\phi_b'} qv_Z(E_Z)T(E_Z) \int_0^{\infty} f(E_Z+E_T) \frac{8\pi m^*[2m^*(E_Z+E_T)]^{1/2}}{h^3} dE_T\, dE_Z , \quad (3)$$

where ϕ_b' is the barrier height modified by the image-force barrier lowering, f(E) is Fermi-Dirac distribution, and E_T is the electron energy associated with the momentum parallel to the interface.

In Fig. 3, the calculated numerical data for TE and TFE currents and measured Cr/Au and cermet Schottky diode leakage currents for temperatures between 160 K and 360 K are shown. The numerical and experimental data are in good agreement within this temperature range, showing thermionic-field emission is likely the dominant mechanism for the gate leakage current. This excludes a possibility of impurity-assisted tunneling that

is related to the material quality and is much more difficult to quantitatively evaluate. Improved agreement can be obtained by adjusting the parameters described above from previously published values, but does not significantly affect our understanding of the phenomena. It is also observed that the cermet diode exhibited more than an order of magnitude less leakage current than that of the Cr/Au diode. Although not yet fully understood, the lower current might be attributed to the reduction of the effective area of the diode since the cermet is believed to be composed of metallic clusters embedded in the dielectric. As can be seen in Fig. 3, the temperature dependence of the TFE gate leakage current is relatively weak, implying that continued efforts at dark current reduction will be necessary to achieve ultra-low dark current at 65 K. One possible avenue of exploration is the use of p-i-n doped gate structure to increase the effective barrier height seen by electrons[9].

In conclusion, thermionic field emission has been identified as the dominant mechanism for dark current in AlGaAs/GaAs 2DEG CCDs, and good agreement was obtained between theory and experiment. Planar-doped device structures exhibit reduced dark current by two orders of magnitude compared to uniform-doped structures due to the reduction in electric field. 2DEG-CCDs fabricated with a planar-doped structure exhibit a concomitant improvement in low frequency operation limits.

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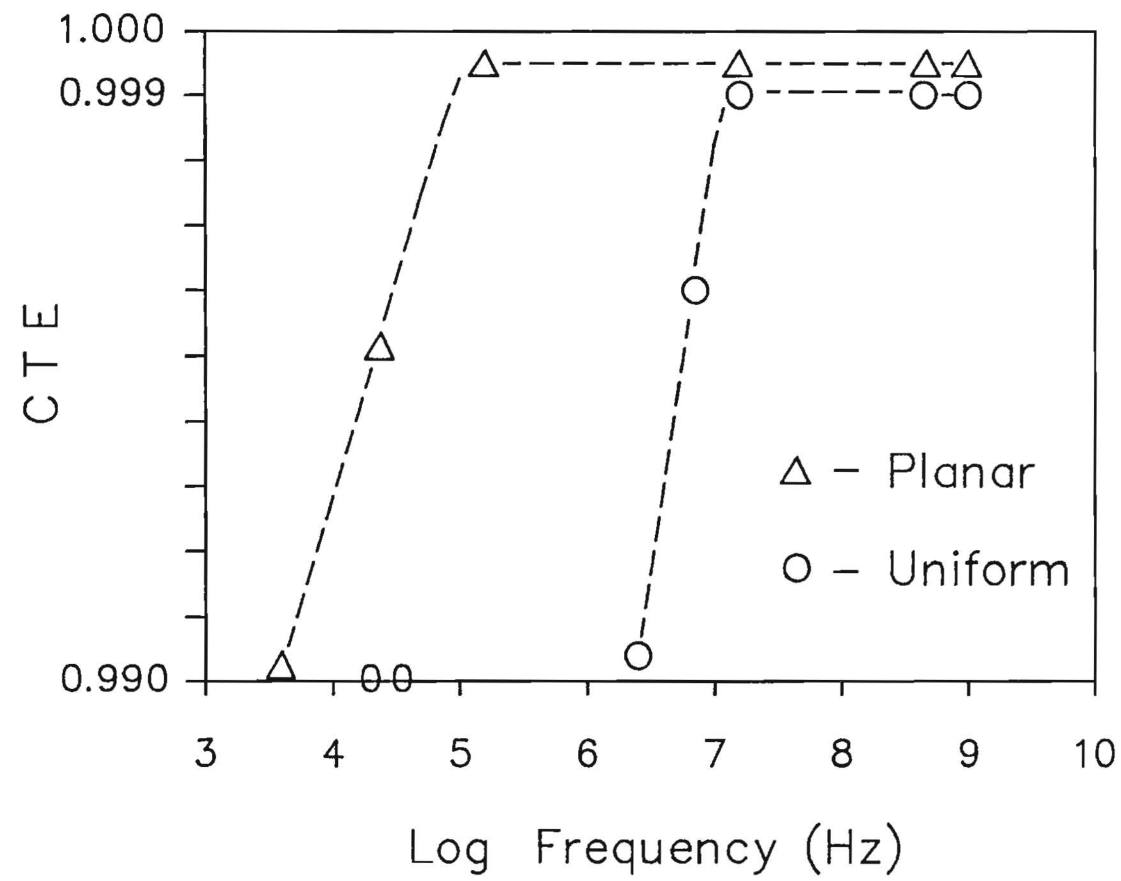
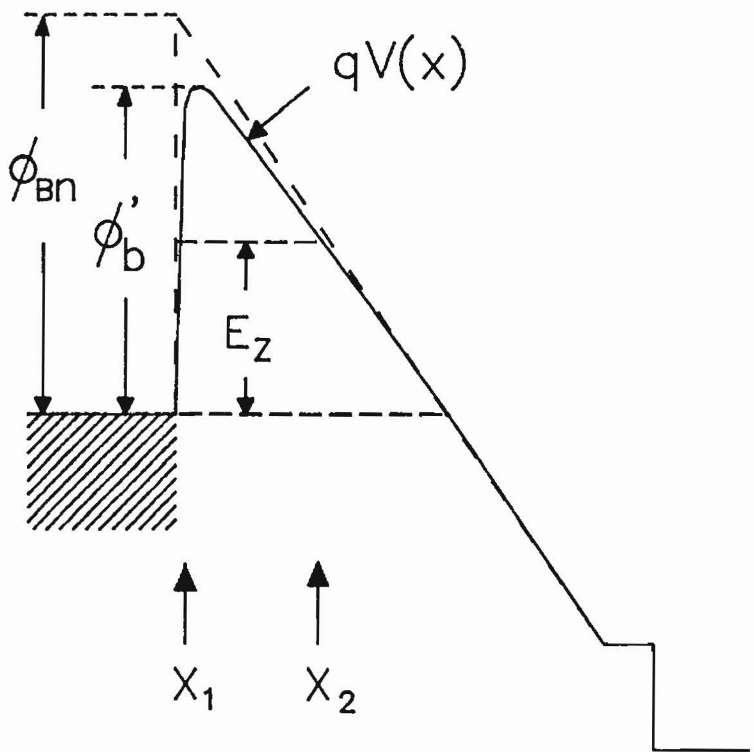
Figure Captions

Fig. 1 Frequency dependence of charge transfer efficiency (CTE) for the resistive-gate planar-doped AlGaAs/GaAs 2DEG CCD (1 GHz clock frequency is the limit of our test station).

Fig. 2 Energy band diagram of a reverse-biased Schottky diode on a planar-doped AlGaAs/GaAs heterostructure used for the numerical model.

Fig. 3 Gate leakage current of the planar-doped AlGaAs/GaAs heterostructure as a function of temperature. Symbols are experimental data points and solid line shows results of thermionic-field emission and thermionic emission calculations.


1.000
0.999
0.990
CTE
3
4
5
6
7
8
9
10
Log Frequency (Hz)
Δ – Planar
O – Uniform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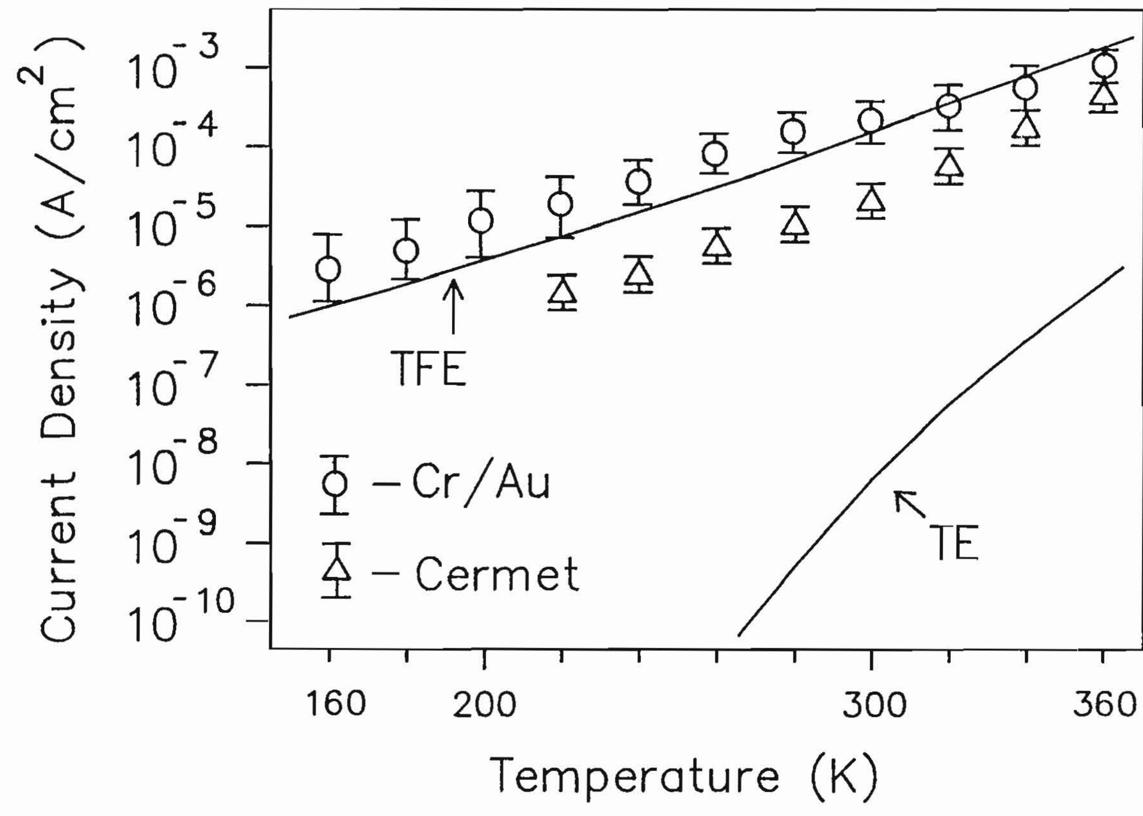
φ'b
qV(x)
Ez
X1
X2


Current Density (A/cm2)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
TFE
TE
– Cr/Au
– Cermet
160
200
300
360
Temperature (K)