Silicon Photodetector Structure for Direct Coupling of Optical Fibers to Integrated Circuits

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Abstract—**A novel detector structure exhibiting real-estate efficient coupling of optical fibers to semiconductor devices is described. The integrated fiber-optic coupler employs vertical insertion of a tapered single-mode fiber into a laser-etched cylindrical hole in the substrate. It features a small surface footprint, mechanical stability, and accurate alignment. Fabricated in silicon, the p-n junction detectors have typically shown responsivities of 0.23 A/W at 0.63 μm, corresponding to a quantum efficiency of 45 percent, and dark currents below 1 nA.**

I. INTRODUCTION

THE USE of optical interconnections between high-speed integrated circuits is viewed as a potential solution to a growing problem in VLSI technology. Conventional metallic conductors, carrying electronic signals from chip to chip, are susceptible to electromagnetic coupling that can result in parasitic capacitance, inductance, and noise pick-up. Overall system performance, particularly at high bit rates, suffers from the limitations thus imposed by the interconnections. Signals transmitted photonically are immune to these effects, and this accounts for much of the current interest in optical interconnections. Potential applications of optical interconnects have been evaluated theoretically; skewless distribution of clock signals and routing of chip-to-chip data links via optical fibers are among those considered promising [1], [2]. These applications would require a means of coupling a large number of fibers to a single semiconductor chip, but no standard technique to satisfactorily perform this function now exists. Techniques employing lens elements [3], a Burrus-type structure [4], or simple butt-coupling [5], which have been used for coupling fibers to discrete optoelectronic components, require too much space to be useful in VLSI interconnection schemes. A recently reported hybrid approach [6], using silicon V-grooves to guide fibers into an integrated 12 × 1 photodiode array, would place restrictions on detector placement as well as presenting assembly and stability problems typically associated with hybridization. The most technically advanced technique reported to date employs a horizontal fiber terminating in an angled mirrored facet that reflects incoming light down onto the semiconductor substrate [7]. However, use of a multimode fiber requires a large-area detector, and the lateral approach consumes considerable on-chip real estate, limiting the number of fibers that may be coupled to a single IC chip.

To address the problem of real-estate consumption by optical interconnects, we have been investigating a new device structure, the integrated fiber-optic coupler (IFOC). The basic concept and preliminary characterization of a prototype device have been presented earlier [8]. In this paper, techniques used to routinely fabricate and evaluate the novel coupling structure are reported. Emphasis is placed on processes unique to the fabrication and characterization of this device structure, rather than on the performance of devices in this first design iteration. Appropriate patterns on pre-existing photolithographic masks were used for device definition in order to expedite demonstration of the viability of the IFOC structure as a component technology. Accordingly, optimization of certain parameters critical to high-speed photoreceiver applications was left to the next design iteration. Design changes to be implemented, including those facilitating extension of the proven techniques to GaAs circuitry, are discussed in Section III of this paper.

In the IFOC structure, the tapered tip of a single-mode fiber is inserted vertically into a cylindrical hole etched in the semiconductor. The inner surface of the hole is doped to form a p-n junction photodetector. A schematic cross section of the IFOC detector is shown in Fig. 1. The small diameter of the hole (15–18 μm) and the minimal thickness of excess fiber cladding allow for a receiver that occupies less space than previously demonstrated fiber-optic interconnect designs. The real-estate reserved for the detector need not substantially exceed the diameter of a single-mode core, while the remainder of the fiber's footprint may be utilized by additional circuitry. This includes elements for amplification of the input signal, as well as those engaged in subsequent signal processing or logic functions. Such a reduction in the detector area allows for the highest possible packing density of optical interconnects.

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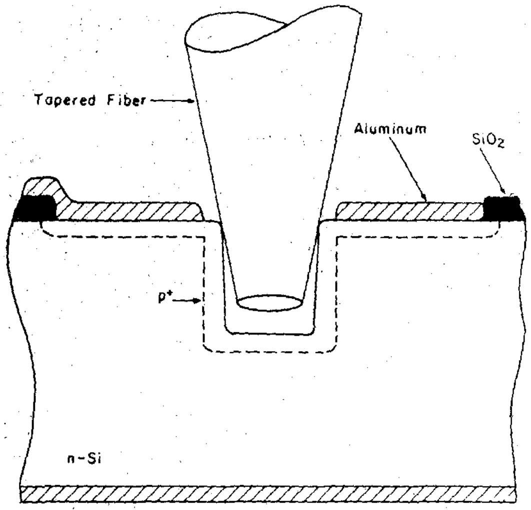


Fig. 1. Schematic cross section of IFOC photodetector.

II. Device Fabrication

The fabrication of the IFOC device proceeds in two distinct stages: the formation of the detector, and the preparation and insertion of the optical fiber. In the first stage, a 10-Ω · cm n-type silicon wafer with (100) orientation is cleaned and oxidized in steam at 900°C. Photolithography is performed to define alignment marks in the substrate and to open windows for the etching of the detector cavities, which is done using a nonthermal laser-induced wet etching technique [9]. Typically, the silicon substrate is covered with a dilute HF solution (10 percent by volume in DI water) and a continuous-wave UV beam is focused onto the substrate at the desired location. The UV beam is obtained from a frequency-doubled argon-ion laser yielding a 257-nm line. The power density of the illuminating spot determines the etch rate, and the spot size determines the final hole diameter, which is between 15 and 18 μm for the work described here. A 20-min etch at a power density of 10 W/cm^2 is used to form the 20–25-μm-deep cylindrical holes that serve as coupling sites in the IFOC structure. The technique allows for holes of any depth to be drilled while maintaining vertical sidewalls with no significant variation in diameter, since light-guiding within the cavity for deep UV wavelengths results in a highly anisotropic etch. This characteristic, as well as the nonthermal damage-free nature of the process, makes the laser-assisted etching technique most advisable for the creation of cavities that will serve as active circuit elements. Laser radiation can also be used to thermally etch holes, but damage induced on the surrounding area is considerable and undesirable. Adverse effects arising from substrate damage, such as increased dark current and trap-related noise, were major considerations in ruling out the use of reactive ion etching for detector cavity formation. Anisotropic wet etching techniques, which yield crystallographically defined vertical-walled trenches in (110) oriented substrates [10], were found to be unsuitable for applications requiring three-dimensional features with more than one set of vertical walls [11]. Although the laser-assisted etching process is currently performed serially, its throughput can be increased by switching to a projection etching process using an excimer laser [12].

After etching, the remaining oxide is stripped and a 5000-Å-thick field oxide is grown in steam at 900°C. A diffusion window centered on the etched hole is opened and dopant is introduced by one of two techniques. One alternative involves the use of a boron-containing polymer spin-on film to dope the exposed silicon, including the inner surface of the hole. An analysis of spin-on doping of similar structures [13] indicates that predeposition is assisted by capillary action for holes with an aspect ratio of less than five, as used in the IFOC. However, to experimentally determine whether gas-phase predeposition of dopant might be better suited to the cavity geometry, the use of a solid diffusion source was also investigated. Reproducible and consistent results were obtained with both techniques, and they are considered to be equally viable for this application. Following predeposition, a 110-min impurity drive-in is performed at approximately 1000°C in an open-tube furnace with a 95-percent N_2/5-percent O_2 gas mixture flowing.

Following the diffusion of the detector cavity, a contact window is opened and 3000 Å of aluminum is evaporated and patterned photolithographically. The most important aspect of this step is the removal (by a standard wet etch) of all aluminum from the cavity's interior, decreasing optical loss due to reflections. Finally, a backside aluminum contact is evaporated, followed by a 12-min forming gas anneal at 400°C. As the above description implies, IFOC device fabrication is compatible with standard integrated-circuit processing. We have recently fabricated a charge-coupled device test chip configured to accept both electronic and fiber-optic inputs. Ongoing tests indicate that the inclusion of IFOC sites has no detrimental effect on adjacent circuitry.

The second stage of fabrication begins with the preparation of the optical fiber. The tip of a single-mode Corning fiber with a core diameter of 9 μm and a cladding outer diameter of 125 μm is tapered to approximately 12 μm in a continuously stirred solution of HF buffered with ammonium fluoride. In order to obtain the desired profile, a portion of the fiber's plastic jacket (which resists the HF etch) is removed, and then the length of exposed glass is reduced to about 40 μm using a straight-pull scribe and break technique [14]. Inhibited transport of etchant inside the jacket results in a conically tapered profile with a half-angle of 12–15 degrees. Since the distance that must be etched radially (55 μm) is greater than the length of exposed glass, the tip lies within the protective jacket at the conclusion of the 3-h etch. This facilitates safe storage of the batch-fabricated fibers prior to the final assembly of the device. The final assembly step involves mechanically stripping back the jacket, carefully inserting the fiber into the detector cavity, and fixing it with respect to the microcircuit package that houses the IFOC chip. The insertion process is performed on a dedicated work station, which is drawn schematically in Fig. 2.

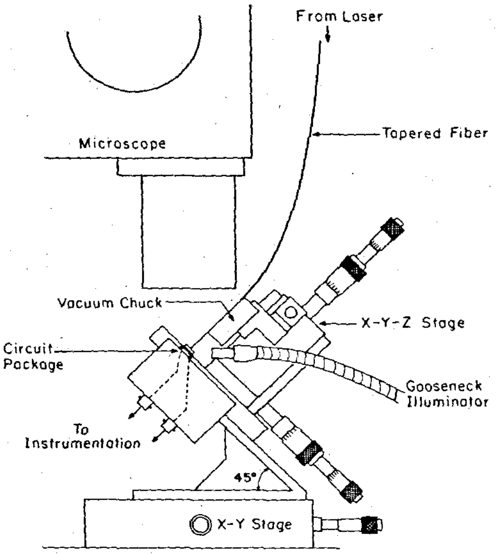
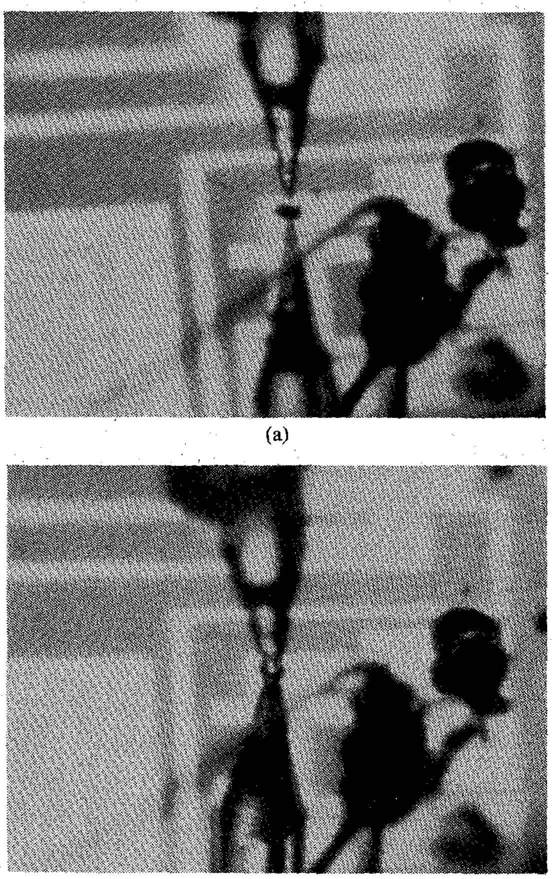


Fig. 2. Schematic diagram of the work station used for fiber insertion.

The insertion station consists of a mount for the circuit package, an *X-Y-Z* translational stage with a vacuum chuck fitting to hold the optical fiber, and an Olympus SZH microscope that gives reasonable magnification while maintaining a long focal length for maximum working distance. The microscope is angled 45 degrees from both the fiber and the chip, affording a clear view to aid the operator in achieving proper mechanical mating. Electrical connection is made to the photodiode through the mounting box, and live photocurrent monitoring supplements visual observation in the determination of the best final resting position for the fiber. Fig. 3 shows the photographs taken through the microscope during the insertion process. Following insertion, the fiber tip remains in place despite small movements of the vacuum chuck, indicating the lateral alignment stability provided by the etched hole.

To prevent stress on the taper, a UV-cured adhesive is used to affix the fiber to the edge of a glass slide bonded onto the microcircuit package. This is done at a point approximately 300 μm above the chip surface, where both the cladding and the protective jacket of the fiber are still intact. No adhesive is needed at the surface of the chip, as in other fiber-optic coupler designs [4]–[7] because the detector cavity itself prevents any lateral misalignment. The package configuration is stable enough that no fiber has yet pulled out of a detector cavity during testing once it has been bonded to the slide. Adhesion at the fiber-slide joint and physical mating between the vertically inserted fiber and the cavity combine to ensure a stable well-aligned structure. This reveals one advantage inherent in the use of vertical coupling structures for optical interconnect applications. Furthermore, as the level of integration in VLSI circuitry increases, Rent's rule [1] predicts that the required number of interconnections will outpace the availability of connection sites on the chip periphery. This "pinout problem" is best addressed by providing interconnection sites in the chip's interior; the vertical structure of the IFOC makes such an approach possible. A photograph demonstrating this appears in Fig. 4. The fiber-to-fiber spacing of ~1.5 mm seen there is determined by the pre-existing chip layout. Simulations of the packaging process, involving the insertion and bonding of tapered fibers into holes etched in unprocessed silicon chips, have achieved fiber spacings as low as 300


(a)

(b)

Fig. 3. (a) Photograph of fiber positioned above detector cavity, just prior to insertion. (b) Photograph of final physical structure at the IFOC site. A reflection from the chip's surface and a conventional wire bond can be seen in each of the photographs.

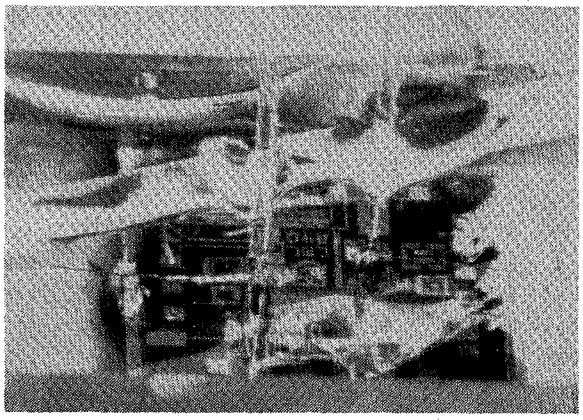


Fig. 4. Photograph of packaged device accomodating two IFOC inputs to the interior of an IC chip.

μm, limited primarily by the bulky adhesive layer applied to the edge of the glass slide. It is likely that more sophisticated packaging techniques will permit IFOC arrays with center-to-center spacing nearly as small as the outer cladding diameter of the fibers used.

III. DEVICE CHARACTERIZATION AND DISCUSSION

Electrical characterization of the photodetectors included measurement of series resistance, capacitance, and dark current, both before and after device packaging. Information concerning the quality of the fabrication process, particularly the effects of steps unique to the process, can be obtained from this data, which is also gathered for test structures on adjacent sites. The average value for sheet resistance measured on diffused test sites was 25 Ω/□, predicting a series resistance for the IFOC photodiode geometry of $R_s = 25\ \Omega$. This is in accord with experimental values of 50–80 Ω for fabricated devices, if contact resistance effects are included. The capacitance and dark current of the reverse-biased photodiodes are recorded in a sweep from 0 to −10 V. Typically, a junction capacitance of 10 pF at −5 V was noted for unpackaged diodes, with an additional 2–3 pF due to bond wires and instrumentation interfaces seen after packaging.

Measurement of the dark current of IFOC photodiodes and comparison with that of adjacent test diodes provided the primary quality control data for the overall process. Devices exhibiting soft low-voltage breakdown (V_B = 3–10 V) or dark current greater than an arbitrary cutoff value (2 nA at −10 V) were considered failures, and they comprised about half of the fabricated IFOC's. This was only slightly greater than the "failure" rate of planar test diodes. The difference is believed to be due primarily to the greater difficulties of removing chemical contaminants from the inside of the etched holes. Several fabrication runs employing especially thorough cleaning processes yielded devices with a reduced incidence of failure. On occasion, increases in the photodiode dark current were observed while monitoring the device's I–V characteristic during the fiber insertion process. This effect appeared in very few instances, and generally in conjunction with breakage of the tapered fiber tip inside the cavity. Occurrences of this sort are easily detected and avoided, and couplers with properly seated fibers show no dark current anomalies. However, such effects should be carefully monitored during long-term device operation. Overall, it was normal processing considerations, rather than those related to IFOC fabrication, that set the limits on device performance and yield.

From the average values of series resistance (R_s) and junction capacitance (C_j) obtained, a diode cutoff frequency $f_t = (2\pi R_s C_j)^{-1} = 200$ MHz could be inferred. This would be realized in a p-i-n diode with these parameters, but the lag in response due to carrier diffusion delays in the current p-n structure further limit the operating speed. Fig. 5 shows the response of the IFOC detector to an input 825-nm light pulse. At this wavelength, the absorption depth in silicon (~15 μm) is much greater than the width of the depletion region; the lag in carrier collection accounts for the 125-ns rise and fall times observed. Since high-speed performance of the devices in the next design iteration should be RC limited, it is important to determine the extent to which these values may be reduced. A decrease in capacitance by a factor of ten can be achieved without altering the basic IFOC design, simply by eliminating most of the excess p-n junction area surrounding the cavity. Additionally, a reduction in series resistance is expected to result from more comprehensive design alterations now being implemented. The relatively large value of R_s can be attributed to the unique geometry of the photodiode, which requires carriers generated at the bottom of the hole to drift the entire length of the cavity sidewalls before being collected at the upper contact. A structure allowing for ohmic contact to more of the active region would reduce R_s, but it must be configured so as to minimize optical loss due to reflections. A backside-illuminated photodetector structure that satisfies these criteria is currently under investigation, and will be described below.

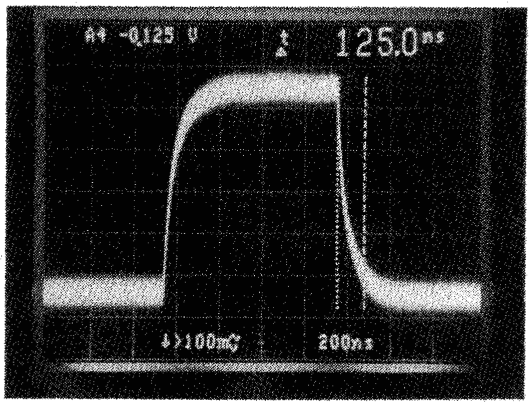


Fig. 5. Oscilloscope trace of the IFOC photodiode's response to a modulated 825-nm optical input.

Characterization of the dc optoelectronic performance of the coupler was undertaken with CW He-Ne and GaAs lasers acting as optical sources at 633 and 825 nm, respectively. Several sets of responsivity data were collected and compared. First, the photocurrent generated by a free-space He-Ne laser beam incident perpendicularly on the surface of the detector was recorded. A slight reconfiguration of the insertion station facilitated the measurement, which involved focusing the laser beam to a 10-μm spot and scanning across the diffused region of the photodetector chip just prior to insertion of the fiber. Following the insertion and bonding of the fiber, the photocurrent was measured relative to the optical power launched into the inserted fiber. This yields a net responsivity that lumps any loss of photons due to the tapered fiber geometry and the coupling scheme together with the loss of optically generated carriers due to recombination in the semiconductor, and is more meaningful to the characterization of the IFOC as an optoelectronic component. The measurement of net responsivity was performed at both of the available laser wavelengths to gauge the effect of the spectral dependence of the absorption coefficient.

The measurement employing the free-space beam served to spatially profile the diode responsivity and to obtain values independent of any optical losses from the fiber. The observed spatial uniformity of the photogenerated current, including instances in which the laser spot is focused entirely within the cavity, provided further confirmation of the success of the detector doping processes. The average value of responsivity recorded in these measurements was 0.23 A/W, corresponding to a quantum efficiency of 45 percent for $\lambda = 633$ nm.

In the measurements of net dc responsivity at 633 nm, the He-Ne laser beam was coupled into a single-mode fiber that was spliced to the tapered IFOC fiber using a low-loss GTE laboratory splice. A curve tracer was used to monitor the *I-V* characteristic of the photodiode under illumination and in the dark. The difference between the two curves is the photogenerated current I_{ph}, which was recorded at a 5-V reverse bias. A sample datum is shown in Fig. 6. For the experiments at 825 nm (including the aforementioned response time measurements), a commercial GaAs diode laser with a multimode fiber pigtail was employed. In this case the splice to the tapered single-mode fiber introduces considerable loss (~ 16 dB). Because of the small signal level, a picoammeter in series with the photodiode is used to measure I_{ph}. At both wavelengths, measurements of optical power were made with a single-mode reference fiber substituted for the tapered fiber, in order to evaluate the precise loss due to splicing and estimate the power launched into the IFOC coupler. The average responsivity values obtained at 633 and 825 nm were 0.21 and 0.10 A/W, respectively. The reduction at the higher wavelength is due to the loss of diffusing carriers generated deep within the substrate. Within the experimental uncertainty, agreement between the two $\lambda = 633$ nm measurements indicates that the coupling scheme introduces no significant optical loss.

A separate investigation of possible optical losses arising from the fiber etch was also undertaken: microscope inspection of both overetched and properly etched tips of fibers carrying approximately 1 mW of He-Ne laser light shows that tapering can be controlled so that no appreciable radiation is emitted from the sides of the fiber. For the current IFOC device, in which the cavity's sidewalls are part of the photodetector, this is not a critical feature; however, it is necessary for the successful implementation of backside-illuminated detector designs. Such designs employ a cavity etched from the backside of the wafer through to within several micrometers of the front surface, where the photodiode is fabricated as part of a routine processing sequence.

A laser-assisted technique for etching high aspect ratio holes in GaAs has been developed [15], and fabrication of IFOC devices in this material is under investigation. Because of the larger absorption coefficient, detectors based in GaAs will exhibit improved response time and quantum efficiency. Furthermore, in backside structures utilizing semi-insulating substrates, such as Cr-doped GaAs, crosstalk between adjacent elements can be sharply reduced by the common technique of mesa etching. These structures would also allow improvements in high-speed performance due to reductions in R_s and the possibility for detector configurations with transit-time limited ac response. Recent work demonstrating the fabrication of GaAs optical devices on silicon substrates containing electronic devices [16], [17] suggests that IFOC devices fabricated in both materials will find applications.

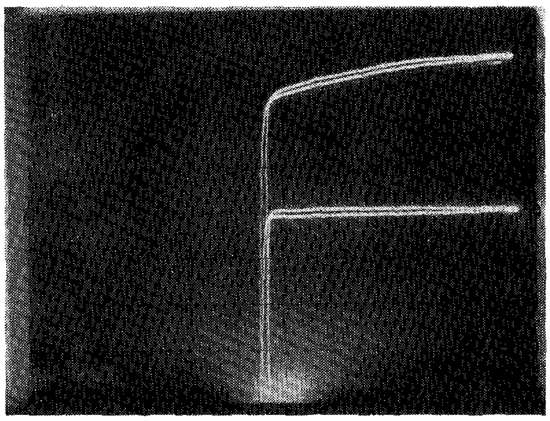


Fig. 6. Photograph of dark and illuminated *I-V* characteristics used to determine net dc responsivity to 633-nm optical signal. Horizontal and vertical axes represent 1 V and 2 μA per division, respectively, and the input optical power is 25 μW. Hysterisis is due to capacitance in the external leads of the curve tracer.

IV. SUMMARY

The integrated fiber-optic coupler, a novel structure that facilitates reliable high-density coupling of optical fibers to integrated circuits, has been described. It features vertical insertion of a tapered single-mode fiber into a laser-etched cavity 15 to 18 μm in diameter, and represents the most real-estate-efficient coupling technique for optical interconnections yet reported. The simple device fabrication sequence is compatible with standard silicon IC processes, and results in good quality photodiodes, as evidenced by the 45-percent quantum efficiency and low dark current (10^{-6} A/cm^2). Minor variations of the techniques described above can be applied to GaAs, offering the potential for fiber-optic interfaces to both sources and detectors on the same substrate using the IFOC technique.

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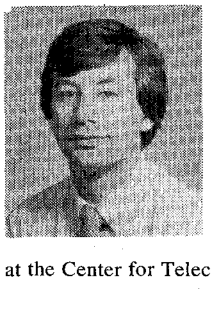

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A. H. Amirfazli, photograph and biography not available at the time of publication.

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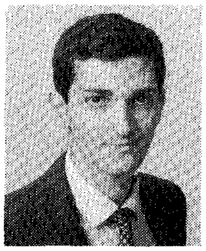

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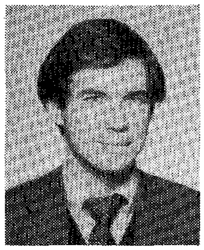

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