Radiation-Induced Dark Signal in 0.5-Micron CMOS APS Image Sensors

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1. ABSTRACT

A CMOS APS image sensor test chip, which was designed employing the physical design techniques of enclosed geometry and guard rings and fabricated in a 0.5-μm CMOS process, underwent a Co^{60} γ-ray irradiation experiment. The experiment demonstrated that implementing the physical design techniques of enclosed geometry and guard rings in CMOS APS image sensors is possible. It verified that employing these design techniques does not represent a fundamental impediment for the functionality and performance of CMOS APS image sensors. It further proved that CMOS APS image sensors that employ these physical design techniques yield better dark signal performance in ionizing radiation environment than their counterpart that do not employ those physical design techniques. For one of the different pixel designs that were included in the test chip pixel array, the pre-radiation average dark signal was approximately 1.92 mV/s. At the highest total ionizing radiation dose level used in the experiment (approximately 88 Krad (Si)), average dark signal increased to approximately 36.35 mV/s. After annealing for 168 hours at 100°C, it dropped to approximately 3.87 mV/s.

2. INTRODUCTION

There has been a growing interest in radiation hard CMOS Active Pixel Sensor (APS) image sensors. This is evident by the recent publication of research work in this area [1, 2, and 3]. The three major and consequential effects of ionizing radiation on standard CMOS devices are shift of threshold voltages, current leakage in NMOS transistors, and N-channel inter-transistor (isolation field) current leakage. The physical design technique of *enclosed geometry* (or *edge-less* transistors) proved to be very effective for significantly reducing current leakage in NMOS transistors [4]. The N-channel inter-transistor (isolation field) current leakage was substantially curtailed employing the physical design technique of P-channel *guard rings* [5]. Employing design techniques to enhance the radiation tolerance of integrated circuits, *hardness-by-design* [6], is gaining more acceptance because of the strong economic case that it presents.

The magnitude of radiation induced threshold voltage shift is proportional to the number of holes created (and trapped) in the gate oxide due to ionizing radiation. The number of holes created in the gate oxide by ionizing radiation is proportional to its thickness (volume). Therefore, the magnitude of radiation induced threshold voltage shift is smaller for less thick oxides. For particularly thin oxides (less than 12 nm thick), the radiation induced holes in the gate oxide have a much better chance to tunnel out of the oxide (requiring only 6 nm effective tunneling distance) before their conversion to interface states. Radiation-induced threshold voltage shift for both N- and P-channel transistors was experimentally found to get considerably smaller when the gate oxide is less than 12 nm thick [7].

It was concluded that employing the physical design techniques of enclosed geometry and guard rings in a standard CMOS technology that has a gate oxide thickness of 12 nm or less will significantly enhance the radiation tolerance of CMOS APS image sensors. A CMOS APS image sensor test chip was designed employing the physical design techniques of enclosed geometry and guard rings. The process used to fabricate the test chip is a 0.5-μm CMOS process. It is a triple-metal layer, double-polysilicon layer process. The process has a gate oxide thickness of approximately 11.5 nm.

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The paper has three main sections. In the first one, the description of the test chip is presented. In the second section, the irradiation experiment setup is described. The experimental results are presented in the third section, which is followed by a section of discussion and conclusions.

3. DESCRIPTION OF TEST CHIP

The physical design techniques of enclosed geometry and P-channel guard rings were used to design a set of radiation hard photodiode pixels. This design effort yielded a set of eight pixels. Employing the physical design techniques of enclosed geometry and P-channel guard rings yielded a geometrical fill factor of approximately 30% for a *baseline* square pixel with a 21-µm pitch. The geometrical fill factor is defined as the ratio of the area of the photodiode to the total area of the pixel. It should be noted that the effective fill factor is higher than the geometrical fill factor. The reason behind that is that the part of pixel surrounding the photodiode is not entirely photo-insensitive. This means that photons incident on the pixel but outside the photodiode area may be absorbed, leading to the generation of photo-electrons. These electrons diffuse, and some of them may reach the photodiode area, which is the collection node. This mechanism is usually referred to as *lateral diffusion*. Those electrons that reach the collection node contribute to the output signal. The increase of the output signal due to the absorption of photons incident outside the photodiode area makes the effective fill factor higher than the geometrical fill factor.

To realize the same geometrical fill factor (approximately 30%) without having to use the physical design techniques of enclosed geometry and P-channel guard rings, the pixel pitch would have been approximately 14 µm. Thus, the penalty of radiation hardening the pixel was to increase the pixel pitch from 14 µm to 21 µm, an approximately 2-fold increase in silicon real estate. It should be noted that the layout was extended to 28-µm square pixel pitch such that it fits within the frame of an existing design. If the geometrical fill factor of the baseline pixel was to be calculated based on the total area (28 µm X 28 µm), it would be approximately 17%. The eight pixels differ in several design aspects such as photodiode area, photodiode shape, location of photodiode guard ring, and symmetry. Hence, they have different geometrical fill factors.

The eight pixel designs were compiled into an array. The array size is 256 X 256, constituting an imaging area of approximately 7.2 mm X 7.2 mm. The 256 X 256 array was divided into eight sub-arrays, each is 64 X 128. Each of the eight sub-arrays has only one of the eight pixel designs.

The periphery circuits were then integrated around the pixel array. The main periphery circuits are row and column decoders, row buffers, and an analog circuit processor. The row and column decoders are similar and are used to select the particular row(s) and column(s) of the array that are under consideration at a given time. The windowing function, and the electronic pan and tilt functions can be realized by manipulating the digital inputs of those decoders. The row buffers are used to drive the pixel control signals, such as reset and row select, to the pixels across the array. The analog signal processor is used to sample-and-hold and drive the output signal voltage level (illuminated level) and the output voltage reset level (dark level) off chip. Correlated-double-sampling (CDS), albeit it is only pseudo CDS, can be realized off chip by taking the difference between those two voltage levels. It should be noted that the periphery circuits were not designed to be radiation hard. The test chip is intended to test only the radiation hard pixels. The periphery circuits are to be shielded when the chip is irradiated.

The full chip was verified using Design Rule Checking (DRC) and Layout versus Schematic (LVS) techniques. The database was transmitted to a mask house for a mask set generation and then fabrication. The process used to fabricate the chip is a 0.5-µm CMOS process. It is a triple-metal layer, double-polysilicon layer process. The inclusion of a second polysilicon layer is significant as it permits the implementation of linear capacitors employing polysilicon layer to polysilicon layer capacitors. The process has a gate oxide thickness of approximately 11.5 nm.

The complete physical design of the radiation hard CMOS APS image sensor test chip (with the pixel core removed) is shown in Fig. 1. The total size of the die is approximately 8.7 mm X 8.2 mm. The total number of the I/O pads is 78. A photograph of the test chip attached to the package and wire bonded is shown in Fig. 2. A laboratory bench-top camera board was developed for the test chip. An image taken by that camera board is shown in Fig. 3.

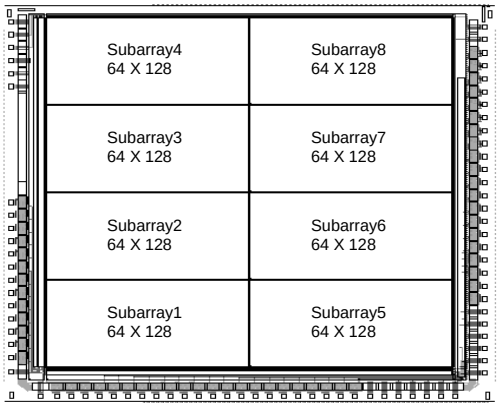

Fig. 1 The complete physical design (the pixel core removed).

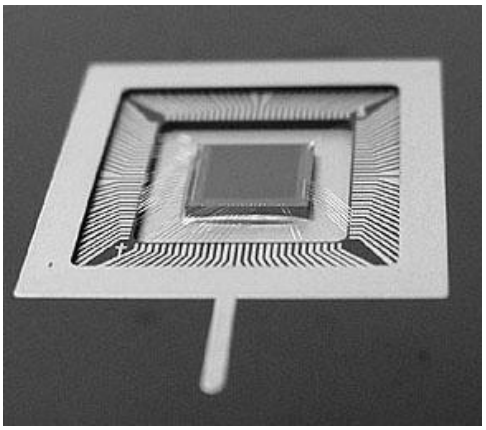

Fig. 2 A photograph of the chip in its package.

Fig. 3 An image taken by the camera board utilizing the test chip.

4. IRRADIATION EXPERIMENT SETUP

The irradiation of the test chip was successfully performed at Space Electronics Inc., in San Diego, California, USA. The source used was Co^{60} γ-ray radiation source. The *MIL-STD-883E, Method 1019.5*, Ionizing Radiation (Total Dose) test standard was followed. The software and hardware of the radiation hard camera board system were modified for more automated image data acquisition. Each set of test devices had one control device, which was not irradiated and its measurement results were used to calibrate for any change in testing conditions. The captured images were saved as raw data during measurement. Another piece of software was used to analyze the data.

As described in the previous section, the pixel array was the only part of the image sensor test chip that was designed employing radiation hardening design techniques. These techniques were not applied to the periphery circuits and the I/O pads. Hence, *two irradiation strategies* were adopted. The first one was to protect the periphery circuits and I/O pads by way of shielding, and expose only the pixel array to radiation. This strategy has the disadvantages that the test setup is somewhat cumbersome and that the radiation level across the pixel array is less uniform (that it would have been if there was no need for shielding the periphery circuits and the I/O pads). However, this strategy has the advantage that total dose in the experiment can be relatively high, thus making the experiment more useful in assessing the effectiveness of the employed radiation hardening design techniques. The second strategy was to expose the entire chip to radiation (thus eliminating the need for the cumbersome shielding setup, making the radiation level across the pixel array more uniform), and keep the total dose relatively low.

To implement the first irradiation strategy, rectangular grooves (each is approximately 6.5-mm wide and 3.25-mm deep) were cut into lead bricks. A schematic illustration (not to scale) of a grooved lead brick is shown in Fig. 4. The lead bricks used were standard lead bricks with a 2”-height, 4’’-width, and 8”-length. When two grooved lead bricks are put together such that two grooves are facing each other, a lead block (4” X 4” X 8”) with square openings (windows) is formed. The size of each window was approximately 6.5 mm X 6.5 mm, slightly smaller than the size of the pixel array. The lead block with a square window provided for the collimation of the γ-rays that is needed to irradiate the image sensor pixel array, but not the periphery circuits and the I/O pads. The surfaces of the lead bricks facing each other to form the lead block were machined smooth to minimize the radiation leakage through the minimal space formed when they were put together. The effectiveness of the shielding provided by this setup was verified by measuring the radiation dose rate at the faceplate of the pixel array, and at areas of the chip that surrounds the pixel array. The setup was optimized (through two iterations) such that the dose rate at the areas of the test chip that surrounds the pixel array is less than 1% of the radiation dose rate at the pixel array.

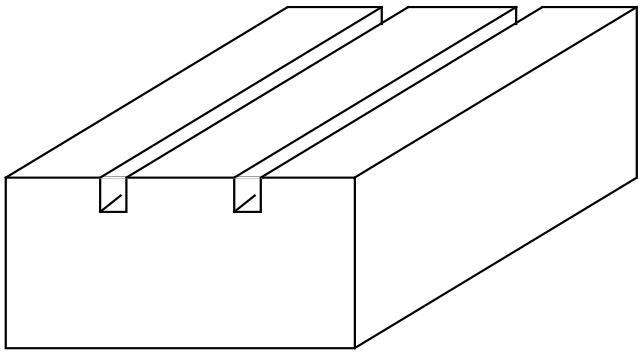

Fig. 4 A schematic illustration (not to scale) of a grooved lead brick.

The setup inside the irradiation cell is shown in Fig. 5. Part (a) is the setup employed in the first irradiation strategy described above, depicting the grooved lead bricks used to shield the peripheral circuits and the I/O pads. This set up was placed on a hydraulic lift, and its height was adjusted in concert with the height of the radiation source. Part (b) is the set up employed in the second irradiation strategy described above. Part (c) is two vertical pipes through which two Co^{60} γ-ray radiation sources come when an irradiation experiment is to start. When not in use, the two radiation sources rest 20 feet underground (totally shielded). They are manipulated down to underground and up to the irradiation cell by air pressure. Each of the two sources can be individually selected for use. Part (d) is a Geiger meter to monitor radiation in the cell when two sources are underground. Part (e) is a set of connectors to a laboratory area outside the irradiation cell. These connectors

are used to provide power and monitor signals. The laboratory area outside the cell is used to do measurements in a timely fashion consistent with the *MIL-STD-883E, Method 1019.5*, Ionizing Radiation (Total Dose) test standard that was followed. A more detailed photograph of part (a) is shown in Fig. 6. The two vertical pipes that appear in front of the setup in this photograph are the pipes through which the two radiation sources come.

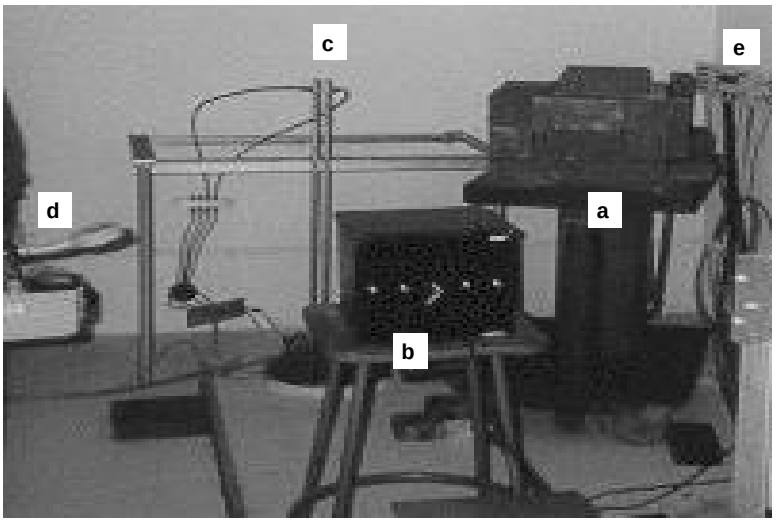

Fig. 5 The setup inside the irradiation cell.

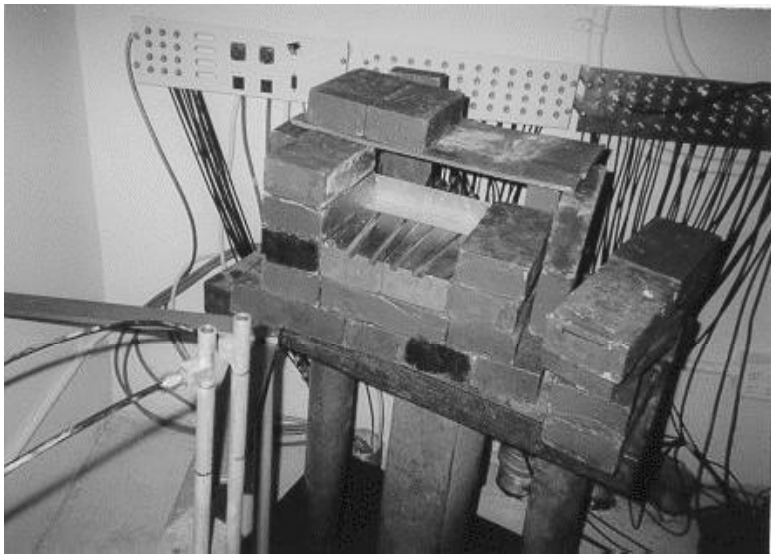

Fig. 6 A photograph of the setup employed in the first irradiation strategy.

5. EXPERIMENTAL RESULTS

1. Measurements Employing the First Strategy:

Irradiation and measurements were performed at ambient temperature and pressure. The measured dose rate at the test chip pixel array faceplate was approximately 0.4 rad (Si)/s. The relatively low dose rate was because of the required setup, in which lead blocks with windows were used to only expose the pixel array (and not the periphery circuits and the I/O pads) to radiation, as described in the previous section. To ensure uniformity of radiation across the array, the setup was relatively far from the radiation source, hence the relatively low dose rate. Measurements of dark signal were done at several total dose levels up to approximately 88 Krad (Si). During irradiation, the image sensor test chip was biased and clocked, simulating actual operation. At all the total dose levels, up to and including approximately 88 Krad (Si), the image sensor test chip was functional. The highest total dose level to which the image sensor test chip was exposed to (approximately 88 Krad (Si)) was the highest total dose level that can be realized within the time allocated to the irradiation experiment (one week), and not because the image sensor test chip seized to function afterwards.

The dark output voltage was measured for each pixel within the pixel array by integrating the test chip image sensor in the dark for a certain integration time. The average dark output voltage of a specific pixel type was calculated by averaging the dark output voltages from all the relevant pixels within that pixel type subarray. Then, the integration time was varied (several times) and the corresponding average dark output voltages were measured for each pixel type. The average dark output voltage was then plotted against integration time (for each pixel type), producing a straight line, the slope of which is the average dark signal (dark output voltage per unit time). The data is presented in Fig. 7, which shows the average dark signal in mV/s versus the total dose level in Krad (Si) for each of the eight pixel designs included in the test chip pixel array. After irradiation, the test chip image sensor was annealed for 168 hours at 100°C. The measured average dark signal for each of the eight radiation hard pixel designs after annealing is shown in Fig. 7 as well. Also included, for comparison, is data for a conventional pixel that was not designed to be radiation hard [8]. However, the pixel size of the non-radiation hard pixel is 14 μm X 14 μm compared to 28 μm X 28 μm for each of the radiation hard pixels. It should be noted that dark signal scales with pixel area. The data presented in Fig. 7 shows that the dark signal performance of any of the radiation hard pixels is better than that of the non-radiation hard pixel, even though the area of the non-radiation hard pixel is four times smaller than that of each of the radiation hard pixels. Among the eight radiation hard pixel designs, two (pixel type3 and pixel type 8) exhibited significantly worse dark signal performance than the other six designs. For a closer look at the data, Fig. 8 shows the same data after excluding the non-radiation hard pixel and the two radiation hard pixel designs (pixel type 3 and pixel type 8) that exhibited significantly worse dark signal performance than the other six designs.

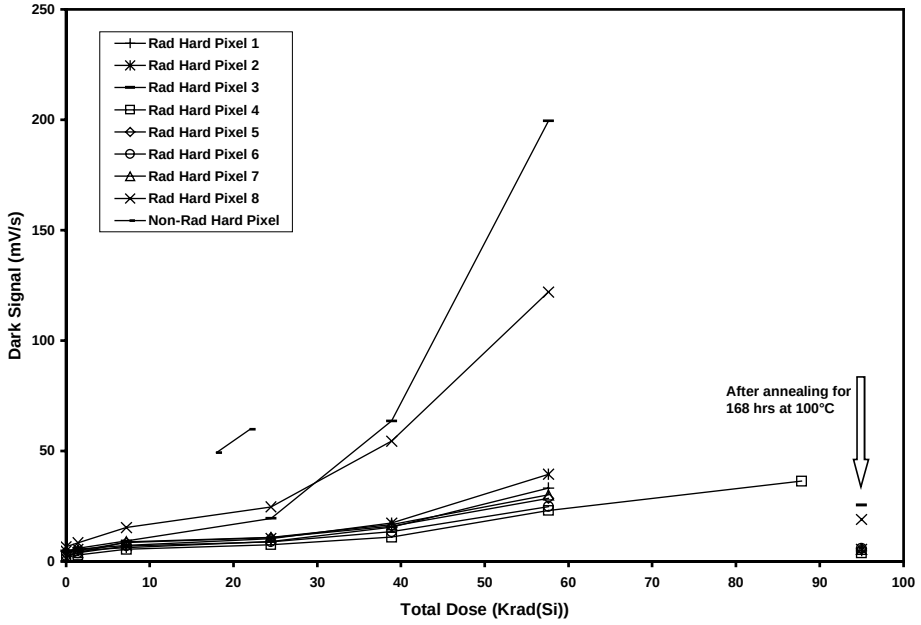

Fig. 7 Average dark signal versus total dose level for various types of pixels, radiation hard and non-radiation hard.

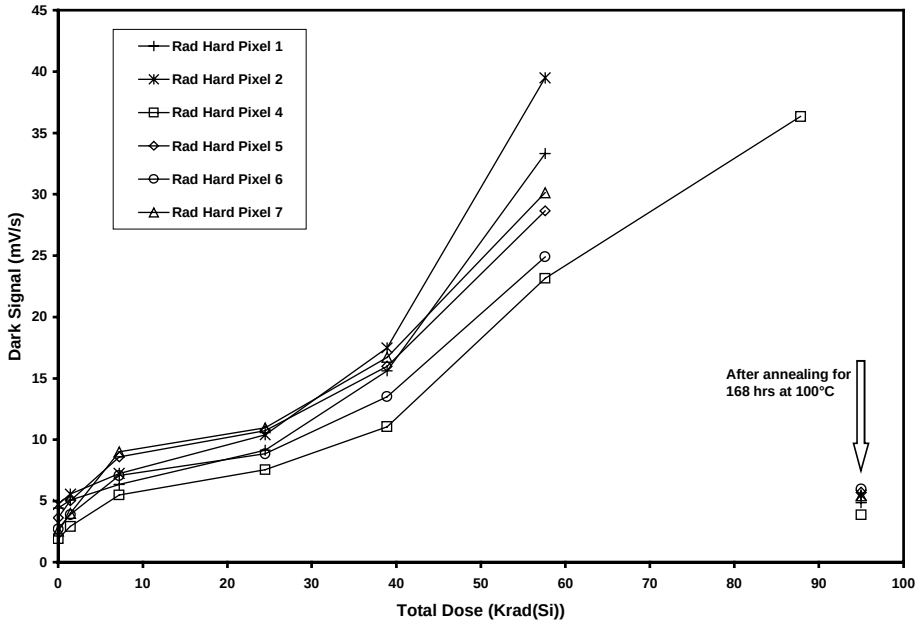

Fig. 8 Average dark signal versus total dose level for six types of radiation hard pixels.

It is apparent from Fig. 8 that pixel type 4 has the best dark signal performance among the eight pixel designs included in the test chip pixel array. For an even closer look at the performance of pixel type 4, its data is shown exclusively in Fig. 9. For pixel type 4, the pre-radiation average dark signal was approximately 1.92 mV/s. At a total dose level of approximately 88 Krad (Si), it increased to approximately 36.35 mV/s. After annealing for 168 hours at 100°C, it dropped to approximately 3.87 mV/s.

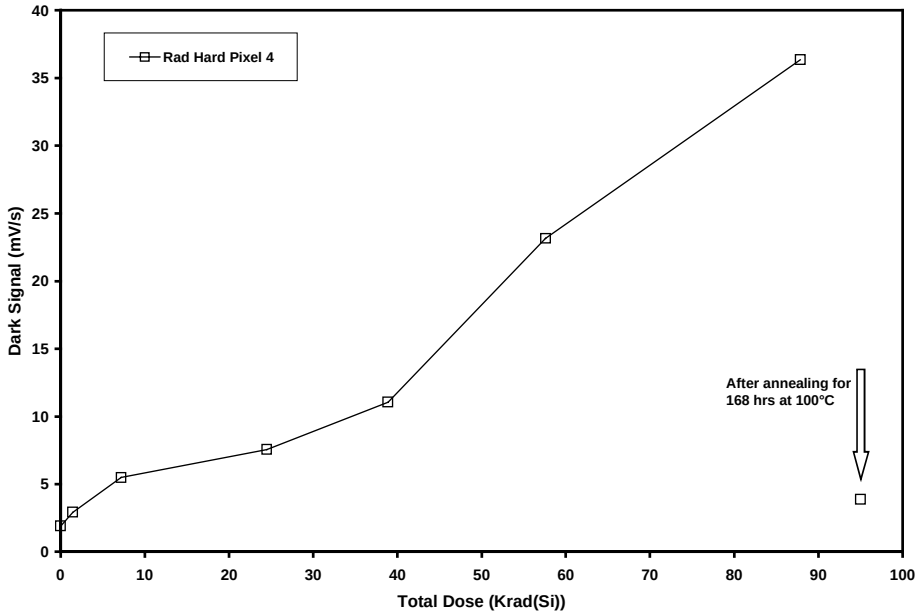

Fig. 9 Average dark signal versus total dose level for pixel type 4.

2. Measurements Employing the Second Strategy:

Irradiation and measurements were performed at ambient temperature and pressure. The measured dose rate at faceplate was approximately 0.3 rad (Si)/s. Both the radiation hard test chip image sensor and a non-radiation hard test chip image sensor were exposed to radiation for comparative measurements. Measurements of dark signal were done at total dose levels of approximately 1 Krad (Si) and 19 Krad (Si), and after one-day annealing at room temperature. Static biases representing the worst case scenario for radiation effects were used.

At a total dose level of approximately 1 Krad (Si), the average dark signal of the radiation hard pixel (type 4) was approximately 4.5 mV/s, while that of the non-radiation hard pixel was approximately 5.3 mV/s. However, the sizes of the radiation hard pixel and the non-radiation hard pixel were different. The size of the radiation hard pixel is 28 μm X 28 μm, while that of the non-radiation hard pixel is 14 μm X 14 μm. Taking the two different sizes into consideration, it is concluded that the radiation hard pixel exhibited better dark signal performance than that of the non-radiation hard one by *at least* a factor of approximately 1.18 at the low total dose level of 1 Krad (Si).

At a total dose level of approximately 19 Krad (Si), the average dark signal of the radiation hard pixel (type 4) was approximately 12.4 mV/s (approximately 2.8 times that at 1 K rad (Si)). On the other hand, at the same total does level, the average dark signal of the non-radiation hard pixel was 46.2 mV/s. This means that at a total dose level of 19 Krad (Si), the radiation hard pixel exhibited better dark signal performance than that of the non-radiation hard one by *at least* a factor of approximately 3.73.

After one day of annealing at room temperature, the average dark signal of the radiation hard pixel (type 4) dropped to approximately 8.6 mV/s. On the other hand, that of the non-radiation hard pixel dropped to approximately 29.7 mV/s. This means that after one day of annealing at room temperature, the radiation hard pixel exhibited better dark signal performance than that of the non-radiation hard one by *at least* a factor of approximately 3.45.

6. DISCUSSION AND CONCLUSIONS

The endeavor of designing a CMOS APS image sensor test chip and irradiating it proved to be very fruitful. It demonstrated that implementing the physical design techniques of enclosed geometry and guard rings in CMOS APS image sensors is possible. It verified that employing these design techniques does not represent a fundamental impediment for the functionality and performance of CMOS APS image sensors. It further proved that CMOS APS image sensors that employ these physical design techniques yield better dark signal performance in ionizing radiation environment than their counterpart that do not employ those physical design techniques.

The inclusion of eight different pixel designs in the test chip pixel array proved to be a very useful evaluation tool. The design approach of having a guard ring in close proximity to the photodiode (pixel types 4, 5, 6, and 7) proved to be very effective in mitigating the adverse effects of total ionizing radiation dose on the dark signal of CMOS APS image sensors. It was also verified that it is possible to reconcile the requirement of a symmetrical pixel (pixel types 5, 6, and 7) and the requirement of tolerable dark signal in ionizing radiation environment. The requirement of pixel symmetry is critical to some space applications such as star tracking. It was also proved that it is possible to have different photodiode shapes (such as rectangular, square, and circle) and still have tolerable dark signal in ionizing radiation environment.

The highest level of total ionizing radiation dose to which the image sensor test chip was exposed to was approximately 88 Krad (Si). The total dose level of 88 Krad (Si) was the highest dose level that can be realized within the time allocated to the irradiation experiment, and not because the image sensor test chip seized to function afterwards. Thus, it is possible that the image sensor test chip may have been able to tolerate a higher level of total ionizing radiation dose. However, the next step is envisioned to be another radiation hard CMOS APS image sensor test chip designed in another CMOS process that has a thinner gate oxide. The current test chip was fabricated in a CMOS process that has a gate oxide approximately 11.5 nm thick. The future radiation hard CMOS APS image sensor test chip is envisioned to be in a CMOS process that has a gate oxide approximately 7.0 nm thick, and be tested up to a total dose level of a few hundreds Krad (Si).

7. ACKNOWLEDGEMENT

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