PROGRESS IN CMOS ACTIVE PIXEL IMAGE SENSORS

Sunetra K. Mendis*, Sabrina E. Kemeny, Russell C. Gee, Bedabrata Pain, Quiesup Kim and Eric R. Fossum

Center for Space Microelectronics Technology
Jet Propulsion Laboratory - California Institute of Technology
Pasadena, CA

ABSTRACT

Recent research results regarding the investigation of CMOS active pixel image sensors (APS) are reported. An investigation of various designs for the pixel, including photogate devices of various geometries and photodiode devices has been performed. Opto-electronic performance including intra-pixel photoresponse maps taken using a focused laser scanning apparatus are presented. Several imaging arrays have also been investigated. A 128 × 128 image sensor has been fabricated and characterized. Both p-well and n-well implementations have been explored. The demonstrated arrays use 2 μm CMOS design rules and have a 40 × 40 μm pixel pitch. Typical design fill-factor is 26%. Output sensitivity is 3.7 μV/e^- for the p-well devices and 6.5 μV/e^- for the n-well devices. Read noise is less than 40 e^- r.m.s. for the baseline designs. Dynamic range has been measured to be over 71 dB using a 5 V supply voltage. The arrays are random access with TTL control signals. Results regarding on-chip suppression of fixed pattern noise will also be presented.

1. INTRODUCTION

In smart image sensor applications, integration of the image sensor with other circuitry both for driving the image sensor and for performing on-chip signal processing is becoming increasingly important [1]. In addition to good imager performance with low-noise, no lag or smear and good blooming control, it is also desirable to have random access, simple clocks and fast read out rates. The development of a CMOS compatible image sensor technology is very beneficial since CMOS is a mature and commonly available technology.

Charge-coupled devices (CCDs) are currently the dominant technology for image sensors. CCD arrays with high fill factor, small pixel sizes and large formats have been achieved and limited signal processing operations have been demonstrated with charge-domain circuits [2-7]. However, CCDs cannot be easily integrated with CMOS circuits due to the additional fabrication complexity and increased cost. CCDs also need complex clocks for operation. The readout rate is limited due to the inherent sequential read out of CCDs and the need to achieve nearly perfect charge transfer efficiency to maintain signal fidelity. CCDs also suffer from smear and susceptibility to radiation damage.

An active pixel image sensor is defined as an image sensor technology that has one or more active transistors within the pixel unit cell [8]. Previously demonstrated active pixel sensor (APS) technologies include the amplified MOS imager (AMI) [9], charge modulation device (CMD) [10], bulk charge modulated device (BCMD) [11], base stored image sensor (BASIS) [12] and the static induction transistor (SIT) [13]. Although AMIs are both CMOS compatible and amenable to integration with on-chip circuitry, high noise levels and lag are a problem. CMDs, BCMDs and BASIS are also amenable to integration with on-chip circuitry, but can be made CMOS compatible only with additional fabrication steps. SITs are difficult to integrate with on-chip circuitry and are not CMOS compatible.

The CMOS active pixel sensors described in this paper are inherently CMOS compatible. Each pixel unit cell contains an imaging element and three transistors for readout, selection and reset. A column parallel architecture is used for readout and the imager is scanned row by row. In all the designs random access is possible, allowing selective readout of

* Sunetra K. Mendis is a student at Columbia University, NY, conducting her Ph.D. dissertation research at the Jet Propulsion Laboratory.

Table 1: Summary of pixel designs

Name	Pixel Design	Array Size
AR28P2	P-well photogate	28 × 28
AR128P2	P-well photogate	128 × 128
AR28N	N-well photogate	28 × 28
AR128N1	N-well photogate	128 × 128
APSG2	P-well photogate with light shield	28 × 28
APSG4	P-well square photogate	28 × 28
APSG1	P-well tiny pixel photogate	28 × 28
APSG3B	P-well single poly tiny pixel	28 × 28
APSG5	N-well photodiode	28 × 28
AR28NCB	N-well photogate with crowbar	28 × 28

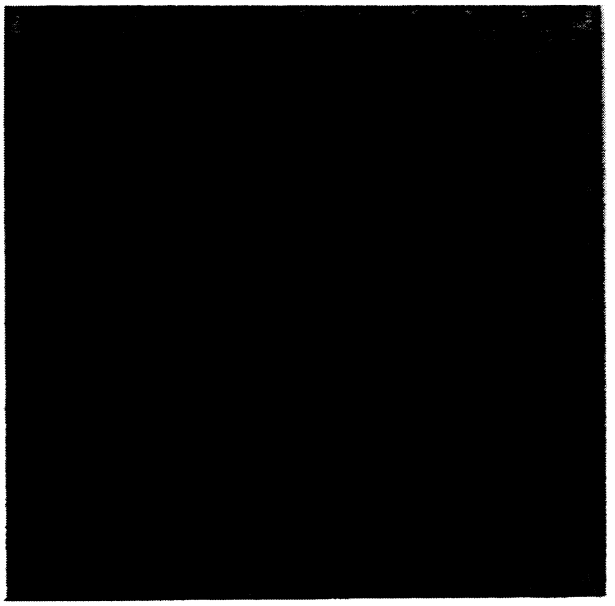

Fig. 1: Photograph of completed integrated circuit. (128 × 128 array)

windows of interest. The image sensors are operated with TTL clocks and at most two other d.c. voltages. These image sensors achieve lateral blooming control through proper biasing of the reset transistor. No lag or smear is evident. The reset and signal levels are read out differentially, allowing off-chip correlated double sampling (CDS) to eliminate kTC noise, 1/f noise and fixed pattern noise from the pixel. Low noise and high dynamic range are achieved. The option of using a radiation hard CMOS process is also available. CMOS active pixel image sensors are suitable for many applications including robotics and machine vision, guidance and navigation, automotive applications, and consumer electronics such as video phones, computer inputs and home surveillance devices.

This paper presents recent achievements in CMOS APS research. Section 2 describes the basic chip architecture employed in the design of CMOS active pixel image sensors. Section 3 presents the baseline design, its operation and experimental results. Section 4 describes the different pixel unit cell designs explored and compares their performance with the baseline design. Two fixed pattern noise suppression methods that were investigated are presented in section 5.

2. CMOS APS TEST CHIPS

The 10 different active pixel arrays that were fabricated are summarized in table 1. All the designs were fabricated at Orbit Semiconductor through the MOSIS foundry service. In the baseline design, each pixel contains a photogate imaging element like a single CCD stage with a floating diffusion output. This design was first implemented using a p-well CMOS technology as a 28 × 28 test array (AR28P2) and later expanded to a 128 × 128 array (AR128P2) and n-well implementations (AR28N and AR128N1). Other test arrays were demonstrated for pixel designs with a light shield on the transistors within the pixel (APSG2), a square photogate (APSG4), a minimum size photogate (APSG1) and a single-poly implementation of the minimum size photogate (APSG3B). A 28 × 28 photodiode active pixel sensor array was also implemented (APSG5). A test array of the baseline pixel design with a modified readout circuit was developed for fixed pattern noise suppression using an n-well CMOS technology (AR28NCB).

2.1 Chip architecture

The CMOS active pixel sensor chips were fabricated using 2 μm CMOS technology with two levels of polysilicon and two levels of metal. The resulting pixel size was 40 μm × 40 μm. A photograph of a completed 128 × 128 CMOS APS array is shown in Fig. 1. A column parallel architecture was used, where an entire column of pixels shares one readout circuit. The row decoders and clock generator circuits to the left of the APS array and the column decoders and readout circuits below the APS array were all designed to fit within the 40 μm pixel pitch. The 7-bit row and column address

decoders were formed using standard CMOS logic permitting direct X-Y addressing of the image sensor. The circuitry outside the pixel array is covered by a light shield. The 28 × 28 test arrays were also designed with the same chip architecture. The die areas of the large and small arrays were 6.8 mm × 6.8 mm and 2.20 mm × 2.25 mm respectively. The pixel unit cell and readout circuits were designed to achieve 30 Hz operation of a 128 × 128 array.

2.2 Readout circuit

A schematic of the readout circuit used in the CMOS APS arrays is shown in Fig. 2(a). The pixel unit cell is shown within the dotted outline. In addition to the imaging structure consisting of a photogate (PG) with a floating diffusion output (FD) separated by a transfer gate (TX), the pixel unit cell also contains a reset transistor (R), the input transistor of the first source-follower and a row selection transistor (X). The readout circuit which is common to an entire column of pixels includes the load transistor of the first source-follower (VLN) and two sample and hold circuits for storing the signal level and the reset level. Each sample and hold circuit consists of a sample and hold switch (SHS or SHR) and capacitor (CS or CR) and a second source follower and column selection transistor (Y1 or Y2). The load transistors of the second set of source-followers (VLP1 and VLP2) are common to the entire array of pixels.

3. BASELINE DESIGN OF CMOS ACTIVE PIXEL IMAGE SENSOR

3.1 Design and Operation

The first CMOS active pixel image sensor demonstrated has a pixel unit cell with a photogate (PG), transfer gate (TX) and a floating diffusion output (FD) as shown schematically in Fig. 3(a). In essence, a small surface-channel CCD has been fabricated within each pixel.

The operation of this image sensor is illustrated in Figs. 3(a)-(d). The rail voltages are set at 5V and 0V, and the transfer gate is biased at 2.5V. During the signal integration period (Fig. 3(a)), photo-generated electrons are collected under the photogate PG biased at 5V. The reset transistor R is biased at 2.5V to act as a lateral anti-blooming drain, allowing excess charge to flow to the reset drain. The row-selection transistor X is biased off at 0V. Following signal integration, an entire row of pixels are read out simultaneously. First, the pixels in the row to be read out are addressed by enabling row selection switch X. Then the floating diffusion output node of the pixel (FD) is reset by briefly pulsing the reset gate R to 5V. This resets FD to approximately 3.5V (Fig. 3(b)). The output of the first source follower is sampled onto capacitor CR at the bottom of the column by enabling sample and hold switch SHR. Then, PG is pulsed low to 0V, transferring the signal charge to FD (Fig. 3(c)). The new output voltage is sampled onto capacitor CS by enabling sample and hold switch SHS (Fig. 3(d)).

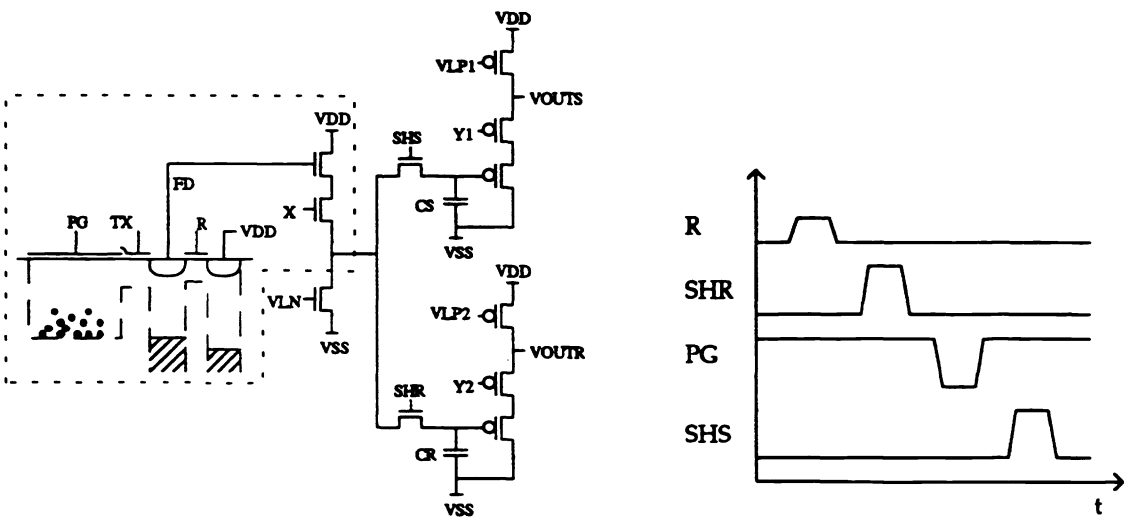

Figure 2(a): Schematic of readout circuit (b) timing for CMOS APS read out

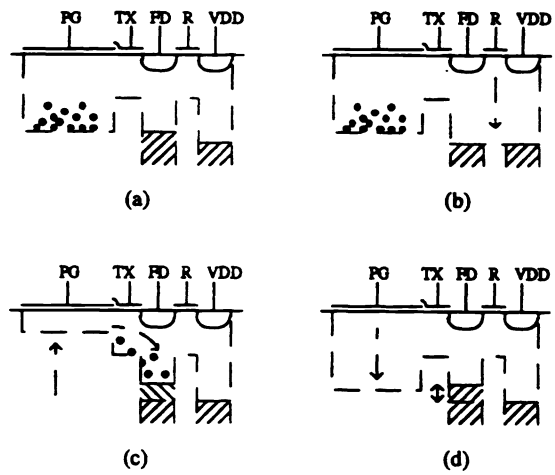

Fig. 3: Operation of CMOS APS (a) signal integration (b) reset (c) signal charge transfer (d) signal readout

The stored reset and signal levels are sequentially scanned out through the second set of source followers by enabling column address switches Y1 and Y2. This timing sequence is shown in Fig. 2(b).

Sampling both the reset and signal levels permits correlated double sampling (CDS) which suppresses kTC noise from the floating diffusion node of the pixel and 1/f noise and threshold variations from the source-follower input transistor within the pixel [14]. The main source of noise in this system is the kTC noise introduced by the sample and hold capacitors in the readout circuit. The sample and hold capacitors of the 28×28 test arrays and the 128×128 p-well array were designed to be poly1-poly2 capacitors of 1 pF. The calculated r.m.s. noise is 64 μV per capacitor, resulting in 91 μV for differential mode. The sample and hold capacitors of the n-well 128×128 arrays were increased to approximately 2.3 pF by using an MOS capacitor under the poly1-poly2 capacitor. The calculated r.m.s. noise for this circuit is 42 μV per capacitor, resulting in 60 μV for differential mode.

3.2 Experimental Results

The active pixel image sensors were operated with the timing and voltages described above. However, in the n-well imager sensors, the load transistor of the first source follower had to be biased at 1.25 V. Higher biasing made the column amplifiers "glow" and saturate the bottom part of the image sensor array. This effect can be reduced by switching off column selection transistors Y1 and Y2 in all the columns during long integration periods. Both dark and illuminated testing of the sensors were performed. Through shot noise measurements, the pixel sensitivity was determined to be 3.7 $\mu V/e^-$ for the p-well design and 6.5 $\mu V/e^-$ for the n-well design. By performing electrical tests on a test structure on a separate IC, the sensitivity at the output of the first source follower was measured to be 4.0 $\mu V/e^-$ for the p-well design. Although the well capacity was calculated to be approximately 6×10^6 e^-, saturation was determined by the output amplifier. The observed saturation level was 600 mV corresponding to 162,000 e^- for the p-well design and 1.2V corresponding to 185,000 e^- for the n-well design. However, higher saturation levels can be achieved by operating the image sensors with a higher supply voltage. For example, by increasing the supply voltage to 6V, the saturation level in the p-well design was increased to approximately 1.1V corresponding to 297,000 e^-.

The sensors were nominally clocked at 2 μs/pixel, corresponding to a frame rate of approximately 30 Hz. For 5V operation, power dissipation was measured to be approximately 7 mW for the 128×128 arrays and 5.9 mW for the 28×28 arrays. The major power dissipation was in the p-channel transistors (87%) compared to the column-parallel n-channel transistors (13%). Low power operation of the test array was demonstrated with a supply voltage of 3V. The power dissipation was 0.84 mW and the saturation level was 200 mV for this mode of operation.

A raw output image from the 128×128 p-well image sensor is shown in Fig. 4(a). The fixed pattern noise is dominated by column-wise fixed pattern noise as evidenced by faint vertical streaks in the image. (Note that the half-toning process gives rise to artificial streaks not present in the original photograph.) In the p-well designs, global fixed pattern noise (FPN) observed in the differential output signal was approximately 20 mV p-p (3.3% sat.), with a local variation of approximately 8 mV p-p. The global variation is attributed to poor control of the p-well potential towards the center of the array since slower clocking rates reduced the effect, and the 28×28 array showed a similar but much smaller effect. Dark current was measured to be approximately 0.26 V/s, or under 1 nA/cm^2. Noise in the fabricated p-well array is fundamentally

Fig. 4(a): Raw image from 128 × 128 CMOS APS

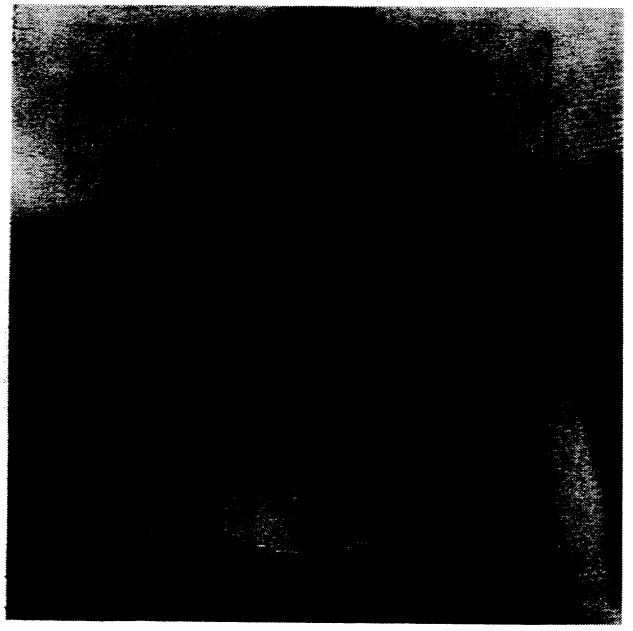

Fig. 4(b): Image with FPN suppression through subtracting a column reference

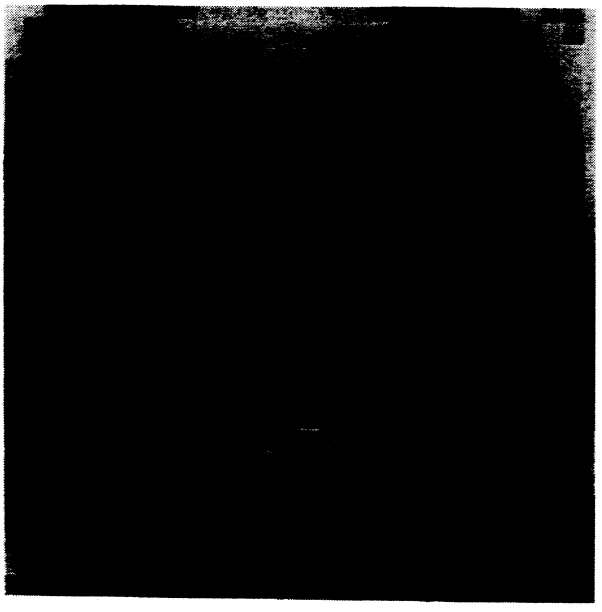

Fig. 4(c): Raw image at 3V operation (28 × 28 array)

limited to 88 μV due to the kTC noise on the 1 pF sample and hold capacitors. However, the measured noise level at a 30 Hz frame rate at room temperature is presently limited by dark current shot noise to approximately 160 μV, resulting in a dynamic range of 71 dB. Fig. 4(c) shows a raw image from the p-well 28 × 28 array in the low power mode of operation.

The responsivity of the n-well image sensor was approximately 3 times that of the p-well sensor at the same illumination. Global fixed pattern noise (FPN) observed in the differential output signal was approximately 30 mV p-p (2.5% sat.). Dark current was measured to be approximately 1.76 V/s. The measured noise level at a 30 Hz frame rate at room temperature was approximately 209 μV, resulting in a dynamic range of 75 dB. In both the p-well and n-well implementations, no lag or smear was observed. Blooming was suppressed through proper biasing of the reset transistor R.

The higher responsivity in the n-well designs can be attributed to the increased collection depth as shown in the pixel cross sections in Fig. 5. In the p-well designs, the well depth of approximately 2 μm limits the carrier generation depth (Fig. 5(a)). In addition, the well depth is small compared to the pixel dimensions of 40 μm × 40 μm. Therefore, electrons that are generated deep in the well outside a photogate area are more likely to diffuse to the n-substrate than be collected under a photogate. In the n-well designs, electrons that are generated in the substrate below a photogate can be collected by that pixel or diffuse to adjacent pixels (Fig. 5(b)). This phenomenon also results in higher cross talk in the n-well designs than the p-well designs.

Fig. 5(a): Cross section of p-well pixel

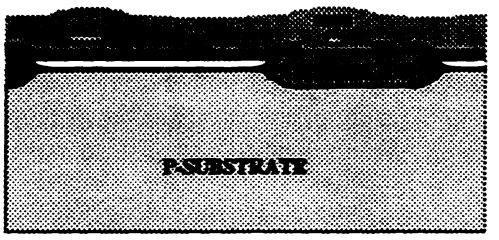

Fig. 5(b): Cross section of n-well pixel

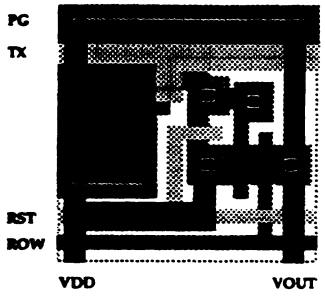

Fig. 6(a): Layout of baseline pixel

Laser spot scans of individual pixels at 632.8 nm and 488 nm showed both higher response and higher cross talk in the n-well designs than the p-well designs. The pixel layout of the baseline pixel is shown in Fig. 6(a) for comparison with the responsivity maps. The 632.8 nm He-Ne laser had a beam diameter of approximately 1.5 μm and a step size of approximately 2 μm. The responsivity maps of the p-well and n-well pixel are presented in Fig. 5(b) and 5(c) respectively. In the p-well design, the response is uniform across the photogate area with only poly1 and drops off rapidly at the edges. A lower response is noticeable in areas overlapped by poly2 or metal. In the n-well design, the response drops off more gradually, and cross talk from adjacent pixels is evident. The responsivity maps at 488 nm in Figs. 5(d) and 5(e) show similar patterns. However, the response is lower than at 632.8 nm due to the polysilicon photogate.

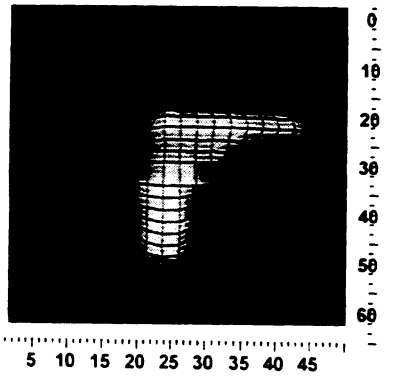

Fig. 6(b): responsivity map of p-well pixel at 632.8 nm

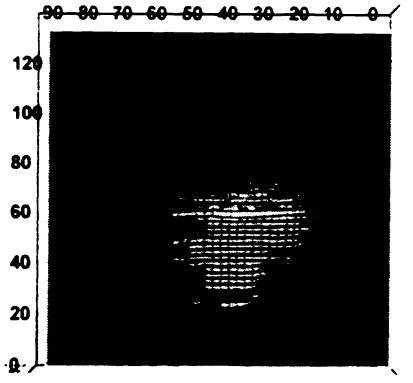

Fig. 6(c): responsivity map of n-well pixel at 632.8 nm

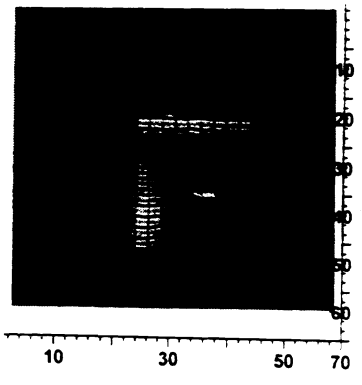

Fig. 6(d): responsivity map of p-well pixel at 488 nm

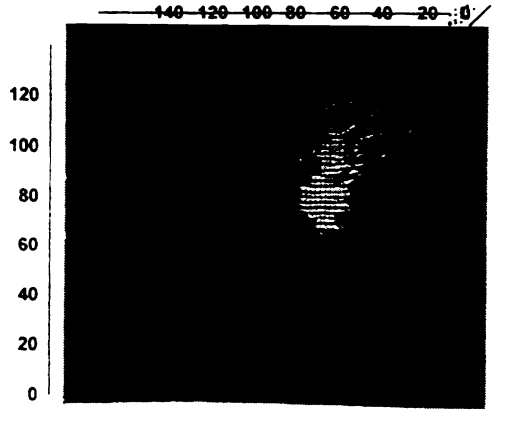

Fig. 6(e): responsivity map of n-well pixel at 488 nm

4. OTHER CMOS APS DESIGNS

Variations of the baseline CMOS APS design were investigated and fabricated using a p-well CMOS process. In addition to normal operation of the image sensors laser spot scans of pixels were performed at 632.8 nm. These designs and results are presented below and summarized in table 2.

4.1 Light shielded pixel

A pixel design with light shield covering the entire pixel except the photogate to limit cross talk was fabricated (Fig. 7(a)). The responsivity (Fig. 7(b)) was similar to the p-well baseline design, but showed a steeper drop off at the edge of the photogate area and no detectable response in the area covered by the light shield. The saturation level was 800 mV and the output sensitivity was determined to be 3.0 $\mu V/e^-$. The measured noise was 168 μV, similar to the other p-well designs.

4.2 Square photogate pixel

A pixel design with a square photogate which achieved a fill factor of 18% was demonstrated (Fig. 8(a)). The baseline design was optimized for high fill factor, which resulted in an L-shaped photogate area. However, a pixel with a regular photogate structure is more suitable for use with microlenses which can increase the effective fill factor to over 70%. A square pixel is also more amenable for use by centroiding algorithms. The sensitivity of the square photogate pixel was determined to be 3.1 $\mu V/e^-$. The full well capacity of the square pixel was calculated to be approximately 3.7×10^6 e^-, but similar to the baseline design, saturation was limited to approximately 132,000 e^- by the output amplifier. A laser spot scan of this pixel (Fig. 7(b)) shows that responsivity is highest under the photogate as in the other p-well designs.

4.3 Tiny photogate pixel

A minimum size photogate design of 3 $\mu m \times 4$ μm with a fill factor of 0.75% was investigated (Fig. 9(a)). Typical diffusion length for electrons in these devices is in the order of centimeters. Therefore, it is possible for photo-generated charge outside the photogate area to diffuse towards the photogate and be collected. Since the blue response is affected by the photogate, it was hoped that the open area within the pixel with a minimum size photogate would improve the blue response. However, due to the effect of the p-well depth described in section 3.2 above, no significant response was observed outside the photogate area as shown in the responsivity map in Fig. 9(b). It is expected that an n-well implementation of this design would show much higher response. The saturation level was 400 mV and the sensitivity was determined to be 2.8 $\mu V/e^-$. The measured noise level was 168 $\mu V/e^-$. The full-well capacity for this design was approximately 175,000 e^- which is still higher than the saturation limit determined by the output amplifier.

4.4 Single-poly tiny photogate pixel

A p-well tiny pixel was also implemented as a single-poly design (Fig. 10(a)). This design was investigated as single-poly CMOS processes are more commonly available in sub-micron technologies than double-poly processes. The responsivity was very similar to the tiny photogate pixel (Fig. 10(b)). The sensitivity of the single-poly tiny-pixel was determined to be 3.6 $\mu V/e^-$ and the saturation level was 500 mV. The measured noise level was 180 μV.

4.5 Photodiode pixel

A photodiode pixel with the same output structure as the above circuits was demonstrated in a p-well process (Fig. 11(a)). This pixel design achieved a fill factor of 35%. Since the output node is the same as the signal charge collection area, it is not possible to reset the output node before readout to eliminate kTC noise by CDS as in the photogate designs. However, by resetting the photodiode after readout and using that reset level for CDS, it is possible to eliminate 1/f noise and fixed pattern noise from the pixel. The capacitance of the photodiode node is higher than the capacitance of the output node of the photogate designs, resulting in lower sensitivity. The sensitivity of the photodiode pixel was determined to be approximately 2.1 $\mu V/e^-$. Although the sensitivity is lower, the signal level was approximately 5 times higher than in the baseline photogate design at the same illumination due to the improved blue response. The saturation level was observed to be approximately 1.3 V. Fixed pattern noise was approximately 7 mV p-p or less than 0.6% sat. Measured noise was 177 μV. Laser spot scans at 632 nm and 480 nm (Figs. 11(b) and 11(c)) show improved blue response over the photogate designs.

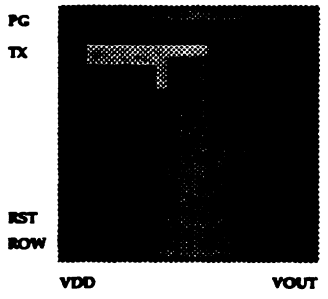

Fig. 7(a): Layout of light-shielded pixel

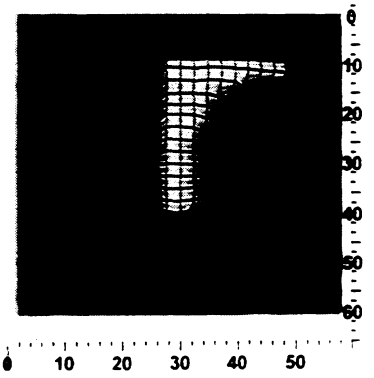

Fig. 7(b): Responsivity map of light-shielded pixel

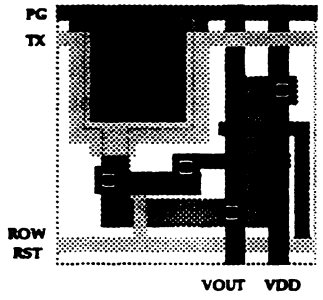

Fig. 8(a): Layout of square pixel

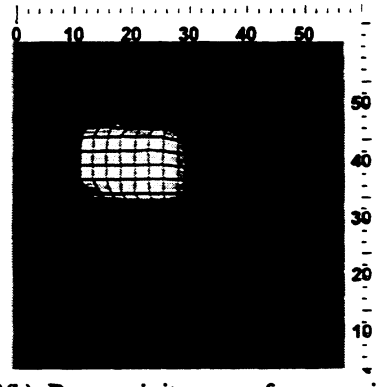

Fig. 8(b): Responsivity map of square pixel

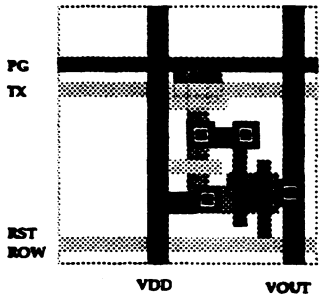

Fig. 9(a): Layout of tiny photogate pixel

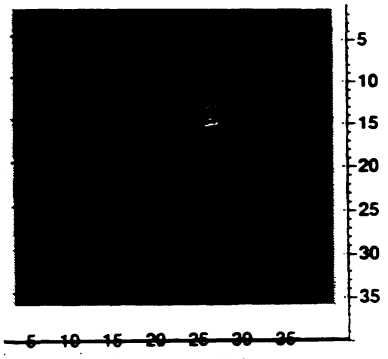

Fig. 9(b): Responsivity map of tiny photogate pixel

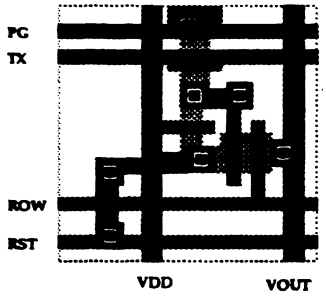

Fig. 10 (a): Layout of single poly pixel

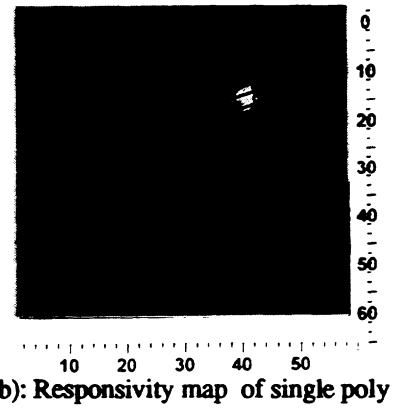

Fig. 10(b): Responsivity map of single poly pixel

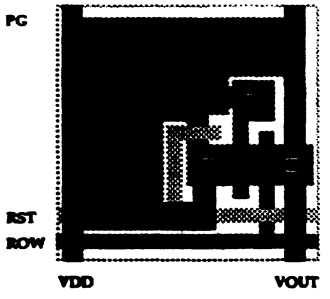

Fig. 11(a) Layout of photodiode pixel

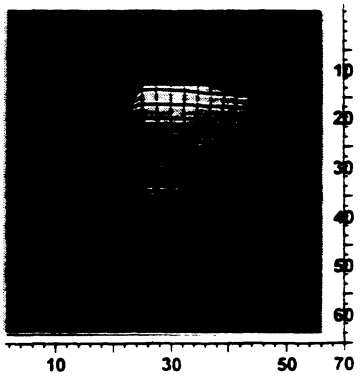

Fig. 11 (b): responsivity map at 632 nm

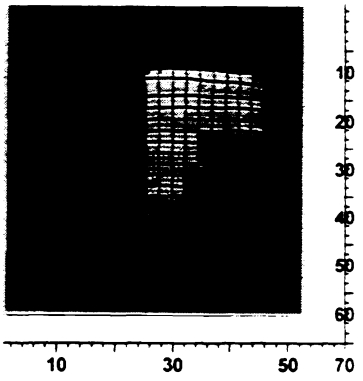

Fig. 11(c) responsivity map at 488 nm

5. FIXED PATTERN NOISE SUPPRESSION

5.1 Subtracting a column reference

It was evident in all the CMOS active pixel image sensor designs described above that the fixed pattern noise was dominated by the column to column variations. FPN can therefore be greatly reduced by eliminating or reducing the column-wise FPN. The first such method demonstrated uses computer software to subtract a dark reference voltage from the signal. The reference for each column is obtained from the last row of pixels in the array, which is covered by light shield. Fig. 4(b) demonstrates the improvement in image quality when FPN suppression is on. With FPN suppression on, the measured global FPN reduces to 0.8% p-p from 3.3% p-p in the p-well baseline design. Of course, an entire dark image can be subtracted from an acquired image for greater FPN suppression, but this requires acquisition of the dark image.

5.2 Crowbar circuit

A column-FPN suppression scheme was incorporated into the output circuit of the next design. The baseline design of a photogate pixel with floating diffusion output was used with the modified output circuit shown in Fig. 12(a). In each column output circuit, a crowbar switch (CB) and two column selection switches on either side (S1 and S2) were added to selectively short the two sample-and-hold capacitors CS and CR. The image sensor is operated as described previously up to the sampling of the reset and signal levels onto the two sample-and-hold capacitors. However, during the scanning of the columns, an additional step is performed. After differentially reading out the reset level and signal level stored in each column (Δ1), the crowbar switch is pulsed, thereby shorting the two sample-and-hold capacitors in the column that is being addressed. The outputs of the reset and signal branches are again read out differentially and this reference level (Δ2) is

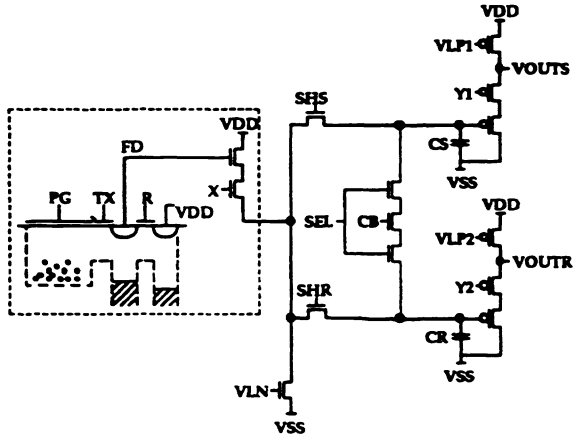

Fig. 12(a): CMOS APS unit cell and crowbar readout circuit

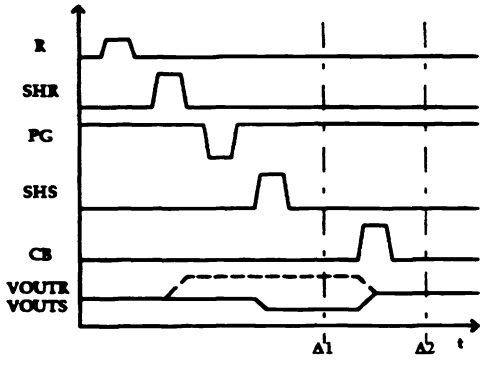

Fig. 12(b): Timing for crowbar readout

Fig. 13(a): FPN with crowbar off

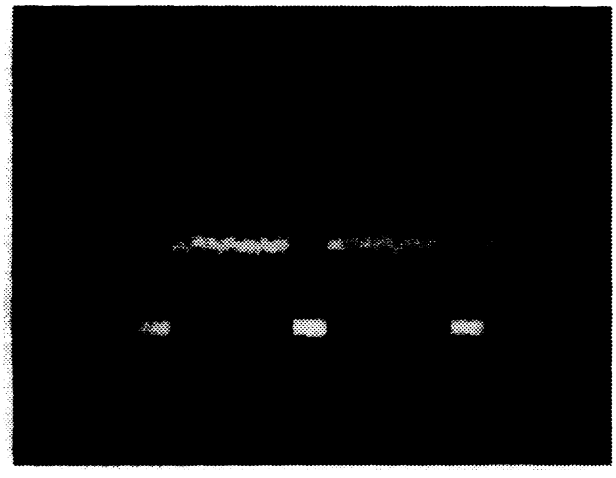

Fig. 13(b): FPN with crowbar on

subtracted from the previous reading ($\Delta'=\Delta1-\Delta2$). Oscilloscope photos of the output from an n-well crowbar array without and with the crowbar operation are shown in Figs. 13(a) and 13(b) respectively. Global FPN of approximately 10 mV was reduced to approximately 1 mV with the crowbar operation. Since the saturation in this image sensor was 1.3V, the FPN is reduced from 0.8% sat. to less than 0.08% sat. The output sensitivity was determined to be 7.1 $\mu V/e^-$ and the measured noise level was 197 $\mu V/e^-$.

6. CONCLUSIONS

The development of several CMOS-based image sensors has been presented. Good blooming control was achieved and no lag or smear was observed. Various pixel designs optimized for limiting cross talk, integration with microlenses, improving blue response and use of single-poly CMOS processes have been investigated. In general, n-well designs had higher sensitivity and saturation levels than p-well designs which can be attributed to lower capacitance of the floating diffusion output node in the n-well process than in the p-well process. P-well designs showed lower responsivity and no cross talk between pixels due to the well depth. N-well designs showed higher responsivity but also showed some cross talk. Since the noise levels were also higher in the n-well designs, dynamic range was comparable to the p-well designs. Both on-chip and off-chip column-FPN reduction schemes were explored. Global FPN was reduced to less than 0.1% using the crowbar circuit.

Table 2: Summary of experimental results

Name	Pixel Design	Saturation	Sensitivity $\mu V/e^-$	Noise* μV	input referred noise e^-	Dynamic Range	r.m.s. FPN	Dark Current
AR28P2	P-well PG	700 mV	3.3	160	37	73	26 mV	
AR128P2	P-well PG	600 mV	3.7	153	30	72	20 mV	0.262 V/s
AR128N1	N-well PG	1.2 V	6.5	209	28	76	30 mV	1.76 V/s
APSG2	Light-shielded	800 mV	3.0	168	44	74		
APSG4	Square PG	1 V	3.1					
APSG1	Tiny PG	400 mV	2.8	168	47	68		
APSG3B	Single poly	500 mV	3.6	180	41	75		
APSG5	Photodiode	1.3 V	2.1	177	68	77	7 mV	
AR28NCB	Crowbar	1.3 V	7.1	197	23	76	1 mV	1.16 V/s

*System noise: 102 μV

Improved readout schemes and methods to further reduce FPN are currently being investigated. Integration of on-chip analog-to-digital conversion is being explored. Reduction in pixel size through the use of 0.8 μm and 1.2 μm CMOS technology can reduce dark current. The use of microlenses can improve the effective fill-factor to over 70%. This on-going research work paves the way for the development of more complex pixel structures and the integration of on-chip electronics in the future [15].

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