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ABSTRACT

The use of charge-coupled device (CCD) circuits in Z-plane architectures for focal-plane image processing is discussed. The low-power, compact layout nature of CCDs makes them attractive for Z-plane application. Three application areas are addressed; non-uniformity compensation using CCD MDAC circuits, neighborhood image processing functions implemented with CCD circuits, and the use of CCDs for buffering multiple image frames. Such buffering enables spatial-temporal image transformation for lossless compression.

INTRODUCTION

High frame rate and high definition imaging demands massive throughput in real-time image processing systems. Digital processors operating on pixel data at the required throughput rate (typically several billion operations per second) consume significant power and volume, and thus are generally inappropriate for applications such as remote sensing, autonomous vehicles, and machine vision.

Focal-plane image processing, in which image acquisition and image processing circuitry are integrated on the same chip, shows promise for alleviating the severe constraints associated with real-time image processing as well as improving signal quality.[1] Focal-plane image processing can imply a wide degree of signal processing functions. Edge detection and image coding require a high degree of processing whereas integration of detector buffer/amplifiers is significantly less demanding. Spatially parallel architectures have a processor associated with each pixel thereby increasing throughput by using a high degree of parallelism. Utilization of a spatially parallel architecture in focal-plane image processing is made difficult by the lack of available real-estate on the focal plane. Analog circuits tend to pack more processing power into a smaller amount of real-estate, and for image processing, the accuracy delivered by analog circuits is generally sufficient. Furthermore, the use of analog circuitry obviates the need for A/D conversion on the focal plane prior to processing. The use of analog charge-coupled device (CCD) circuits can further reduce the real-estate required to implement particular circuit functions[2], and several monolithic focal-plane image processors based on the CCD technology are being explored[3,4,5]. However, in each case detector fill-factor suffers from this integration.

The Z-plane architecture enables the practical realization of three dimensional electronic circuitry.[6] In the case of imaging, the Z-plane architecture provides the additional real-estate for pixel processing circuitry perpendicular to the image plane and facilitates the implementation of spatially parallel focal-plane image processing without sacrificing detector fill-factor. In Fig. 1, an exploded view of the Z-plane architecture is illustrated. Thinned integrated circuits (ICs) are stacked to form a three-dimensional cube of circuitry. An imager array is hybridized to the IC stack so that each row of the imager array is attached to one of the ICs. An individual connection is made for each pixel. Communication between the stacked ICs is possible through the use of a hybridized backplane circuit, though the backplane is used primarily for readout. To date, the pixel pitch is typically 4 mils (100 microns) in both directions.

The Z-plane architecture has a severe cooling constraint. Though some heat sinking may be possible, electronic circuitry must minimize power dissipation. Thus, possible candidate circuit technologies are limited to CMOS and CCD, with CMOS being a more well-established choice. Analog CMOS can be realized either in continuous-time or with switched capacitors. The former, though useful in fixed, low dynamic range applications, is not of general use in image processing. Switched capacitor circuits have the advantage of operating in discrete-time which facilitates synchronization with external digital circuitry but requires significant real-estate for the implementation of ubiquitous operational amplifiers. For high throughput, the area requirements become excessive and dc power consumption is also increased.

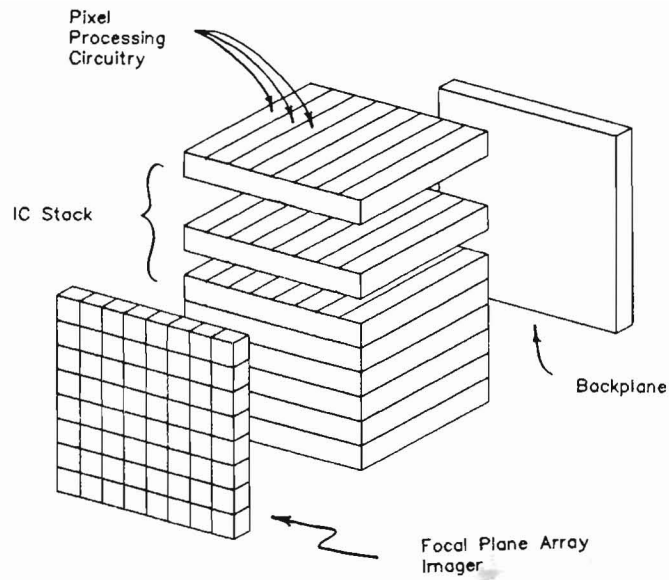

Fig. 1. Z-plane architecture.

Charge-coupled devices store signals as dynamic, analog charge packets residing in the semiconductor. For solid-state imagers, CCDs have become a major technology choice for read-out multiplexing. For signal processing, CCDs have the advantage of not needing operational amplifiers. They are compact in layout and of high bandwidth. For image processing, charge-coupled computing circuits based on the CCD technology offer the same advantages.[7] An important differentiation between conventional CCDs and charge-coupled computing circuits are that in the former, charge is transferred without modification and remains within the semiconductor. In the latter, modification of the signal is made and charge transfer takes place not only in the substrate but over metallic wires as well. In this case, constraints on circuit topology are relieved.

In this paper, three possible applications of the Z-plane architecture are described in which CCD technology might play a major role. These are non-uniformity compensation, neighborhood operations, and spatial-temporal image transformation.

NON-UNIFORMITY COMPENSATION

Solid-state imaging systems which use advanced materials suffer from significant spatial non-uniformities in detector responsivity and dark current. In infrared applications, the non-uniformity is of the order of 10% to 20%. Such non-uniformity is typically corrected (compensated) using off-chip digital hardware operating at very high speed with a commensurately large power dissipation. The compensation must take place prior to image processing to prevent erroneous results such as the detection of false edges. The Z-plane architecture provides the means for performing the non-uniformity compensation (NUC) in parallel prior to subsequent focal plane image processing. As described below, gain and offset ("two-point") compensation can be readily implemented using analog CCD circuits in a pipelined fashion.

Compensation need not be constrained to detector non-uniformity. Front-end analog circuitry performing functions such as pedestal removal or signal regeneration can be compensated as well. Thus, NUC can be considered as a correction for lumped-parameter non-uniformity, provided the lumped parameter system is well-behaved.

The general approach taken in this work is to use a multiplying digital-to-analog converter (MDAC) for both offset and gain compensation. The MDAC produces an analog signal which is the product of the input analog signal and digital word, in which the digital word represents a number between zero and one. For example, a 3 bit MDAC using the digital word 101_2 would multiply the analog signal by the amount (1/2 + 0/4 + 1/8) = 5/8. Fig. 2 schematically illustrates how the MDAC is used for compensation. The detector signal is fed to a first MDAC which performs gain adjustment. Offset adjustment is provided by using a second MDAC and a constant reference signal level. The two signals are summed to form the compensated signal.

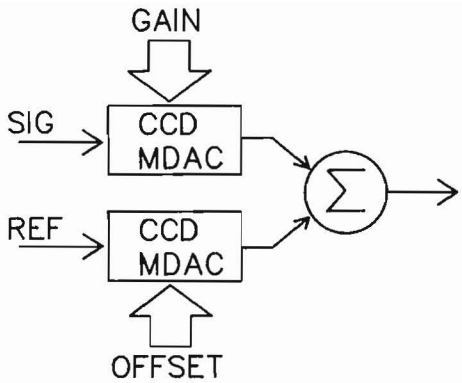

Fig. 2. MDAC approach to non-uniformity compensation.

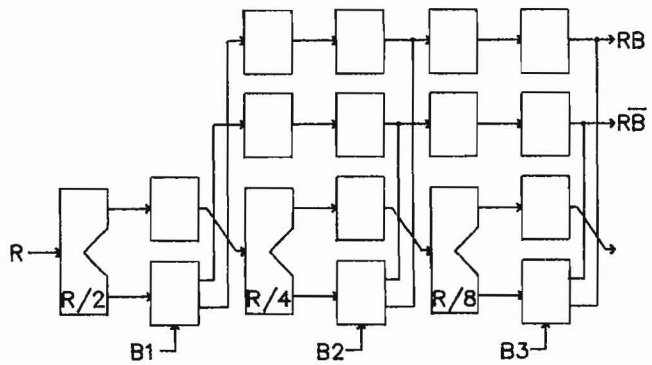

Fig. 3. Block diagram of CCD pipeline MDAC circuit.

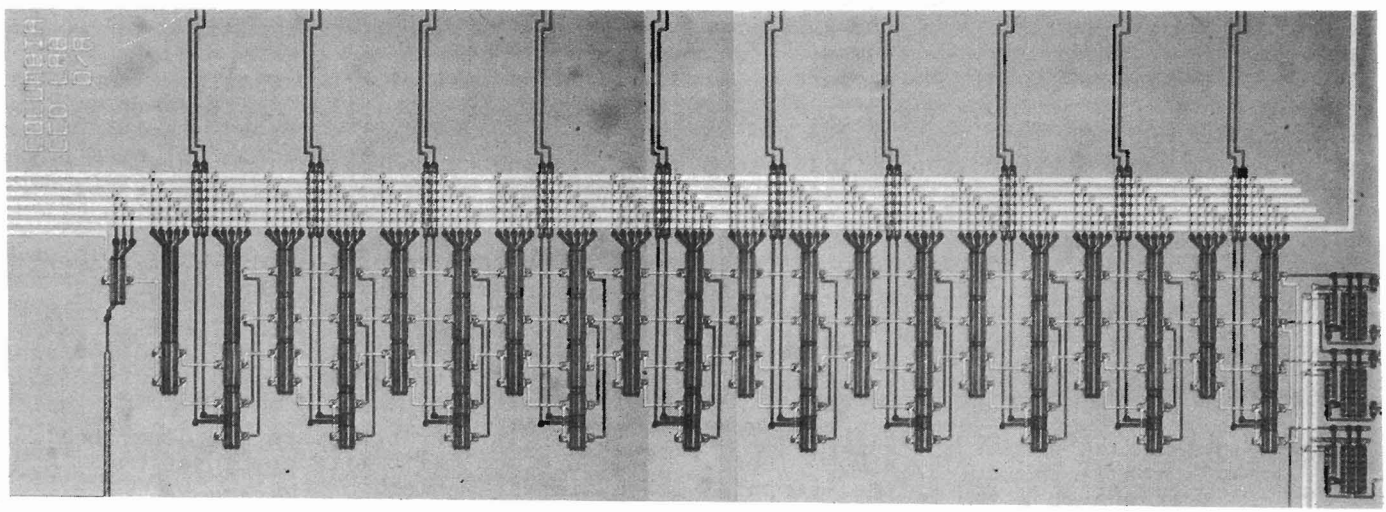

Fig. 4a. Experimental 10-stage CCD pipeline MDAC. Circuit size is approximately 0.03 x 0.14 mm^2.

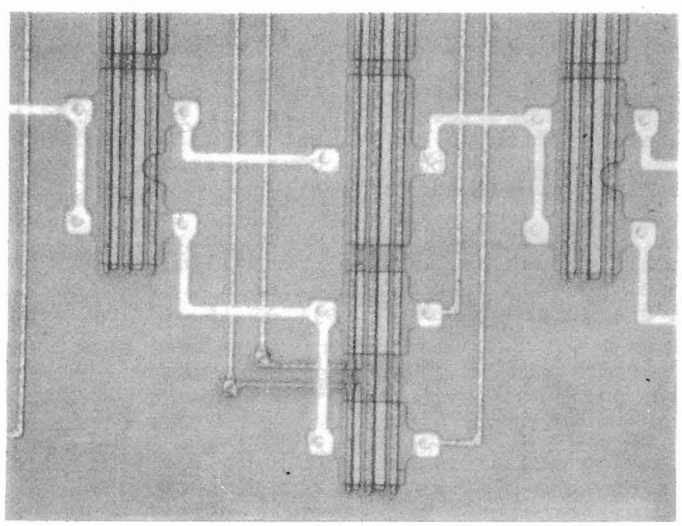

Fig. 4b. Detail of single CCD MDAC stage.

The MDAC can be realized in the charge domain in a number of ways. For example, charge packets of various sizes can be generated using input metering wells of varying size.[8] These packets can be conditionally generated depending of the value of the bits in the digital word. The charge packets are then summed to form the analog signal. The drawback with this approach is the limitation imposed by fabrication accuracy of the defined geometries, and the large real-estate required in order to realize both the least significant bit (LSB) and most significant bit (MSB) as geometric area ratios. An alternative approach to forming the charge packets is to generate them by successively splitting a reference charge packet in half. A CCD charge packet splitter with high accuracy and tolerant of alignment error has been described by Bencuya et al.[9] This symmetric splitter has accuracy in the 1 part in 1000 to 4000 range or 10 to 12 equivalent bits.

In an approach under development at Columbia, an MDAC circuit is formed by combining charge packet splitters with circuits for routing charge packets to one of two destinations. The destination is controlled by applying complementary digital signals to the router. A block diagram of the MDAC architecture is shown in Fig. 3. A charge packet reference signal (R) is input to the first stage splitter and one of the two halves (with value R/2) is transferred to the input of the second stage splitter after going through a buffer (delay) element. The other half is transferred to a router and the destination is one of two accumulating buffer elements. If the digital control bit (B1) is a logic one, the upper buffer is selected and this upper buffer chain accumulates the MDAC output charge packet. The alternate buffer (selected on logic zero) accumulates the complementary signal. The second stage commences with the splitting of R/2 into two R/4 portions followed by routing selected by a second control bit (B2). The output of the upper accumulating buffer is then seen to be given by:

$$Q_{out} = R \cdot (B_1/2 + B_2/4 + B_3/8 + \ldots + B_N/2^N)$$

where N is the number of stages in the MDAC, and $B = [B_1, B_2, B_3, \ldots B_N]$ is the digital gain word. The complementary output is simply $(R - Q_{out})$.

A 10-stage experimental MDAC circuit based on this architecture has been designed in the Columbia CCD Laboratory and fabricated by a CCD foundry. Testing of the device is currently in progress at Columbia. In Fig. 4a, a photograph of the experimental MDAC circuit is shown. A close-up view is shown in Fig. 4b.

For non-uniformity compensation on arrays with detector responsivity variations on the order of 10% to 20%, the gain multiplication factors predominately fall in the range of 0.9 to 1.1, implying under utilization of the MDAC gain compensation range. An improved strategy for gain compensation with increased resolution[10] is shown in Fig. 5. In this case, the detector signal is sent as before to a binary MDAC but additional splitting circuitry is appended to the signal chain. This splitter has a split ratio of 1:9 (in this example) and the two outputs are independently selected and summed using the switches labelled A and B. A second path from the detector signal is established which provides a second 1:9 splitter with input. The two outputs from this splitter are also independently selected using switches C and D and summed with the above signals.

For a given MDAC accuracy, the selection and summation circuitry described improves the compensation resolution significantly. For example, by closing switches A and D, the output is given by:

$$Q_{out} = Q_{sig} \cdot (0.9 + 0.1 B)$$

where B is the digital gain word with value less than one, and Q_{sig} is the input applied to both branches of the circuit. Alternatively, selection of switches A,C and D yields an output given by:

$$Q_{out} = Q_{sig} \cdot (1.0 + 0.1 B)$$

which provides for gain greater than one. Fewer bits are required in the digital word B in order to achieve the same gain resolution as in the case without a second branch. By choosing combinations of the four range switches (A,B,C,D), the range of the gain compensation circuitry can be adjusted for pathological detectors, as illustrated in Fig. 6.

In practice, calibration of the detector array for non-uniformity compensation would be performed a limited number of times in the array's lifetime, since non-uniformity is primarily dictated by material and geometry considerations which do not, in principle, drift with age. Typically, gain and offset values are calculated from calibration measurements, stored in programmable read-only memory (PROM) circuits, and then used in off-chip digital compensation circuitry. An iterative approach to finding optimum

compensation values may also be employed. In the case of the Z-plane NUC CCD circuitry, PROM circuits need to be integrated for long-term memory. It may also be possible, depending on the application, to utilize a portion of the Z-plane real-estate for on-board autocompensation circuitry.

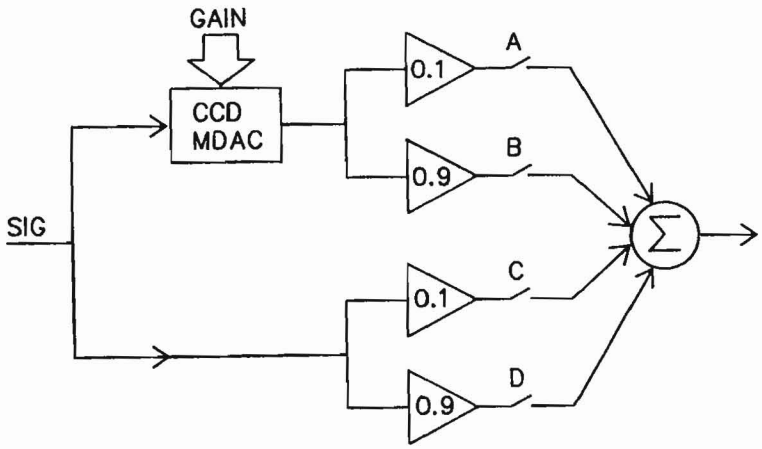

Fig. 5. MDAC gain compensation with improved resolution and range.

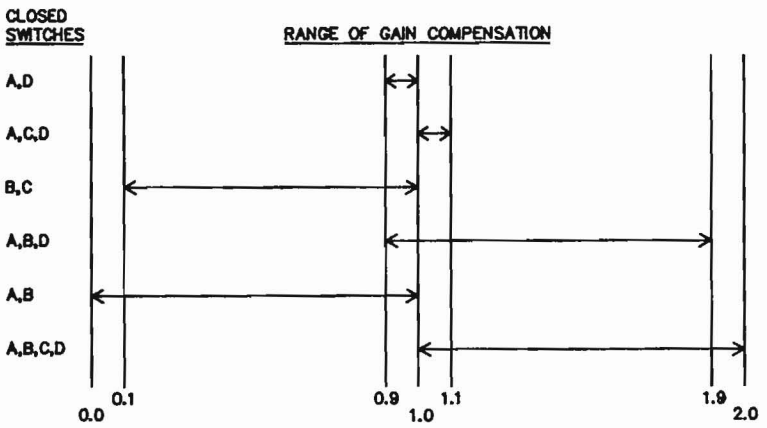

Fig. 6. Range of compensation for various switch settings.

NEIGHBORHOOD OPERATIONS

The Z-plane architecture, while providing additional real-estate for pixel processing circuitry, has the limitation of difficult nearest neighbor communication in one of the two imaging array directions (Y), since communication between stacked ICs is cumbersome and can consume significant power. This is unfortunate since many image processing functions can be cast as convolutions involving a local neighborhood of adjacent pixels. A compromise approach is to replicate the pixel data of each row and transmit the data once, in parallel through the backplane, to the adjacent row above it in the stack. A second replication and communication could be made to transmit to the row below. Storage of this neighbor data would be required within the real-estate associated with one pixel. Once captured, the neighborhood data could be used to perform the convolution functions. Since convolution involves multiplying the neighborhood by a fixed weight kernel, the MDAC architecture could be used again for this function.

Increased flexibility can be obtained by using a fully programmable approach. An example of this is the use of charge-coupled computing circuits to form a charge-coupled computer. Such a computer is currently under exploration at Columbia for monolithic spatially parallel focal plane image processing[5]. This chip, named IRET, consists of a 24 x 24 array of pixel processors formed as charge-coupled computers. Each processor serves four photodiodes, making the imager array 48 x 48. The photodiodes are located on a 180 um pitch with a total IC size of 9.4 mm x 9.4 mm. One of the 576 pixel processors on the IRET chip (currently in fabrication/testing) is shown in Fig. 7.

Each processor consists of a differencer circuit, a splitter, a charge packet comparator, a second differencer enabled on the output of the comparator, a bidirectional stack for short-term memory/accumulator functions, and a transceiver for nearest neighbor communication. The processor array is digitally programmable using external clocking signals as a single-instruction, multiple data (SIMD) parallel architecture. The total internal throughput of IRET is designed for 576 million operations per second corresponding to image processing at the rate of 1000 frames per second with a total power dissipation under 25 mW. However, the array output is multiplexed so that serial data output represents the IC bottleneck. If the chip operates as expected, real-time image processing functions such as edge detection and thresholding may be readily achieved at 50 Hz frame rates with minimal power dissipation.

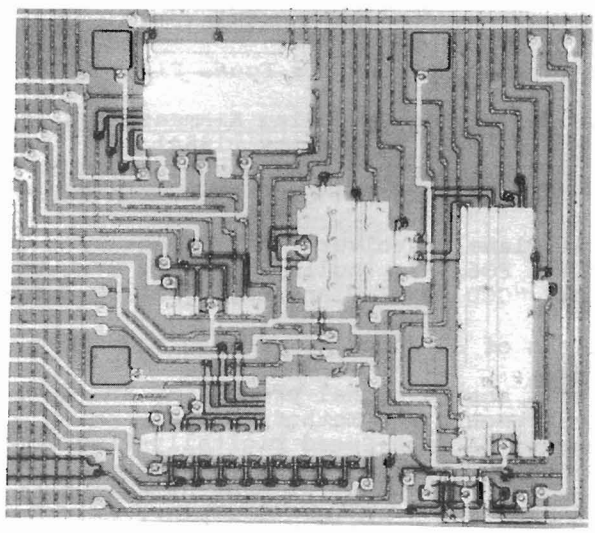

Fig. 7. IRET unit cell with four photodiodes. Unit cell size is 360 x 360 um^2.

SPATIAL-TEMPORAL IMAGE TRANSFORMATION

In addition to the convolution architecture offered by the MDAC approach and the non-linear processing offered by an IRET-like approach, a truly novel application for the Z-plane architecture is proposed. In this application, temporal buffering of successive frames through the use of conventional CCD shift registers is suggested. On each IC of the Z-plane stack, a CCD array with parallel input can be formed. However, instead of the usual X-Y data format, the array will contain X-t data and be shifted in the t (time) direction.

The temporal data might be used in a number of ways. For example, event detection, motion detection and object tracking all require multiple frame operations. Image compression is another important application which can benefit from the temporal buffering of data. Recently, a new image transform for lossless transmission of compressed images was described by Torbey and Meadows[11]. This transform relies on the correlation between adjacent pixels values in the X-Y plane to improve an image intensity histogram for Huffman coding. Typically, an 8 bit pixel image can be encoded with an average of 4.5 bits per pixel using this transform without loss. However, temporal correlation of "adjacent" pixels in the X-t array may be expected to exceed that of an X-Y array, provided that there is not rapid motion in the majority of the image. Use of the Z-plane architecture to achieve such a spatial-temporal transform seems natural. It can be anticipated that realization of such a spatial-temporal transform would require the integration of analog CCD circuitry with digital CMOS control and logic circuits. Recent simulation[12] indicates that additional lossless compression of the image by one to two bits per pixel may be achieved using a spatial-temporal version of the above transform, depending upon the degree of motion in the image. (The same 10 second teleconferencing sequence was used for the simulation in both the X-Y case and the X-t case described above.)

CONCLUSIONS

The Z-plane architecture, while approaching manufacturing viability, has potential for performing unique image processing functions. This paper has discussed three of these which are well-suited to CCD implementation. These are non-uniformity compensation using a CCD MDAC architecture, image convolution using CCD MDAC circuits for weighting the neighborhood or using a general programmable processor such as that in IRET, and a spatial-temporal transform for image compression. The use of the time domain for image compression and processing is an under-explored opportunity for future research, and seems to have high potential for extending the range of application of the Z-plane architecture.

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