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NEW CHARGE-COUPLED DEVICES AND CIRCUITS
FOR ANALOG VLSI FOCAL-PLANE IMAGE PROCESSING

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ABSTRACT

A new approach to designing low-power, compact, charge-coupled device (CCD), analog, VLSI circuits for signal processing is described. A charge domain wire transfer circuit allows the coupling of CCD circuits through the use of a metallic wire. The approach trades charge transfer efficiency for design simplicity. The impact of wire transfer on CCD circuit design is addressed. Charge-coupled computing circuit building blocks are discussed. Circuits utilizing wire transfer are described and include a general purpose charge-coupled computer, an A/D converter, a D/A converter, and a focal-plane image processor chip.

It has been remarked that CCD circuits, unlike transistor circuits, must be monolithically integrated to function. Unfortunately, confinement of the signal charge to the semiconductor inhibits the implementation of circuit topologies in which signal lines cross, a major limitation. Furthermore, such intimate integration makes a building block approach to circuit design difficult to achieve. This paper describes a technique to relieve this constraint and allow a building block design methodology. The technique, called wire transfer, is a hybridization of CCD and bucket brigade charge transfer, and permits the topological crossing of signal lines and a building block approach to CCD design.

WIRE TRANSFER

INTRODUCTION

Charge-coupled devices (CCDs) operate in the analog charge domain and are typically used for solid-state imager read-out and for some signal processing functions. The signal charge is readily transferred within the semiconductor using electrode-induced electrostatic potential wells with charge-transfer efficiency (CTE) approaching 0.999999 in state-of-the-art devices. CCDs, since inception, have predominately found application in circuits involving shift register type operations. While image readout requires very high transfer efficiency to maintain image integrity, several signal processing applications are less susceptible to the effects of lower CTE. One of these is focal-plane image processing, which is the integration of image acquisition and image processing functions on the same chip. Charge-domain circuits are well-suited for focal-plane image processing due to their compact layout, low power dissipation, and discrete time operation.¹

Background

In traditional CCD charge transfer, charge carriers are physically transported from one bucket to the next adjacent one. In wire transfer, a quantity of charge is transferred from one bucket to a second bucket physically removed in distance. The transfer takes place through the use of a conductor (i.e. infinite sea of carriers) so that only the quantity of charge is conserved. There are several possible approaches to this operation. For example, the charge can be transduced into a voltage, and the voltage subsequently used to regenerate a copy of the charge packet. A source-follower circuit could be used in this approach but would consume significant power and suffer from threshold voltage variations. (If the wire interconnect capacitance is high, such an approach becomes more palatable.) A second approach is to use a charge-domain charge packet replicator circuit.² However, the linearity and gain of the replication process deteriorates rapidly with increasing stray wiring capacitance and requires real-estate and clock cycles for reset/generation phases.

Operation

The new wire transfer circuit requires minimal power and real-estate, but also presupposes a low interconnect capacitance. The wire transfer circuit is shown schematically in Fig. 1. Two short CCD registers are shown connected by diffusions and a wire interconnect. Initially, in the left (or output) register is a charge packet Q_{sig} that is to be transferred to the bucket in the right (or input) register. Note that the initial voltage on the diffusion nodes is exactly that corresponding to pinchoff of the channel under the first electrode of the input register (first barrier gate). The first barrier gate is biased approximately one to two volts above threshold; the exact biasing is not critical provided it is well established. The second barrier gate is biased slightly higher than the first. The third gate is biased to form a receiving bucket for the signal charge.

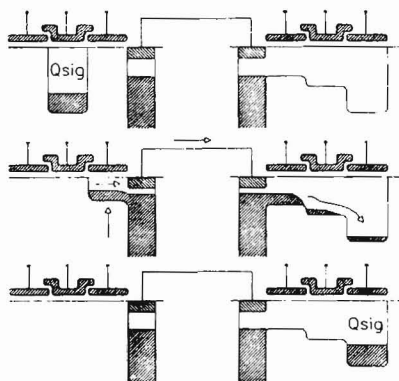


Fig. 1. Illustration of wire transfer.

First, the signal charge is transferred from the second electrode of the output register to the third. Next, the third electrode (or output transfer gate) voltage is ramped at a constant dV/dt to eject the charge from under it. As the bucket collapses, the potential on the diffusion becomes sufficient to turn-on the channel under the first barrier gate. Charge is then injected under the two barrier gates and collected in the receiving bucket. After an initial short transient time, the injected current is constant at a level approximately given by $C_B dV/dt$, where C_B is the bucket capacitance of the output transfer gate. For the circuits considered below, this current is of the order of 100 μA and requires a change in diffusion node voltage of the order of 0.5 volts to provide a matching injection current to the receiving bucket.

The rate limiting process for wire transfer occurs once the output transfer gate is fully ramped so that no signal charge remains under it. At this time, the current source is shut off and the diffusion node discharges by means of the current under the first barrier gate. The driving voltage for this discharge is the node voltage itself and the node discharges slowly with a time constant that scales with node capacitance. To minimize this transfer rate limiting effect, the node capacitance must be kept small. At the end of the wire transfer interval, the diffusion node voltage returns to its initial value. It follows then, that an amount of charge exactly equal to Q_{sig} has been injected into the receiving bucket.

The wire transfer process described above is similar in nature to that found in bucket brigade devices.³ However, in bucket brigade devices, the junction capacitance is used for signal storage and is intentionally large, implying a relatively large node capacitance and slow characteristic transfer times. Indeed, bucket brigade devices typically operate at 10-100 kHz. Furthermore, in the wire transfer circuits, the second barrier gate provides a screening function against lowering of the first barrier by charge storage in the receiving well.

Transfer efficiency in wire transfer is excellent for large charge packets, and poorer for very small packets. In the latter case, the constant current source model fails. Subthreshold current allows the diffusion node to discharge beyond its initial condition. Under these circumstances, a portion of a succeeding charge packet is lost in restoring the node to its quiescent voltage. In the circuits described below, a conservative upper bound for the worst case charge packet loss is approximately 0.3% of a full bucket corresponding to a worst case CTE of approximately 0.997. This value has been experimentally confirmed, though the use of a "fat-zero" significantly improves the CTE.

Discussion

Wire transfer provides for modest CTE at high transfer rates. Most importantly, it provides for the transfer of charge domain signals across wires, thereby allowing signal processing circuit topologies in which signals cross each other, an important advantage. Wire transfer may be used for connecting multiple nodes together. Charge transferred into the connected nodes is summed. Several receiving buckets may be connected together, with the barrier gates

on all but one turned off. This allows routing of a charge packet to one of several receiving buckets with negligible loss in transfer speed. This is a very useful task in signal processing circuitry and difficult to achieve with conventional CCDs.

CCD BUILDING BLOCKS

With wire transfer, a building block approach to CCD computing circuit design becomes feasible. The layout of each block begins with a wiring node, input diffusion, dual barrier electrodes and a receiving bucket. Each block layout ends with an output transfer gate, an output diffusion, and an output wiring node.

A simple buffer block has no other components in between. (If the barrier gates are to be dc biased, another electrode is required to prevent backflow of signal charge.)

A router block has two buffer blocks connected in parallel, but with complementary barrier electrodes such that one of the two electrode pairs permits charge transfer. In this case the node capacitance is somewhat larger and transfer speed reduced.

A splitter block is similar to a buffer block, but a field isolation pattern forming a split in the channel in the transfer direction is utilized to split the input charge packet into two components. The splitter block thus has two output diffusions and wiring nodes.

A charge input block has no wire transfer input node, rather the input diffusion is used for fill and spill charge packet generation.

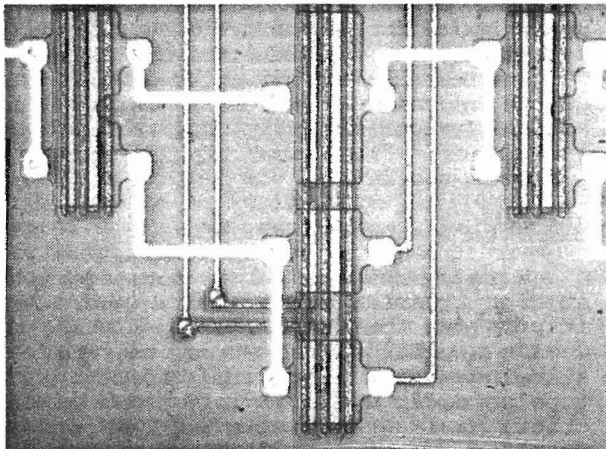


Fig. 2. Photograph showing splitter block, buffer and router blocks, and a second splitter block.

A floating gate sense amplifier block has a floating gate between input and output electrode structures. The voltage shift induced on the floating gate can be used for a variety of functions including output. To improve operation, the floating gate is reset prior to charge input, and shunted to a second supply voltage to eject the charge packet after the sense operation is complete.

CIRCUITS

Wiring of building blocks should be implemented with a minimum of wiring capacitance, or with recognition that increased capacitance decreases transfer speed. Although wire transfer lines can cross each other, they should not cross clock lines unless shielded to prevent clock feedthrough. The blocks can be wired together to perform a variety of functions. Several CCD circuits have been designed for 20 nsec clock widths using this building block approach. Fabricated at a commercial CCD foundry using a double-poly, double-metal process, they are currently under test in the Columbia CCD Laboratory.

CHAMP

A test vehicle for exploring these ideas is the CHAMP (charge manipulation processor) circuit. This circuit contains the blocks described above and includes a floating diffusion (destructive) output amplifier and a comparator circuit.⁴ The latter is basically a flip-flop preset according to two input charge packets. The blocks are connected to a single bus line (an analog "unibus") and all signal communication takes place over this line. Such a circuit is a charge-coupled computer. A photo of CHAMP is shown in Fig. 3.

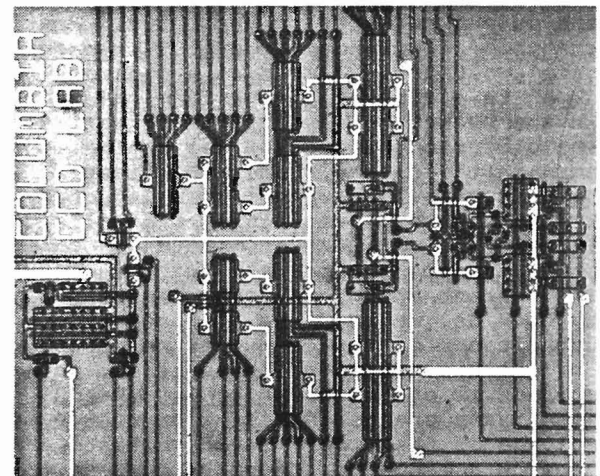


Fig. 3. CHAMP test vehicle.

SAND

A simple successive approximation A/D converter chip (SAND) has been designed and fabricated. It consists of two floating gate sense amplifiers which feed a comparator circuit. In each cycle of the A/D conversion process, successively smaller charge packets are routed to one of the two floating gate amplifiers, depending upon the previous state of the comparator. By generating these packets using a symmetrical charge packet splitter, reference charge packets of size $Q_m/2^n$ (n is the cycle number) are produced. The resultant comparator output represents the digital bits of the conversion.

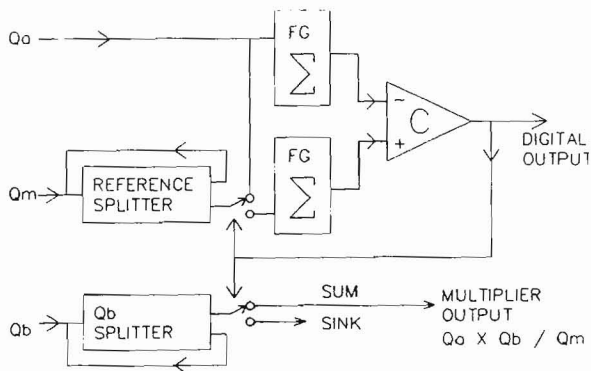


Fig. 4a. Block diagram of A/D-D/A chip.

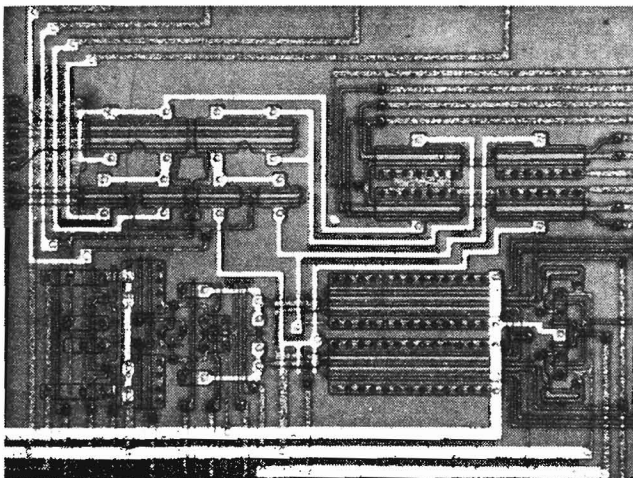


Fig. 4b. Photograph of SAND circuit.

The A/D converter is designed with a slave D/A converter. The slave D/A works by successively summing reference charge packets of size $Q_b/2^n$. Some of these packets are discarded, according to the A/D comparator output. The total circuit size is approximately 200 μm x 300 μm and

is designed to perform 8-bit conversion at 10^6 conversions/second with a power consumption estimated to be under 1 mW. A block diagram of the SAND circuit is shown in Fig. 4a, and a photograph in Fig. 4b.

The A/D and D/A conversion processes can also be performed using pipeline circuits. These circuits, designed and fabricated for 10 bit conversion at 10^7 conversions/sec, consume approximately 10 times the power and real-estate of the serial circuit described above.

IRET

A focal plane image processor chip (IRET) has been designed and fabricated.⁵ IRET is a general purpose, fully programmable SIMD (single instruction, multiple data) architecture consisting of a 24 x 24 array of analog, charge-domain, pixel processors. Each of the 576 processors services four integrated photodiodes, located on a 180 μm pitch. Designed for functions such as smoothing, thresholding, edge detection, and motion detection, each processor has CCD circuits for multiplexing the four photodiodes, a bidirectional stack with 8 storage sites, a charge packet splitter, differencer,² a magnitude comparator, a charge packet differencer enabled by the output of the comparator, and I/O circuitry for nearest neighbor data exchange. The circuits within each processor are connected by a common bus, as in the case of CHAMP. Although this increases the bus capacitance significantly, the relative speed requirements in IRET are low due to the high degree of parallelism. It is estimated that for image processing tasks requiring of the order of one hundred operations per pixel, IRET can achieve an internal throughput of 1000 frames/sec. However, output from IRET is performed using a parallel-to-serial shift register, which is a major bottleneck. Processed image frame rates of 100 frames/sec are expected to be readily achieved. The IRET chip size is 9.4 x 9.4 mm^2 , and is expected to dissipate less than 1 mW. A block diagram of the IRET unit cell is shown in Fig. 5a and a photograph in Fig. 5b. A photograph of the complete IRET chip is shown in Fig. 6.

SUMMARY

A new approach to CCD circuit design has been presented. This approach relies on the use of wire charge transfer, trading transfer efficiency for design simplicity. Analog VLSI CCD circuits have been designed using this principle and show promise for implementation of focal-plane image processing functions.

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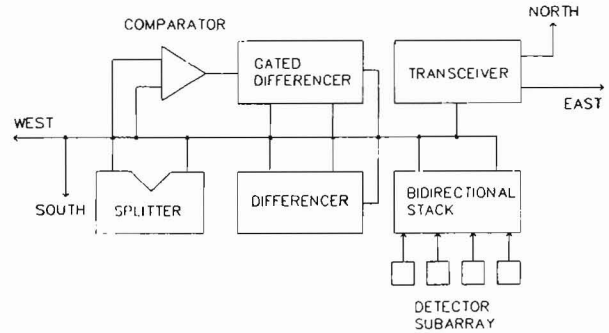


Fig. 5a. Block diagram of IRET unit cell.

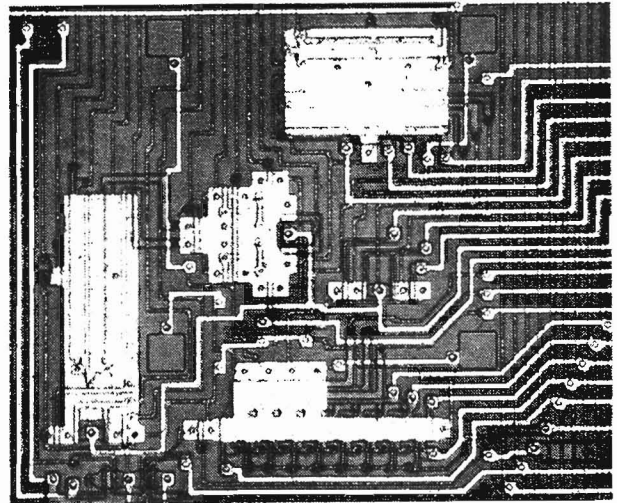


Fig. 5b. Photograph of IRET unit cell. Cell size is 360 μm x 360 μm .

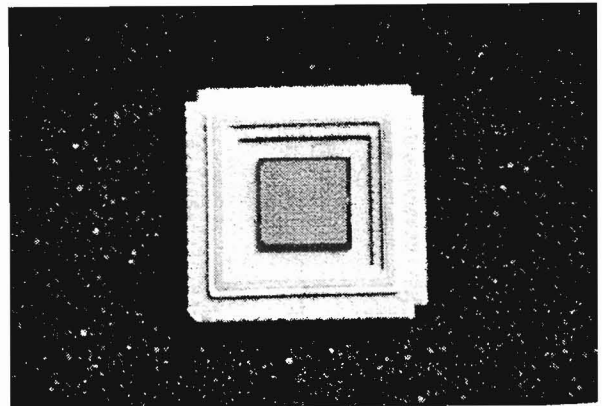


Fig. 6. Photograph of IRET focal-plane image processor chip. Chip size is 9.4 mm x 9.4 mm and contains 576 pixel processors and 2304 photodiodes.