Low-Energy Ion Beam Oxidation of Silicon

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Abstract—**A low-energy oxygen ion beam with energy below 100 eV has been applied to the oxidation of unheated silicon substrates. Ultrathin (~45 Å) FET-gate-quality oxides have been produced for the first time at room temperature using this technique. The high electrical quality of the oxides is demonstrated by the successful fabrication of n-channel MOSFET's.**

I. Introduction

THE requirements for increased performance and decreased dimension of semiconductor devices have necessitated the development of low-temperature fabrication processes such as ion implantation, rapid thermal annealing, and laser photochemical direct-writing processes. Repeated high-temperature processing leads to impurity redistribution, generation of stacking faults, wafer warpage, and oxidation-enhanced diffusion which hinder the performance of small-dimension devices.

Oxidation of silicon is critical to the fabrication process and a variety of reduced-temperature oxidation processes (e.g., plasma oxidation [1] and anodization, plasma-enhanced CVD, photo-activated CVD, sputter deposition in an oxygen ambient [2], and other techniques) have been applied to steps requiring a thick oxide. However, most of these processes fail to yield oxides suitable for use as a gate dielectric, though recently 600°C plasma oxidation has been successfully applied to MOSFET fabrication [3]. To date, high-temperature thermal oxidation remains the most viable means of producing high-quality gate dielectrics.

Ion beam oxidation was first explored for oxidation of Nb using 600-eV oxygen ions to fabricate Josephson tunnel junctions [4]. Oxygen ion beams with energies as low as 45–80 eV have been used in ion-beam oxidation of Ni and Cr [5] and in near-threshold reactive sputtering of copper and silicon [6]. A focused ion beam has been used in conjunction with photoelectron spectroscopy to study the growth of oxide films on silicon (111) [7]. In this paper, we report the use of a broad low-energy oxygen ion beam for the fabrication of MOS gate oxides in silicon at room temperature.

II. Experimental Procedure

The samples are fabricated on p-type (100) 10-Ω·cm silicon wafers, 5-cm diameter, polished on one side. The wafers are cleaned chemically and by growing an initial wet oxide. High-temperature (1050°C) diffusions through wet oxide masks using spin-on sources are used to define the p^+ isolation and n^+ source and drain junctions. A final 5000-Å field oxide is grown in steam at 1000°C. Windows are etched in the field oxide using a standard buffered oxide etchant (BOE). Immediately before ion beam oxidation the samples are dipped in cold dilute HF and dried.

The gate oxide is grown by bombarding the exposed silicon surface with a composite argon–oxygen ion beam produced by a 2.5-cm beam diameter single-grid Kaufman-type source.[1] The bell jar is evacuated to a base pressure of 3×10^{-7} torr. Argon and oxygen gases are introduced into the source in the desired ratio, determined by monitoring their flow rates. The working pressure in the vacuum chamber is 3×10^{-4} torr. The ion beam is extracted through a negatively biased accelerating grid and neutralized by a thermionic filament whose electron emission is adjusted to yield a net neutral beam. The target is positioned on an electrically grounded temperature-controlled substrate holder 15 cm from the source.

The ions are created in an $Ar–O_2$ discharge with discharge voltage $V_D = 36$ V and discharge current $I_D = 0.6$ A. Their energy is determined by the 60-V potential at which the entire source is maintained. A total beam current $I_B = 58$ mA (maximum current density $J_B = 75\ \mu A/cm^2$) is extracted by an accelerating voltage $V_A = -20$ V. The initial oxygen-to-argon flow rate ratio is 1:7 and is increased to 1:1 during the course of the run. The sample is exposed to the beam for 6 min. The sample temperature is 28°C as indicated by a substrate-holder mounted thermocouple. The temperature is observed to rise 5°C during the exposure.

Following ion beam oxidation, source and drain contact windows are opened through the gate oxide and 3000 Å of aluminum is thermally evaporated and patterned. Another 3000 Å of aluminum is evaporated on the backside of the wafer to complete the process.

Measurements are performed both before and after a brief post-metallization anneal, carried out at 400°C in N_2 for 3 min.

III. Results and Discussion

The CV and $I–V$ characteristics of a MOS capacitor fabricated by low-energy ion beam oxidation before and after post-metallization annealing are shown in Fig. 1(a) and (b). The flat-band voltage calculated from the accumulation capacitance prior to annealing is $V_{FB} = -0.95$ V and improves to $V_{FB} = -0.6$ V after annealing. This flat-band

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[1] Ion Tech, Inc., Fort Collins, CO.

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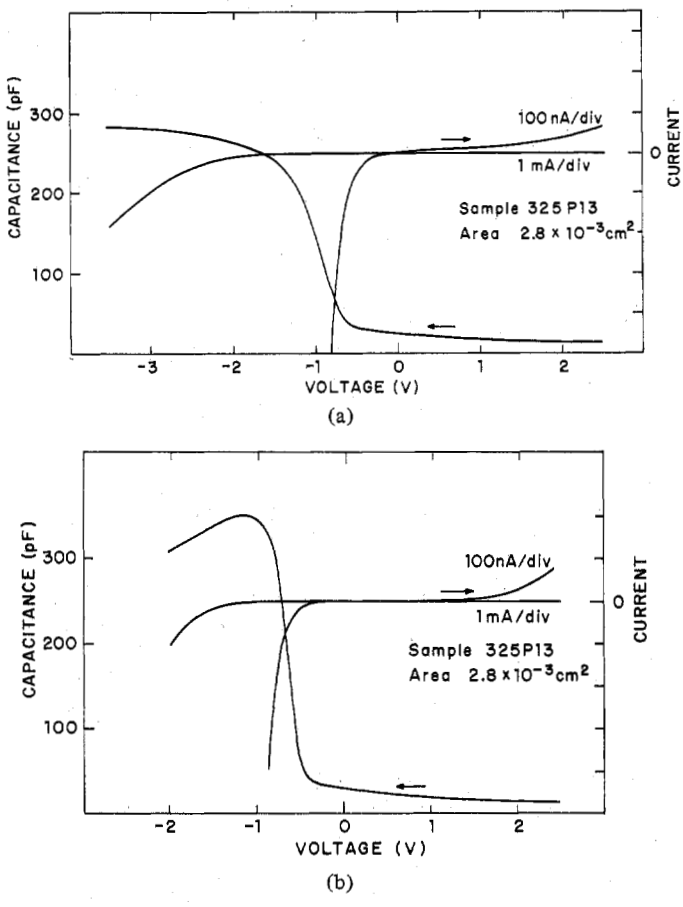

Fig. 1. Capacitance–voltage and current–voltage characteristics of an MOS capacitor fabricated using room-temperature low energy ion beam oxidation. (a) as grown. (b) With post-metallization anneal in N_2 for 3 min at 400°C. Ion energy: 60 eV. O_2 partial pressure: 6.4×10^{-5} torr. Time: 6 min.

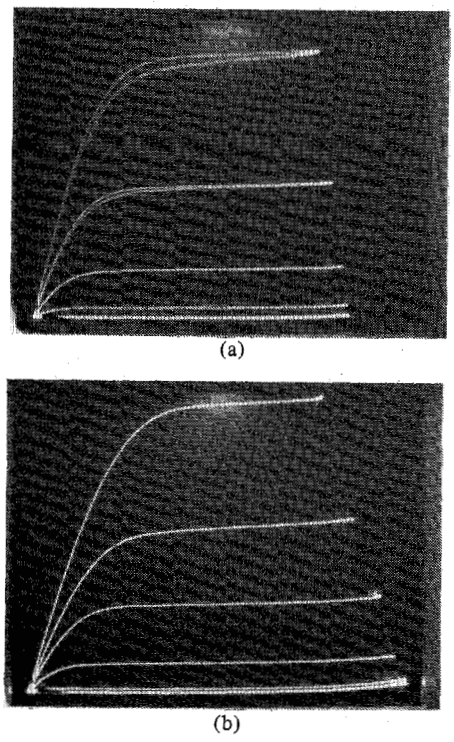

Fig. 2. Current–voltage characteristics of an n-channel MOS transistor with gate dielectric produced at room temperature using a low energy ion beam. (a) as grown—horizontal: 0.2 V/div; vertical: 20 μA/div, 0.2 V/step. (b) With post-metallization anneal in N_2 for 3 min at 400°C—horizontal: 0.2 V/div; vertical: 50 μA/div, 0.2 V/step. Ion energy: 60 eV. Variable O_2 partial pressure. Time: 6 min.

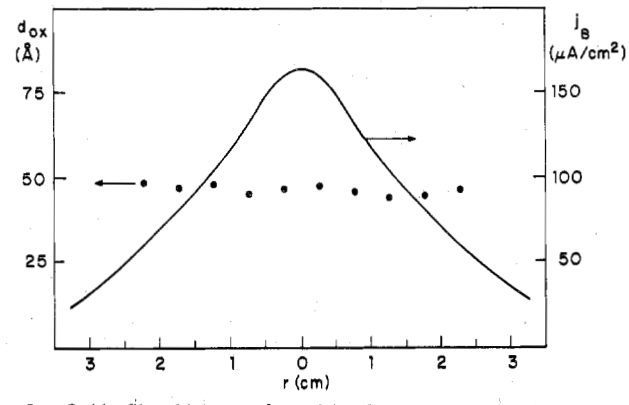

Fig. 3. Oxide film thickness d_{ox} and ion beam current density profile j_b. Current density probe diameter: 1.13 cm. Oxygen partial pressure: 6.4×10^{-5} torr. Ion energy: 60 eV. Accelerating voltage: −20 V. Time: 6 min.

voltage shift may be due partly to damage caused by the ion bombardment and partly to a not-fully-neutralized ion beam. Although the inversion layer charge begins to leak through the oxide at a relatively low applied voltage, the gate leakage current is at least 2×10^3 times lower than the source–drain saturation current at the same applied gate voltage, and thus does not degrade MOSFET performance.

The thickness of the produced oxide layer is 45 Å as measured by ellipsometry. This agrees with a controlled etch-time measurement in cold BOE and Auger sputter profiling. The index of refraction of ion beam-grown oxides is measured to be higher than that for thermally grown SiO_2 films of the same thickness. Also, the oxide capacitance is observed to be lower than that anticipated for a 45-Å oxide. These facts indicate that the film is probably not stoichiometric SiO_2 or that the surface of the Si substrate has been damaged by the ion bombardment.

The characteristics of a room-temperature gate-oxide MOSFET before and after post-metallization annealing are shown in Fig. 2(a) and (b). On the basis of the accumulation capacitance the mobility of the produced MOSFET's prior to annealing is calculated to be 400 $cm^2/V \cdot s$ and is observed to improve by a factor of two after annealing. The threshold voltage is 0.45 and 0.38 V before and after annealing, respectively. The breakdown strength of the gate oxide is 7×10^6 V/cm.

The uniformity of the device characteristics across a large area of the substrate is much better than the uniformity of the ion beam, as shown in Fig. 3. This indicates, to first order, dose independence of the produced oxide films.

IV. Summary

Thin gate-quality dielectrics of uniform thickness have been produced at room temperature on p-type Si wafers. These have been successfully used for fabricating n-channel MOSFET's. The ion bombardment may cause some radiation damage at the

surface but post-metallization annealing at 400°C significantly improves the device characteristics. The electrical properties of the films are of sufficiently high quality to allow their use as gate dielectrics in thin-film MOSFET's.

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