

# Low Power Camera-on-a-Chip Using CMOS Active Pixel Sensor Technology

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## Abstract

A second generation image sensor technology has been developed at the NASA Jet Propulsion Laboratory as a result of the continuing need to miniaturize space science imaging instruments. Implemented using standard CMOS, the active pixel sensor (APS) technology permits the integration of the detector array with on-chip timing, control and signal chain electronics, including analog-to-digital conversion. This paper describes the technology for implementing a low power camera-on-a-chip.

## Introduction

Imaging system technology has broad applications in commercial, consumer, industrial, medical, defense and scientific markets. The development of the solid-state charge-coupled device (CCD) in the early 1970's led to relatively low cost, low power, and compact imaging systems compared to vidicons and other tube technology. The CCD uses repeated lateral transfer of charge in a MOS electrode-based analog shift register to enable readout of photogenerated signal electrons. High charge transfer efficiency (signal fidelity) is achieved using a highly specialized fabrication process that is not generally CMOS compatible. Separate support electronics are needed to provide timing, clocking and signal chain functions. CCD based camcorder imaging systems typically operate for an hour on an 1800 mA-hr 6 V NiCad rechargeable battery, corresponding to 10.8 W of power consumption. Of this, approximately 8 W is dissipated in the imaging system and the rest is used by the tape recording system, display, and autofocus servos. Space-based imaging systems, operating at lower pixel rates, but with a lower degree of integration, typically dissipate 20 W or more.

CCDs, which are mostly capacitive devices, dissipate little power. On-chip dissipation arises mostly from the source-follower amplifier. Biased at a drain voltage of perhaps 24 V, the buried channel source-follower dissipates approximately 10-20 mW. The major power dissipation in

a CCD system is in the support electronics. The CCD, as a chip-sized MOS capacitor, has a large C and requires large clock swings,  $\Delta V$ , of the order of 5-15 V to achieve high charge transfer efficiency. Thus, the  $C\Delta V^2 f$  clock drive electronics dissipation is large. In addition, the need for various CCD clocking voltages (e.g. 7 or more different voltage levels) leads to numerous power supplies with attendant inefficiencies in conversion. Signal chain electronics that perform correlated double sampling (CDS) for noise reduction and amplification, and especially analog to digital converters (ADC), also dissipate significant power.

## CMOS Active Pixel Sensors

### Operation

In an active pixel sensor, both the photodetector and readout amplifier are integrated within the pixel [1]. The voltage or current output from the cell is read out over X-Y wires instead of using a shift register. JPL has developed a CMOS active pixel sensor using standard CMOS technology that has achieved nearly the same performance as a CCD image sensor [2]. The use of CMOS permits ready integration of on-chip timing and control electronics, as well as signal chain electronics. Analog to digital conversion can also be integrated on chip. Such a highly integrated imaging system is referred to as a camera-on-a-chip, and represents a second generation solid state image sensor technology.

A block diagram of a CMOS active pixel circuit is shown below in Fig. 1. Incident photons pass through the photogate (PG) and generated electrons are integrated and stored under PG. For readout, a row is selected by enabling the row select transistor (RS). The floating diffusion output node (FD) is reset by pulsing transistor RST. The resultant voltage on FD is read out from the pixel onto the column bus using the in-pixel source follower. The voltage on the column bus is sampled onto a holding capacitor by pulsing transistor SHR. The signal charge is now transferred to FD by pulsing PG low. The

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voltage on FD drops in proportion to the number of photoelectrons and the capacitance of FD. The new voltage on the column bus is sampled onto a second capacitor by pulsing SHS. All pixels in a selected row are processed simultaneously and sampled onto capacitors at the bottom of their respective columns. The column-parallel sampling process typically takes 1-10  $\mu$ sec, and occurs in the so-called horizontal blanking interval.

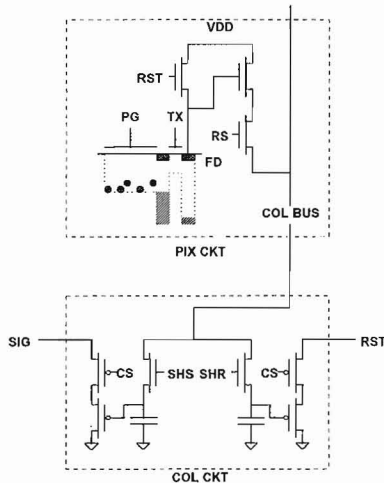


Fig.1. CMOS APS pixel circuit (upper) and column circuit (lower). Load transistors not shown.

For readout, each column is successively selected by turning on column selection p-channel transistors CS. The p-channel source-followers in the column drive the signal (SIG) and horizontal reset (RST) bus lines. These lines are loaded by p-channel load transistors, not shown in Fig. 1. The lines can either be sent directly to a pad for off-chip drive, or can be buffered.

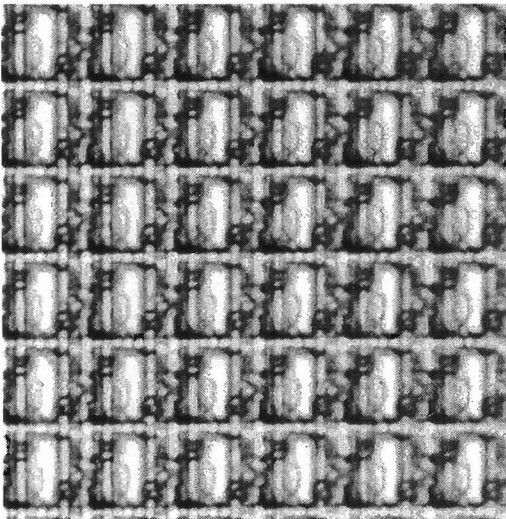


Fig. 2. CMOS APS pixels.

### Noise

Noise in the sensor is suppressed by the correlated double sampling (CDS) of the pixel output just after reset, before and after signal charge transfer to FD. The CDS suppresses kTC noise from pixel reset, suppresses 1/f noise from the in-pixel source follower, and suppresses fixed pattern noise (FPN) originating from pixel-to-pixel variation in source follower threshold voltage. kTC noise is reintroduced by sampling the signal onto the 1-4 pF capacitors at the bottom of the column. Typical output noise measured in CMOS APS arrays is of the order of 140-170  $\mu$ V r.m.s. Output-referred conversion gain is typically 7-11  $\mu$ V/e-, corresponding to noise of the order of 13-25 electrons r.m.s. This is similar to noise obtained in most commercial CCDs, though scientific CCDs have been reported with read noise in the 3-5 electrons r.m.s.

### Power

Typical biasing for each column's source-follower is 10  $\mu$ A permitting charging of the sampling capacitors in the allotted time. The source-followers can then be turned off by cutting the voltage on each load transistor (not shown in Fig.1.) The horizontal blanking interval is typically less than 10% of the line scan readout time, so that the sampling average power dissipation  $P_s$  corresponds to:

$$P_s = n I V d \quad (1)$$

where n is number of columns, I is the load transistor bias, V is the supply voltage, and d is the duty cycle. Using n=512, I=10 $\mu$ A, V=5V and d=10%, a value for  $P_s$  of 2.5 mW is obtained.

To drive the horizontal bus lines at the video scan rate, a load current of 1 mA or more is needed. The power dissipated is typically 5 mW.

### Quantum Efficiency

Quantum efficiency measured in CMOS APS arrays is similar to that for interline CCDs, and a typical curve is shown in Fig. 3. One interesting observation is that the quantum efficiency reflects significant responsivity in the "dead" part of the pixel containing the readout circuitry, as measured by intra pixel laser spot scanning [3]. This is because while the transistor gate and channel absorb photons with short absorption lengths (i.e. blue/green), longer wavelength photons penetrate through these regions and the subsequently generated carriers diffuse laterally to be collected by the photogate. Thus despite a fill factor of 25%-30%, the CMOS APS achieves quantum efficiencies that peak between 30%-35% in the red and near infrared. Microlenses can be added to improve quantum efficiency.

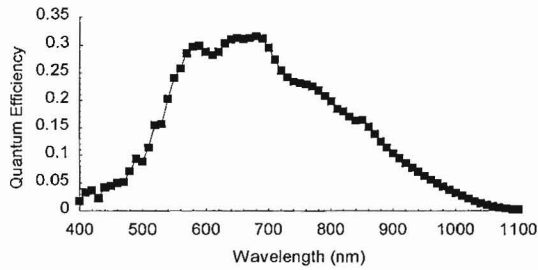


Fig. 3. Typical quantum efficiency of a CMOS APS pixel.

### On-Chip Timing and Control

Integration of on-chip timing and control circuits has been demonstrated in both 128x128 and 256x256 arrays [4]. A block diagram of the chip architecture is shown in Fig. 4. The analog outputs are VS\_OUT (signal) and VR\_OUT (reset), and the digital outputs are FRAME and READ. The inputs to the chip are asynchronous digital signals.

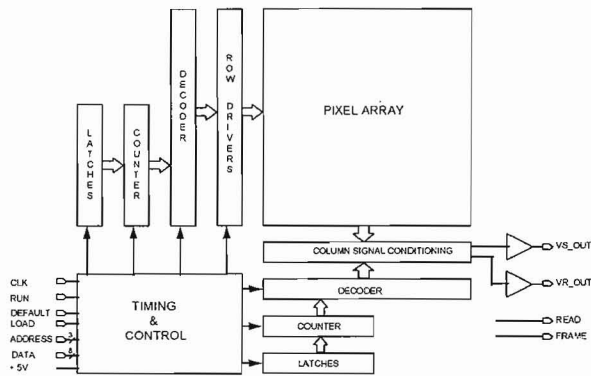


Fig. 4. Block diagram of on-chip timing and control electronics.

The chip can be commanded to read out any area of interest within the array. The decoder counters can be preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus. An alternate loading command is provided using the DEFAULT input line. Activation of this line forces all counters to a readout window of 128x128.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus. A 32-bit counter operates from one-fourth the clock input frequency and is preset each frame from the latch and so can provide very large integration delays. The input clock can be any frequency up to about 10 MHz. The pixel readout rate is tied to one-fourth the clock rate. Thus, frame rate is determined by

the clock frequency, the window settings, and the delay integration time. A 30 Hz frame rate can be achieved without difficulty.

The column signal conditioning circuitry contains a double-delta sampling [4] FPN suppression stage that reduces FPN to below 0.2% sat with a random distribution. Power dissipation in the timing and control digital circuitry is minimal, and scales with clock rate. A photograph of a chip is shown in Fig. 5 and sample output in Fig. 6.

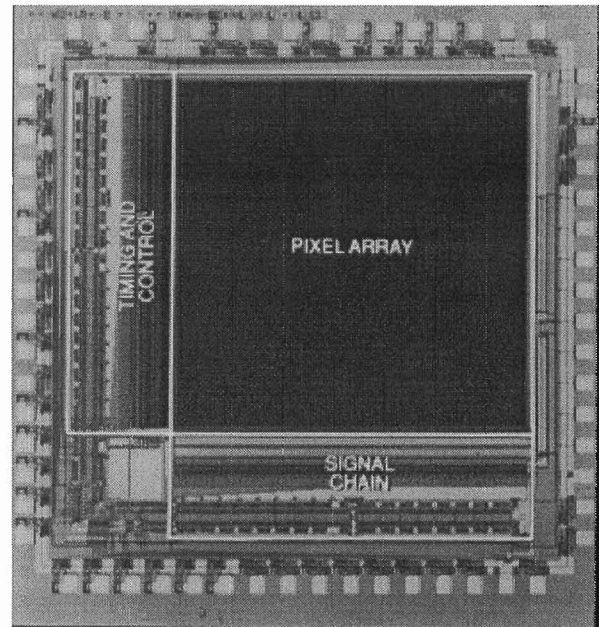


Fig. 5. Chip photograph of 128x128 element CMOS APS with on-chip timing and control circuitry.

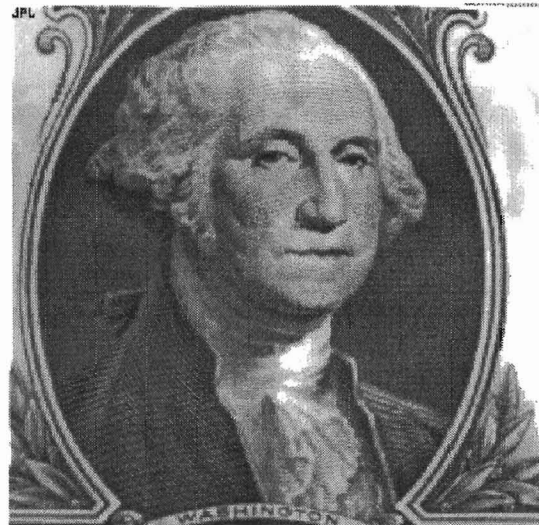


Fig. 6. Image of a dollar bill taken with 256x256 sensor.

## On-Chip Analog-to-Digital Converter (ADC)

On-chip ADC is desirable for several reasons. First, the chip becomes "digital" from a system designer's perspective, easing system design and packaging. Second, digital I/O improves immunity from system noise pickup. Third, component count is reduced. Fourth, while not immediately apparent, lower system power can be achieved, and possibly lower chip power dissipation as well [5].

JPL has developed a column-parallel approach to on-chip ADC, in which each (or nearly each) column in the array has its own tall, thin ADC. Single slope, algorithmic, and oversampled converters have been demonstrated in a column-parallel format. Shown below is a AT&T/JPL sensor with a column-parallel single slope ADC. Resolution of 8 bits at 30 Hz frame rate with 35 mW total power dissipation has been achieved [6]. Reduction in power and improved ADC performance is an active area of research at JPL.

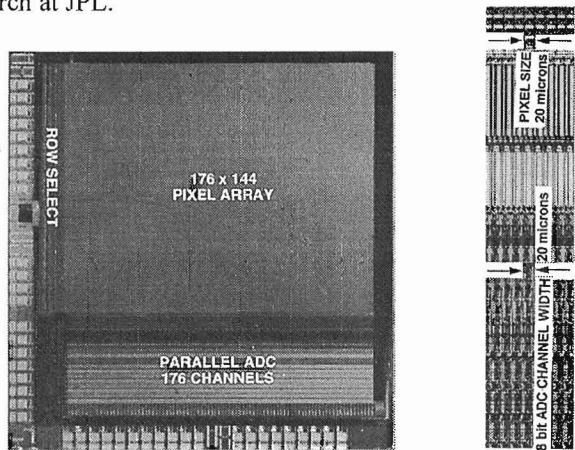


Fig. 7. AT&T/JPL 176x144 APS with 176 8-b ADCs in a column parallel architecture. Chip uses 35 mW at 30 Hz frame rate.

## Camera-On-A-Chip

To date, on-chip timing, control, APS array, and ADC have not yet been integrated to form the first true camera-on-a-chip, but such integration is expected to occur within the next year. JPL is presently developing a 1Kx1K array with a 10  $\mu\text{m}$  pixel pitch and column parallel 10-bit single slope ADC. A 256x256 sensor with algorithmic ADC will be fabricated later this year that will essentially require 5 V power, master clock, and will output serial digital image data. This chip will be used to demonstrate a very small camera called the Digital Imaging Camera Experiment (DICE). The DICE camera is shown below in Fig. 8. Power dissipation in DICE is expected to be well under

50 mW for 30 Hz operation. A wireless version of the DICE camera is under development for ARPA.

Low power, inexpensive cameras based on the camera-on-a-chip technology will find many new consumer applications for electronic imaging, such as home security, automotive, toys, baby monitors, traffic surveillance, PC video conferencing, video phones, and many more.

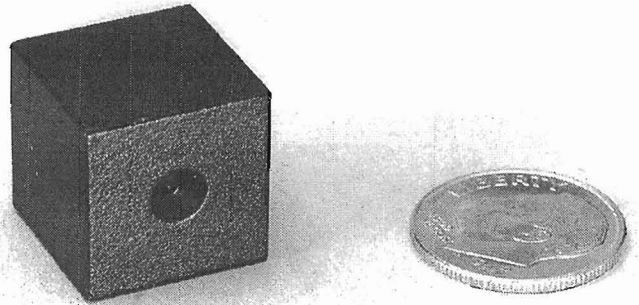


Fig. 7. Mock up of JPL Digital Imaging Camera Experiment (DICE), expected to be achieved in 1997 using camera-on-a-chip technology.

## Acknowledgments

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