Image Capture Circuits in CMOS

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Abstract

CMOS image sensors are a second-generation solid-state imaging technology. CMOS active pixel sensors have performance competitive with CCD technology, and offer advantages in on-chip functionality, system power reduction, cost and miniaturization. CMOS VLSI circuits for imaging and readout, and on-chip integration of ADC and smart functions will be addressed.

Introduction

Imaging with MOS devices predates charge-coupled devices (CCDs) by several years. However, CCDs over the past 27 years have become the predominant image sensor technology for camcorders and electronic image capture due to their superior sensitivity, readout noise, dynamic range, lower fixed pattern noise (FPN) and small pixel size. Recently, CMOS active pixel sensors (APS) have shown performance competitive with CCDs and with their low power, high levels of circuit integration, and lower fabrication cost, are now enabling new electronic imaging applications as well as supplanting CCDs in traditional applications[1].

Contributing to the recent activity in CMOS image sensors is the steady, exponential improvement in CMOS technology. The rate of minimum feature size decrease has outpaced similar improvements in CCD pixels (Fig. 1). Furthermore, sensor pixel size is limited by both optical physics and optics cost, making moot the CCD's inherent pixel size advantage. Recent progress in on-chip signal processing (and off-chip DSP) has reduced CMOS image sensor FPN to acceptable levels[2].

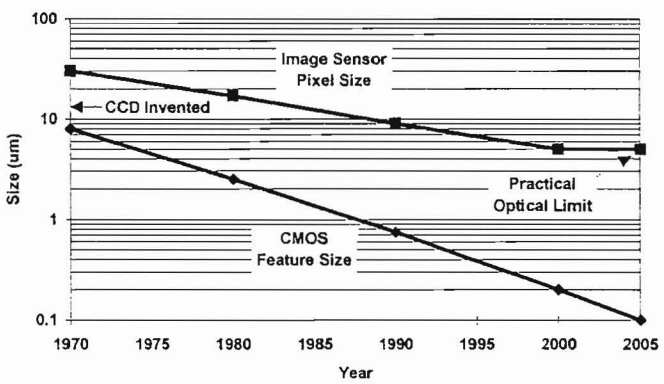

Fig. 1. The steadily increasing ratio between pixel size and minimum feature size permits the use of CMOS circuitry within each pixel.

This paper reviews the CMOS circuits typically used for pixel-level image capture, image readout, and on-chip analog-to-digital conversion.

Overall Architecture

The overall architecture of a CMOS image sensor is shown in Fig. 2. The image sensor consists of an array of pixels that are typically selected a row at a time by row select logic. This can be either a shift register or a decoder. The pixels are read out to vertical column busses that connect the selected row of pixels to a bank of analog signal processors (ASPs). These ASPs perform functions such as charge integration, sample and hold, correlated double sampling and FPN suppression.

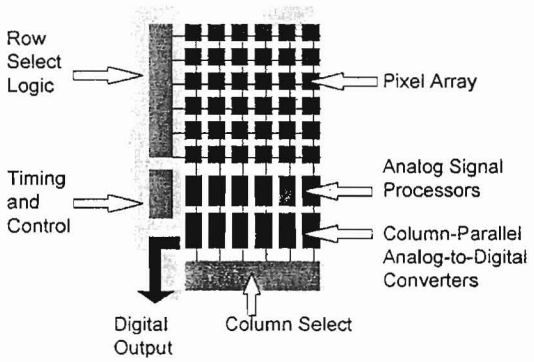

Fig. 2. CMOS APS integrates timing and control, ADC and other circuitry on the same chip.

More advanced CMOS image sensors contain on-chip analog-to-digital converters (ADC). In Fig. 2, the ADCs are shown as column-parallel ADCs; that is, each column of pixels has its own ADC. The digital output of the ADCs (or analog output of the ASPs) are selected for readout by column select logic that can be either a shift register or decoder.

Also integrated on-chip is a timing and control logic block. This digital block is readily defined at a high level using tools such as VHDL and inserted on-chip.

The CMOS image sensor architecture of Fig. 2 permits several modes of image readout. Progressive-scan readout of the entire array is the common readout mode. A *window* readout mode is readily implemented where only a smaller region of pixels is selected for readout. This increases access rates to windows of interest. A *skip* readout mode is also possible where every second (or third, etc.) pixel is readout. This mode allows for subsampling of the image to increase readout speed at the cost of resolution. Combination of skip and window

modes allows electronic pan, tilt and zoom to be implemented.

Pixel Circuits

Pixel circuits can be divided into *passive* pixels and *active* pixels. The active pixel sensor (APS) contains an active amplifier. There are three predominant approaches to pixel implementation in CMOS: photodiode-type passive pixel, photodiode-type active pixel, and photogate-type active pixel. These are described below.

A. Passive pixel approach

The photodiode-type passive pixel approach remains virtually unchanged since first suggested by Weckler in 1967[3,4]. The passive pixel concept is shown below in Fig. 3. It consists of a photodiode and a pass (access) transistor. When the access transistor is activated, the photodiode is connected to a vertical column bus. The charge integrating amplifier (CIA) readout circuit at the bottom of the column bus keeps the voltage on the column bus constant[5]. When the photodiode is accessed, the voltage on the photodiode is reset to the column bus voltage, and the charge, proportional to the photosignal, is converted to a voltage by the CIA. The single-transistor photodiode passive pixel allows the highest design fill factor for a given pixel size or the smallest pixel size for a given design fill factor for a particular CMOS process. The quantum efficiency of the passive pixel (ratio of collected electrons to incident photons) can be quite high due to the large fill factor and absence of an overlying layer of polysilicon such as that found in many CCDs. This passive pixel is the basis for arrays produced by EG&G Reticon, Hitachi[6], Matsushita[7] and more recently, by Edinburgh University and VLSI Vision in Scotland[8,9], Linkoping University and IVP in Sweden[10,11,12], and Toyohashi University[13].

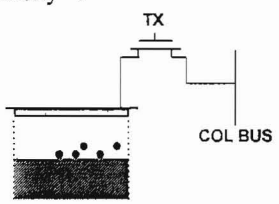

Fig. 3. Passive pixel schematic and potential well. When the transfer gate TX is pulsed, photogenerated charge integrated on the photodiode is shared on the bus capacitance.

The major problems with the passive pixel are its noise level and scalability. Noise on a passive pixel is typically of the order of 250 electrons r.m.s., compared to commercial CCDs that achieve less than 20 electrons r.m.s. of read noise. The passive pixel also does not scale well to larger array sizes and or faster pixel readout rates. This is because increased bus capacitance and faster readout speed both result in higher readout noise. To date, passive pixel sensors suffer from large fixed pattern noise, though this is not a fundamental problem.

B. Active pixel approach

It was quickly recognized, almost as soon as the passive pixel was invented, that the insertion of a buffer/amplifier into the pixel could potentially improve the performance of the pixel. A sensor with an active amplifier within each pixel is referred to as an active pixel sensor or APS. Since each amplifier is only activated during readout, power dissipation is minimal and generally less than a CCD. Non-CMOS APS devices have been developed that have excellent performance such as the charge-modulation devices (CMD)[14] but these devices[15,16,17] require a specialized fabrication process. In general, APS technology has many potential advantages over CCDs[18] but is challenged by residual FPN and less maturity than CCDs.

The CMOS APS trades pixel fill factor for improved performance compared to passive pixels using the in-pixel amplifier. Pixels are typically designed for a fill factor of 20-30%, similar to interline-transfer (ILT) CCDs. Loss in optical signal is more than compensated by reduction in read noise for a net increase in signal to noise ratio and dynamic range. Microlenses are commonly employed with low fill factor ILT CCDs[19,20] and can recover the lost optical signal. The simple, polyimide microlense refracts incident radiation from the circuitry region of the pixel to the detector region. The microlense can improve optical fill factor by 3-fold so that the net optical aperture for the detector is 60%-80%.

C. Photodiode-type APS

The photodiode-type (PD) APS was described by P.Noble in 1968[5] and has been under investigation by F.Andoh at NHK in Japan since the late 1980's[21,22,23] in collaboration with Olympus, and later, Mitsubishi Electric. A diagram of the PD-APS is shown below in Fig. 4.

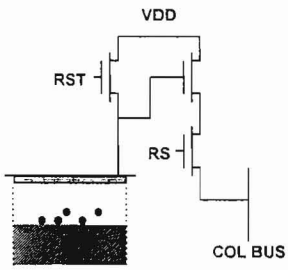

Fig. 4. A photodiode-type active pixel sensor (APS). The voltage on the photodiode is buffered by a source follower to the column bus, selected by RS-row select. The photodiode is reset by transistor RST.

The first high-performance PD-APS was demonstrated by JPL in 1995 in a 128x128 element array that had on-chip timing, control, correlated double sampling and fixed pattern noise suppression circuitry[24]. Arrays as large as 1024x1024 have been developed by a JPL/AT&T collaboration[25]. A 640x480 PD-APS with 5.6 μm x 5.6 μm pixels and on-chip color filter arrays and microlenses was described by Toshiba in 1997[26], and a 800x1000 element PD-APS was reported by VLSI Vision also 1997[27].

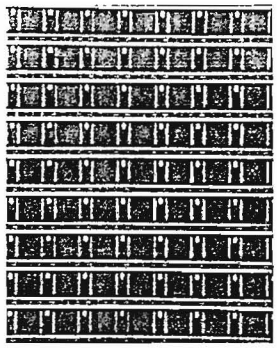

Fig. 5. Close up of 11.9 μm pixel photodiode-type active pixels used in the 1024x1024 array shown in Fig. 9

More complicated pixels can be constructed to improve functionality and to a lesser extent, performance. Hamamatsu reported on an improved sensor that used a transfer gate between the photodiode and the source follower gate[28]. The transfer gate keeps the photodiode at constant potential and increases output conversion gain by reducing capacitance but introduces lag. The Hamamatsu sensor also improved fixed pattern noise using a feedback technique. More complication was added by the Technion to permit random access and electronic shuttering at a significant expense of pixel size[29]. Similar work was reported recently by Stanford[30]. A method for individual pixel reset for regional electronic shutter was presented by JPL[31]. Current-mode readout of CMOS APS has been investigated[32], and reported by Polaroid[33] but gain and offset FPN remain a challenge in current mode.

Photodiode-type APS pixels have high quantum efficiency as there is no overlying polysilicon. The read noise is limited by the reset noise on the photodiode since correlated double sampling is not easily implementable without frame memory, and is thus typically 75-100 electrons r.m.s. The photodiode-type APS uses three transistors per pixel and has a typical pixel pitch of 15x the minimum feature size. The photodiode APS is suitable for most mid to low performance applications, and its performance improves for smaller pixel sizes since the reset noise scales as $C^{1/2}$, where C is the photodiode capacitance. A tradeoff can be made in designed pixel fill-factor (photodiode area), dynamic range (full well) and conversion gain (μV/e-). Lateral carrier collection permits high responsivity even for small fill-factor[34].

D. Photogate-type APS

The photogate APS was introduced by JPL in 1993[35,36,37] for high performance scientific imaging and low light applications. The photogate APS combines CCD benefits and X-Y readout, and is shown schematically below in Fig. 6. Signal charge is integrated under a photogate. For readout, an output floating diffusion is reset and its resultant voltage measured by the source follower. The charge is then transferred to the output diffusion by pulsing the photogate. The new voltage is then sensed. The difference between the reset level and the signal level is the output of the sensor. This correlated double sampling suppresses reset noise, 1/f noise, and fixed pattern noise due to threshold voltage variations.

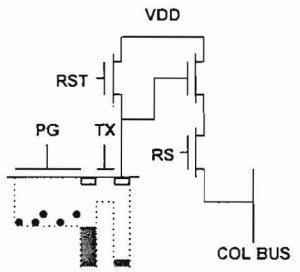

Fig. 6. Photogate-type APS pixel schematic and potential wells. Transfer of charge and correlated double sampling permits low noise operation.

The photogate and transfer gate ideally overlap using a double poly process. However, the insertion of a bridging diffusion between PG and TX has minimal effect on circuit performance and permits the use of single poly processes[38]. (Approximately 100 e- of lag has been attributed to the bridging diffusion[39]) The photogate-type APS uses five transistors per pixel and has a pitch typically equal to 20x the minimum feature size. Thus, to achieve a 10 μm pixel pitch, a 0.5 μm process must be employed. A 0.25 μm process would permit a 5 μm pixel pitch. The floating diffusion capacitance is typically of the order of 10 fF yielding a conversion gain of 10-20 μV/electron. Subsequent circuit noise is of the order of 150-250 μV r.m.s., resulting in a readout noise of 10-20 electrons r.m.s., with the lowest noise demonstrated to date of 5 electrons r.m.s.[34].

E. Logarithmic pixels

In some cases, non-linear output of the sensor is desired. Non-linear output permits an increase in intra-scene dynamic range as the photosignal is companded. Gamma-correction (basically a square-root transform) is one example of companding. A second example is logarithmic transformation, where the output signal from the pixel is proportional to the logarithm of the photosignal[40,41,42]. An example of this type of pixel circuit[43] is shown in Figure 7.

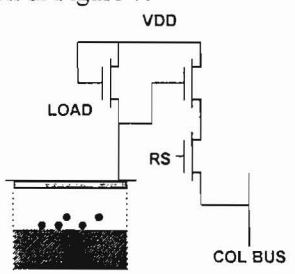

Figure 7. Logarithmic pixel schematic circuit.

The photodiode voltage self-adjusts to a level such that the load transistor current is equal to the photocurrent collected by the photodiode. This results in a logarithmic transformation of the photosignal for typical light levels. The drawback to this non-integrating approach is very slow response time for low light levels, and large fixed pattern noise (e.g. 60 mV). Dynamic range of less than 50

dB was reported due to temporal noise and small voltage swings.

A non-integrating 512x512 element photodiode-type APS was reported by IMEC with a 6.6 μm pixel pitch[44]. This sensor operates in a non-integrating current mode with logarithmic response. FPN was corrected by means of hot-carrier-induced threshold voltage shift.

F. Other pixels

The pinned photodiode, developed for interline transfer CCDs, features high quantum efficiency (esp. in the blue), low dark current, and low noise readout. The pinned photodiode has been combined with CMOS APS readout by JPL/Kodak to achieve high performance pixel response[45].

A photogate CMOS APS with a floating-gate sense amplifier that allows multiple non-destructive, doubly sampled reads of the same signal was developed by JPL for use with oversampled column-parallel ADCs[46].

A floating gate sensor with a simple structure was reported by JPL/Olympus[47]. This sensor used a floating gate to collect and sense the photosignal and features a compact pixel layout with complete reset.

There has been significant work on retina-like CMOS sensors with non-linear, adaptive response. While their utility for electronic image capture has not yet been demonstrated, their very large dynamic range and similarity to the response of the human eye offer intriguing possibilities for on-chip intelligent imaging[48].

New pixel designs that circumvent limitations in future scaled CMOS[49] and take advantage of opportunities in advanced CMOS devices can be anticipated.

Analog signal processing

On-chip analog signal processing can be used to improve the performance and functionality of the CMOS image sensor. A charge integration amplifier is used for passive pixel sensors and sample and hold circuits typically employed for active pixel sensors. JPL has developed a delta-difference sampling (DDS) approach to suppress FPN peak-to-peak to 0.1% of saturation level[24]. Other examples of signal processing demonstrated in CMOS image sensors include smoothing using neuronMOSFETs[50], motion detection[51], programmable amplification[52], multiresolution imaging[53], video compression[54], discrete cosine transform (DCT)[13], and intensity sorting[55]. Continued improvement in analog signal processing performance and functionality is expected. Other computational-type optical sensors have been demonstrated that use CMOS analog signal processing[56,57].

On-chip Analog-to Digital Converter (ADC)

To implement a camera on-a-chip with a full digital interface requires an on-chip analog-to-digital converter (ADC). There are many considerations for on-chip ADC. The ADC must support video rate data that ranges from 0.92 Msamples/s for a 320x288 format sensor operating at 10 frames per second for videoconferencing, to 55.3 Msamples/s for a 1280x720 format sensor operating at 60 frames per second. The ADC must have at least 8b resolution with low integral non-linearity (INL) and differential non-linearity (DNL) so as not to introduce distortion or artifacts into the image. The ADC can dissipate only minimal power, typically under 100 mW, to avoid introduction of hot spots with excess dark current generation. The ADC cannot consume too much chip area or it will void the economic advantage to on-chip integration. The ADC cannot introduce noise into the analog imaging portion of the sensor through substrate coupling or other crosstalk mechanisms that would deteriorate image quality.

Fig. 8. Unprocessed image taken from a Photobit 256x256 element sensor with on-chip ADC operating at 30 fps. Note no blooming from light and lack of other artifacts.

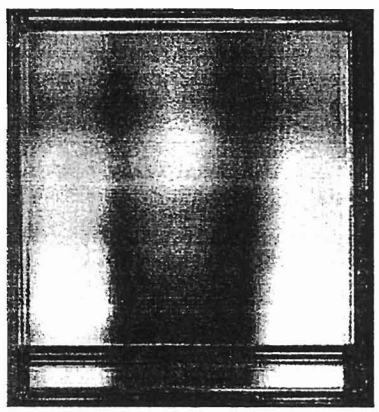

Fig. 9. A JPL 1024x1024 photodiode-type CMOS APS with 1024 column-parallel single-slope ADCs for slow-scan scientific applications.

CMOS image sensors with on-chip single-slope ADC have been reported previously[12,58] and related work on on-chip ADCs for infrared focal-plane array readout has been reported[59,60,61]. There are many considerations for implementation of on-chip ADC[62]. The ADC can be implemented as a single serial ADC (or several ADCs, e.g. one per color) that operate at near video rates [10 Msamples/s]. The ADC can also be implemented in-pixel[63,64,65] and operate at frame rates [e.g. 30 samples/s]. We have been pursuing column-parallel ADCs where each (or almost each) column in the pixel array has its own ADC so that each ADC operates at the row rate [e.g. 15 ksamples/s]. In this architecture, single-slope ADCs work well for slow-scan applications but dissipate too much

power for video-rates. Oversampled ADCs require significant chip area when implemented in column-parallel formats[66]. A successive approximation ADC has a good compromise of power, bit resolution, and chip area. On-chip ADC enables on-chip DSP for sensor control and compression preprocessing.

Conclusions

CMOS image sensors are well-poised to both penetrate many traditional CCD markets as well as enable new applications. The low system power enables new portable applications, and the low system cost enables semi-disposable applications. Rapid advancement is expected over the next few years.

Acknowledgments

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