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GHz GaAs CCDs: promises, problems, and progress

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ABSTRACT

Progress in high-speed GaAs charge-coupled device (CCD) research is described. Experimental and modelling results are reported for two different structures; capacitive gate CCD's and resistive gate CCD's. A charge packet replicator/subtractor circuit is discussed.

1. INTRODUCTION

The promise of GaAs charge-coupled devices (CCD's) lies in the capability for high speed, low noise operation coupled with superior electro-optic material properties. These attributes are a direct consequence of the high electron mobility and wide direct bandgap in this material system. The principal problem with GaAs CCD's, as with other GaAs devices, is the lack of technological maturity relative to silicon. However, the possibility for bandgap engineering of the electronic and electro-optic properties of III-V compounds is rapidly pushing GaAs technology toward parity. In particular, the ability to engineer detectors optimized for specific frequencies in the infrared spectrum is a strong motivation for the implementation of linear and area imagers with GaAs CCD's.

Two CCD device structures based on Schottky barriers, rather than insulated gates, have found application in GaAs: capacitive-gate CCD's (CGCCD's) and resistive-gate CCD's (RGCCD's). Initially, buried-channel CGCCD's were explored since these devices were well understood in silicon. This traditional CCD structure, shown in Fig. 1a, depends on the fringing fields between closely spaced gate electrodes to achieve coupling of adjacent potential wells. As the gap between the electrodes decreases in size, the increasing fringing fields ensure the absence of a potential trough. Of equal importance in CGCCD's is that the gate length be small enough that the charge move rapidly under the influence of the large fringing fields. If gate length is excessive the charge transfer time will be limited by diffusion, greatly reducing the maximum clock frequency. In silicon, strict control of the interelectrode gap is not required since overlapping gates are readily fabricated. While overlapping gates can be realized in GaAs, the metal-on-dielectric in the gap has very little control over the GaAs surface potential because of surface Fermi level pinning. Therefore, for the same reason MOSFET's are not easily realized in GaAs, control of the gap potential must come from the proximity of gate electrodes.

Resistive gate CCD's (RGCCD's) eliminate the interelectrode gap entirely, and ensure that the charge packets are transferred under the influence of electric field. In RGCCD's, shown in Fig. 1b, a layer of resistive material, which forms a Schottky barrier to the GaAs, is used as a continuous voltage divider between two or more finger contacts. The channel potential follows the linear resistive-gate voltage drop between finger electrodes and hence the carriers move under the influence of electric field. In addition, RGCCD's have shown greater compatibility with conventional MESFET technology. Compatibility with typical MESFET active layers is desirable in order to facilitate integration of the CCD's with high-performance on-chip amplifiers and digital logic for clock generation. The primary problem with RGCCD's is that the gates dissipate dc power.

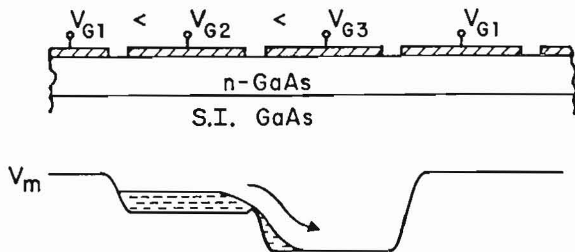


Fig. 1a CGCCD channel potential.

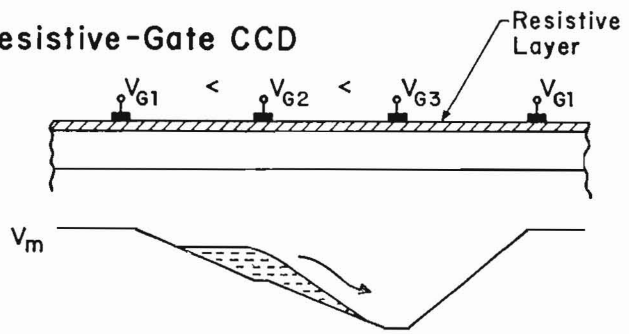


Fig. 1b RGCCD channel potentia.

This paper describes investigation into performance improvements for both CGCCD's and RGCCD's, and exploration of GaAs CCD-based circuits for use in image processing applications. Device improvements and characterization have been carried out in conjunction with 2-dimensional modelling.

2.IMPROVED CTE IN CAPACITIVE GATE CCD'S

The major problem with GaAs CGCCD's is a potential trough in the interelectrode gap region. The gap potential trough problem is illustrated in Fig. 2. A simple one-dimensional solution to Poisson's equation indicates that for an empty potential well, the channel potential is more positive than the gate by the pinch-off voltage of the active layer. If one applies the same analysis along the surface in the interelectrode gap, ignoring surface charge, the center of the gap is more positive than the gates by an amount proportional to doping and gap size. This implies that the channel under the gap is more positive than the channel under the gates by approximately the same amount. The effect of this potential trough is to reduce the charge transfer efficiency (CTE) of the CCD. While making the active layer thinner reduces the pinch-off voltage, reducing the gap size decreases the difference between the gate potential and the potential in the center of the gap. This reasoning also implies that reducing the doping will linearly reduce the potential trough. Unfortunately, a decrease in doping results in a corresponding decrease in dynamic range - the maximum charge packet being proportional to qN_dT', where T' is the effective active layer thickness. In order to balance these considerations, early GaAs CCD investigations utilized relatively thick active layers with low doping[1]. The difficulty is the consequent incompatibility with conventional MESFET's, which require thin, highly-doped active layers for high transconductance.

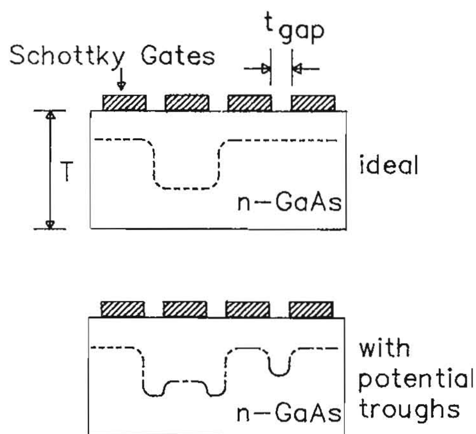


Fig. 2 Channel potential for excessively large gaps.

Table 1. Experimental results

Gap Size (um)	Channel Thick-ness (um)	Doping (cm−3)	Gate Length (um)	Thres-hold Voltage (volts)	Potential Trough (volts)	CTE
1.0	0.35	1.2×10^{17}	2.0	9.5	7.13	< 0.90
1.0	0.35	7.5×10^{16}	2.0	6.0	3.85	0.95
1.0	0.90	7.0×10^{15}	2.0	3.0	0.12	> 0.999

At present, delay lines have been fabricated at Columbia with three different layer structures. The results, shown in Table 1, demonstrate the dramatic effect doping has on transfer efficiency. Potential trough depth has been calculated using a 2-dimensional solution to Poisson's equation, which accounts for surface charge due to Fermi level pinning. CTE has been calculated using the summation of leading-edge/trailing-edge loss, as proposed by Brodersen et al.[2]. Fig. 3 shows the output of a 50-stage, 4-phase shift register fabricated on an active layer with $7\times10^{15}/cm^3$ doping. A cross-section of the CGCCD device is shown in Fig. 4. The CCD gates are 100 um wide and 2 um long, while FET gate length is 1 um. The fabrication of these devices is, in most respects, similar to that of the RGCCD's except for starting material. Devices are mesa isolated by isotropic etch back to the undoped GaAs. All metal definition is by lift-off, with a minimum feature size of 1.0 um. Ohmic contacts are made with AuGe alloyed by rapid thermal annealing. Gate and overlayer metalization is chromium deposited by electron beam evaporation, followed by deposition of gold by thermal resistive boat evaporation. The interlayer dielectric is CIBA-GEIGY Probimide 400, a photolithographically patternable polyimide that requires only a UV cure.

With the goal of achieving good quality MESFET's integrated with high CTE CCD's, a number of schemes for reduction of the gap size have been proposed previously. Techniques for gap size reduction have included angled evaporation of stepped gate electrodes[3], overlapping gates using dielectric spacers defined by reactive ion etching (RIE)[4], and overlapping gates by anodic oxidation of alternating gate electrodes[5]. Of these, the use of dielectric spacers shows the most promise, due to its greater process flexibility and control in defining the gap size. The penalty for reducing the gap size, aside from increased process complexity, is lowering of the gate-to-gate breakdown voltage.

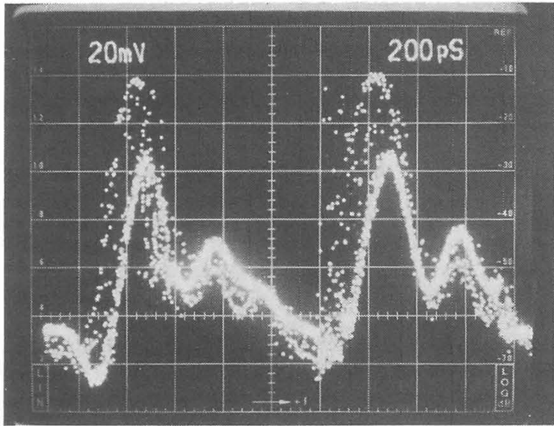


Fig. 3a Delay line output signal.

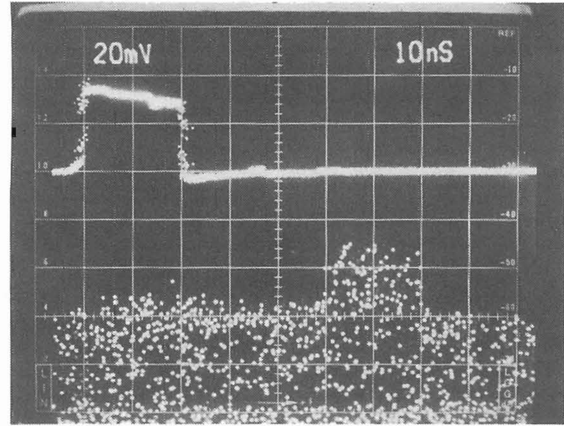


Fig. 3b 50 ns delay from input (-20 dB).

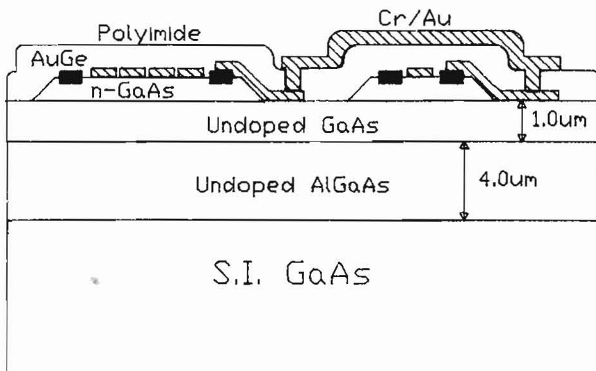


Fig. 4 CGCCD cross section.

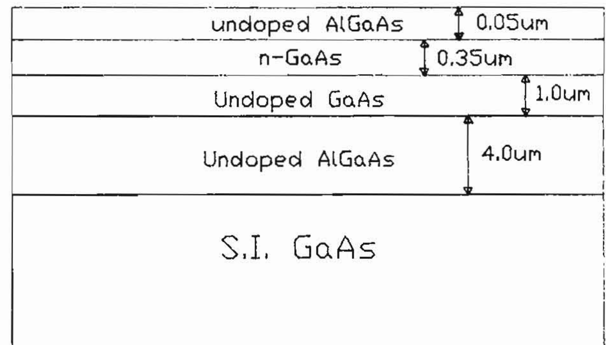
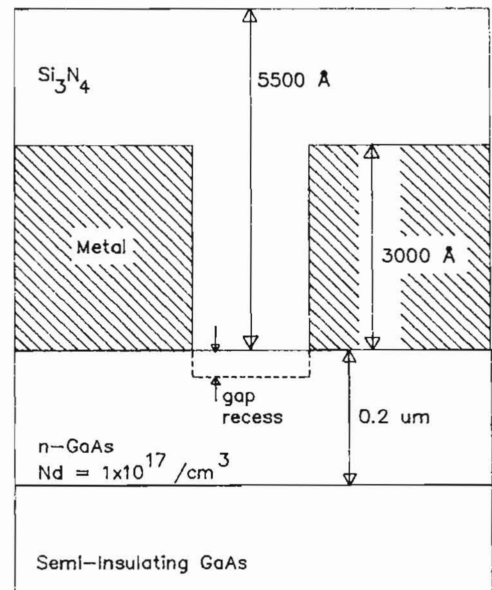


Fig. 5 Structure with AlGaAs cap layer.

Table 2. Simulation of potential trough depth

Gap Size (um)	Channel Thick-ness (um)	Doping (/cm^3)	Gap Recess Depth (A)	Channel Potential Under Gate (volts)	Channel Potential Under Gap (volts)	Potential Trough (volts)
2.0	0.2	1×10^{17}	0	2.36	7.55	5.19
1.5	0.2	1×10^{17}	0	2.36	5.91	3.55
1.0	0.2	1×10^{17}	0	2.36	4.31	1.95
0.75	0.2	1×10^{17}	0	2.36	3.59	1.23
0.5	0.2	1×10^{17}	0	2.36	2.92	0.56
0.25	0.2	1×10^{17}	0	2.36	2.44	0.08
1.0	0.2	1×10^{17}	0	2.36	4.31	1.95
1.0	0.2	1×10^{17}	100	2.36	3.91	1.55
1.0	0.2	1×10^{17}	200	2.36	3.61	1.25
1.0	0.2	1×10^{17}	300	2.36	3.28	0.92
1.0	0.2	1×10^{17}	400	2.36	2.95	0.59
1.0	0.2	1×10^{17}	500	2.36	2.60	0.24
1.0	0.2	1×10^{17}	600	2.36	2.23	−0.13
1.0	0.2	1×10^{17}	700	2.36	1.84	−0.52



A new approach which avoids this breakdown problem is to thin the active layer in the interelectrode gaps. Table 2 shows the results of a 2-dimensional solution to Poisson's equation for the channel potential under two adjacent gates and the gap. Note that surface charge in the gap due to Fermi level pinning has been taken into account. As expected, reducing the gap size alleviates the gap potential problem. The simulations also suggest that reducing the channel thickness in the gap can greatly reduce the potential trough. Recessing of relatively large 1 um gaps is simple to realize, although simulations indicate potential barriers can be created if the gap recess is not well controlled. Fabrication of recessed-gap CCD shift registers is in progress.

3. REDUCTION OF GATE LEAKAGE CURRENT

Excessive gate leakage current degrades CTE and dynamic range by adding charge to the signal packet during each transfer and can be considered a form of dark current. Furthermore, the gate leakage current is non-uniform giving rise to fixed-pattern noise. Improving the gate leakage current is accomplished by increasing the Schottky barrier height. Two different approaches to this problem have been explored at Columbia: modification of the metal-GaAs interface and the use of an AlGaAs top layer. The first method, which is discussed in detail elsewhere[6], is based on the effective work function model (EWF)[7] of the metal-GaAs interface. This model contends that barrier height is an average of the effective work functions of mixed interface phases resulting from chemical reactions between the metal and semiconductor. If low work function regions exist at the interface they could reduce the effective work function and the observed barrier height. Reduction or elimination of these low work function phases is achieved by deposition of an 100 A arsenic layer prior to gate metallization. Leakage current reduction factors of over 25 have been obtained.

Previous work in III-V imagers[8] has sought to take advantage of the low bulk generation rate in wider-bandgap AlGaAs by using this material as the channel layer. Observation of bulk generation dominated dark current in these devices was possible because the Schottky barrier heights on AlGaAs are more than 0.1 eV higher than on GaAs. Unfortunately, the relatively low electron mobility of AlGaAs prohibits the realization of high transconductance FET's. While it is possible to use a GaAs active layer for FET's on top or below the AlGaAs CCD channel layer, this results in increased process complexity and non-planarity of the surface topology.

An alternative approach is to use a thin layer of AlGaAs at the surface to increase the Schottky barrier height. CGCCD's fabricated using this structure, as shown in Fig. 5, have low gate leakage and retain the good FET parameters of a GaAs active layer. No major process modification is needed to accomodate the thin AlGaAs top layer. Fig. 6 shows the results for diodes fabricated on top of the AlGaAs and also on the GaAs after a recessing etch through the AlGaAs. A four order of magnitude reduction in leakage current is achieved, which makes the leakage current of the CCD gates comparable to the bulk generation rate for GaAs. To date, CGCCD's have been fabricated with an AlGaAs cap layer and a 50-stage, 4-phase delay line has been demonstrated at Columbia.

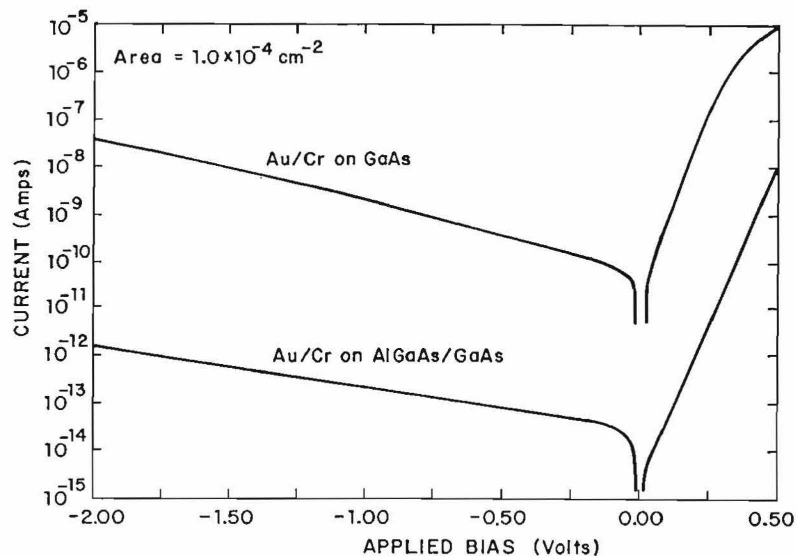


Fig. 6 Schottky I-V's on GaAs and AlGaAs/GaAs.

4. RESISTIVE GATE CCD'S

Resistive gate CCD's have shown impressive performance with demonstrated operation in the 1 Mhz to 4 GHz range and a CTE of 0.99 at 2.5 GHz[9]. These devices had active layers 0.2 um thick with doping of $1.0x10^{17}/cm^3$. As discussed previously, the buried-channel potential follows the linear resistive-gate voltage drop. Therefore the electric field in the empty channel is constant. However, the presence of signal charge perturbs the applied field such that the leading edge of the charge packet experiences a higher electric field than the trailing edge. As in a Gunn diode, if the applied electric field exceeds the critical field for peak electron velocity, the leading edge of the charge packet will have lower velocity than the trailing edge. This can inhibit charge packet broadening[10] caused by diffusion and self-repulsion, resulting in reduced transfer times. Fig. 7 and Fig. 8 show the simulated evolution of a charge packet during transfer for different applied electric fields, demonstrating the inhibition of charge packet broadening. Experimental confirmation of the simulation results is proceeding with the fabrication of RGCCD's using cermet, a SiO_x/Cr mixture, as the resistive gate layer.[11]

In addition to RGCCD's based on cermet, it is also possible to use a low bandgap, high resistivity semiconductor as the resistive gate. This heterostructure RGCCD (HRGCCD) has the potential advantage of providing a more uniform interface with the GaAs and may eliminate some of the contact problems inherent in the use of cermet. Fabrication of HRGCCD's based on an InGaAs resistive gate has begun. Thus far, resistive-gate FET's have demonstrated the feasibility of using this material structure in HRGCCD's.

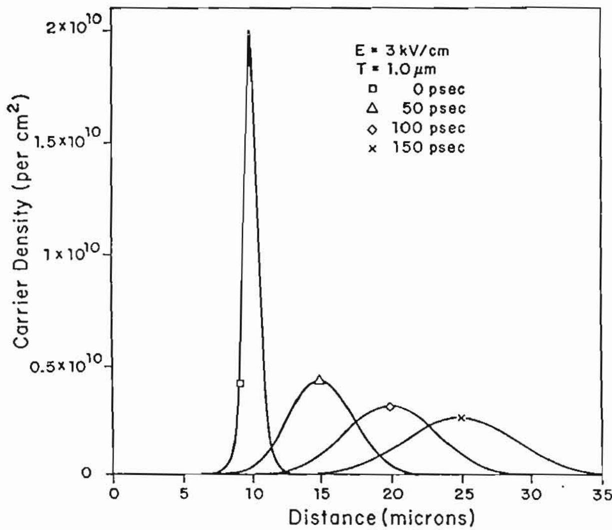


Fig. 7 Charge packet evolution, low field.

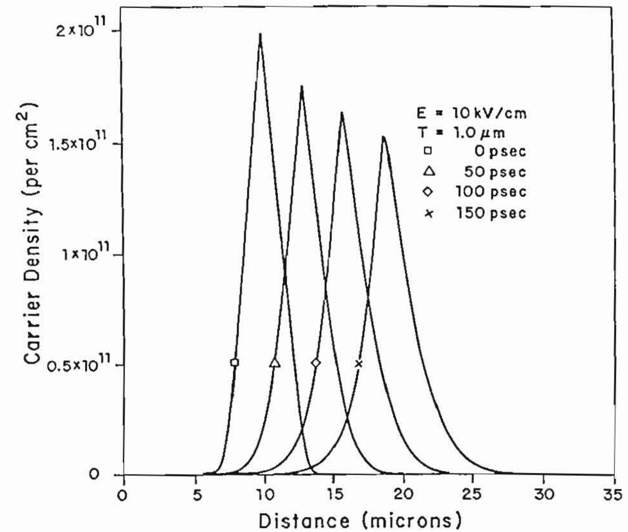


Fig. 8 Charge packet evolution, high field.

5. CHARGE PACKET REPLICATOR/SUBTRACTOR

In conjunction with basic device research, a parallel investigation of circuit concepts based in GaAs CCD's is being conducted. The motivation for this work is to provide the capability for image processing in the analog domain, either at the focal plane or in the output data stream, similiar to the type available in Si.[12,13] In addition, analog-to-digital conversion done with Si CCD technology, might also be implemented in GaAs.[14] Circuits under investigation include a charge packet magnitude comparator, charge domain multiplier, and a charge packet replicator/subtractor.

A schematic diagram of the charge packet replicator/subtractor is shown in Fig. 9. The essential part of the circuit is two capacitively coupled shift registers. When a charge packet is introduced under floating gate B0, a replica equal in magnitude is subtracted from the charge packet stored under floating gate A0. Due to the low parasitic capacitance of the GaAs semi-insulating substrate, nearly all the charge balancing occurs through charge packet redistribution, making the gain of the replication unity. The exact voltage on gate A4 is unimportant, as long as it provides charge confinement under gate A0. FET T1 allows presetting of the floating electrodes and can be used to switch the replication process on and off at the same frequencies used for clocking. The amplifiers shown are necessary only for characterization and not essential to the replication circuit. Fig. 10 shows amplifier outputs for the replica and original charge packets, demonstrating the linear, unity gain replication process. Testing at clock frequencies in the 0.6 - 1.0 GHz range is in progress.

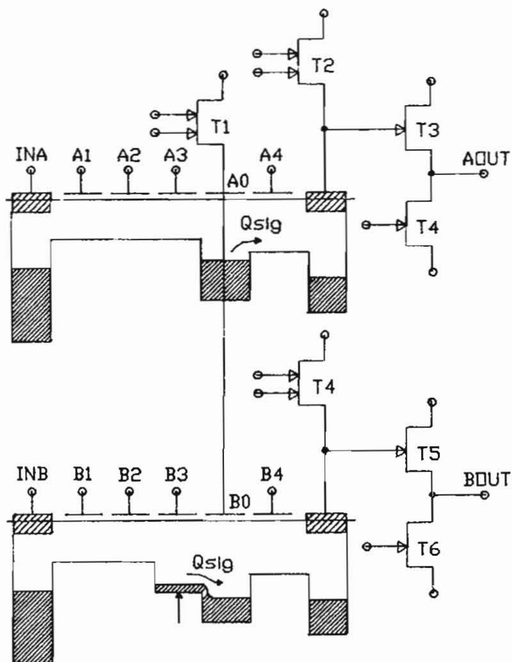


Fig. 9 Charge packet replicator/subtractor.

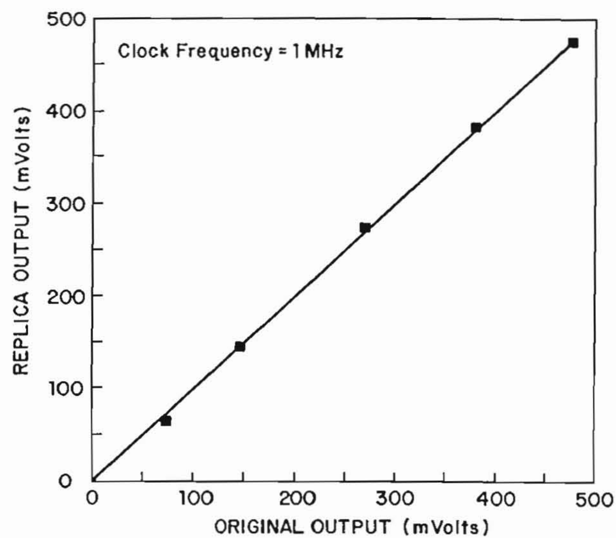


Fig. 10 Output of replica charge packet vs. original charge packet.

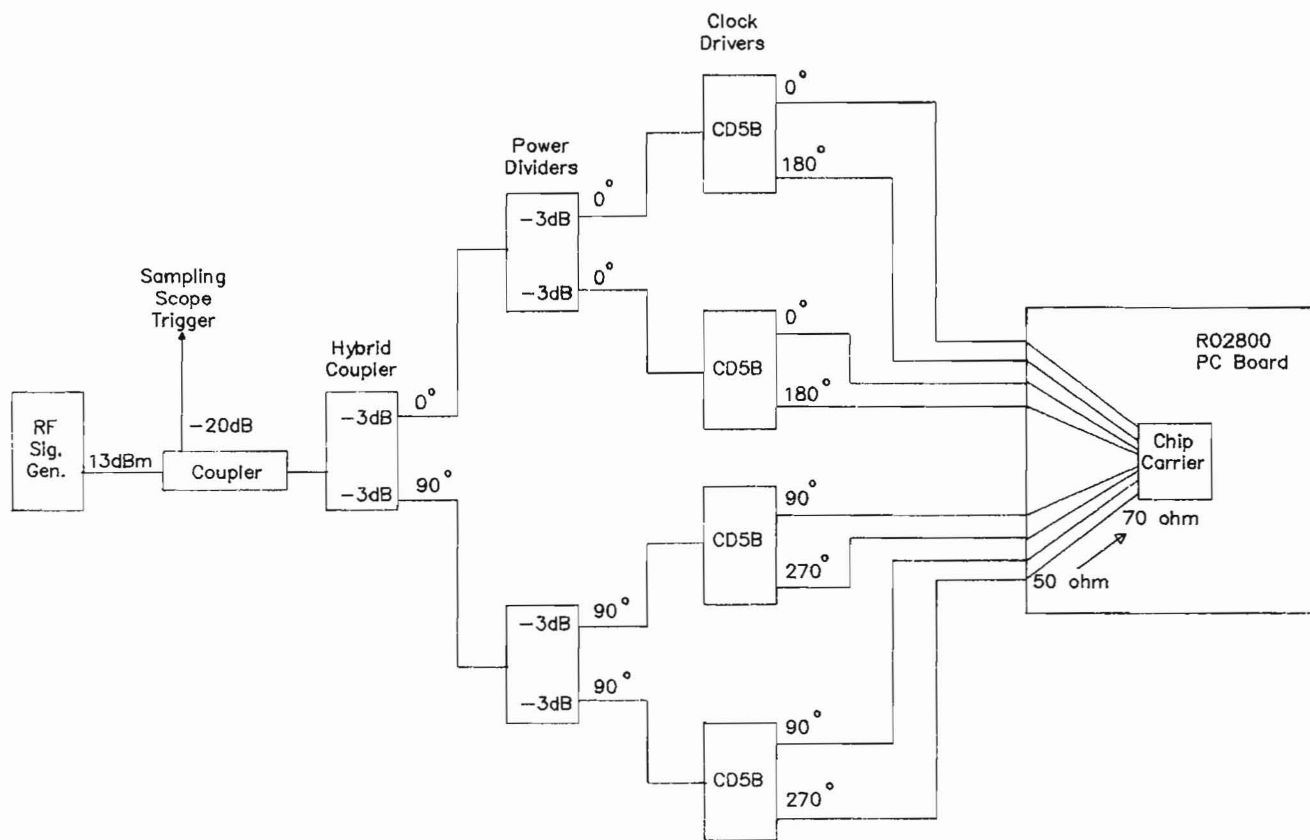


Fig. 11 High speed CCD test station.

6. TEST STATION

A schematic diagram of the main features of the high speed CCD test setup is shown in Fig. 11. This configuration is similar to that used in previous GHz range testing of GaAs CCD's[1], except for the use of the Colby Instruments' CD5B clock drivers. These clock drivers are essentially high speed comparators which accept a relatively low power RF signal and produce a 0-5 volt square wave into 50 ohms at the input signal frequency. Use of the CD5B clock drivers allows duty cycle variation, clock gating, and limited DC offset control. Future work in this area will look at integrating this comparator function on chip, where the comparators need only drive the capacitive load of the CCD gates. The RF signal source is a low cost voltage-controlled oscillator (VCO) based on bipolar silicon technology. Use of this kind of RF source is possible since the relative clock phases are independent of frequency, if clock path length differences are kept small compared to signal wavelength. As is the case in GaAs digital circuits, chip packaging for high pin count devices is a difficult issue. The approach taken in this work involved chip mounting in a 68 pin wire-bonded chip carrier which is pressure contacted to a Rogers RO2800 PTFE Composite circuit board, patterned with 50 ohm microstiplines. Presently, every other pin is used as a ground line to assure low cross talk. Connection to the printed circuit board periphery is through SMA-to-microstripline launcher connectors. This packaging allows 5 volt pulses with 100 ps rise times to travel to the chip carrier and out unattenuated.

7. SUMMARY

In anticipation of the contributions that GaAs and other III-V material systems can make to imaging applications, a number of investigations into improving GaAs CGCCD and RGCCD performance are underway. Problems and fundamental physics particular to two types of CCD structures have been addressed experimentally and with computer modelling. Furthermore, a GaAs CCD based replicator/subtractor has been demonstrated. This circuit represents a first step toward applying GaAs CCD's to analog image processing.

8. ACKNOWLEDGMENTS

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