

Future Prospects for CMOS Active Pixel Image Sensors

Eric R. Fossum
Jet Propulsion Laboratory
California Institute of Technology

Philip H.S. Wong
IBM Research Center
Yorktown Heights, NY

Abstract

Less than two years ago at this meeting, there was a debate about whether it was worthwhile investigating active pixel sensors. Since that time, the JPL CMOS active pixel image sensor (APS) has proven to yield surprisingly good performance and has received significant attention from industry. To date, CMOS APS has achieved low read noise (typically 15-25 electrons r.m.s), quantum efficiency per pixel exceeding that of interline transfer CCDs, high dynamic range (e.g. 75 dB), no smear, and excellent antiblooming control. Arrays as large as 256x256 have been readily fabricated by industry and several 1K x 1K arrays are in development.

The major advantages of a CMOS APS over a CCD are power, cost and integration level. Power dissipation in a CMOS APS camera chip with on-chip timing, control, drive and signal chain is typically under 10 mW, or more than two orders of magnitude less than a CCD-based system. Low cost sensors are achievable because of the high production rate of CMOS around the world. It is estimated that the cost of producing TV-standard (250 kpixel) CCDs is about \$50/Mpixel. Megapixel CCDs have a cost in the neighborhood of \$1000/Mpixel. The cost of producing CMOS image sensors is estimated to be approximately \$50/Mpixel scaled into the megapixel class. Integration of on-chip timing, control, signal chain and analog-to-digital converter electronics impacts sensor system cost since these components must otherwise be supplied and assembled with the sensor chip. Other advantages of CMOS APS include much lower system power requirements (enabling wireless applications), random access readout, and low voltage operation.

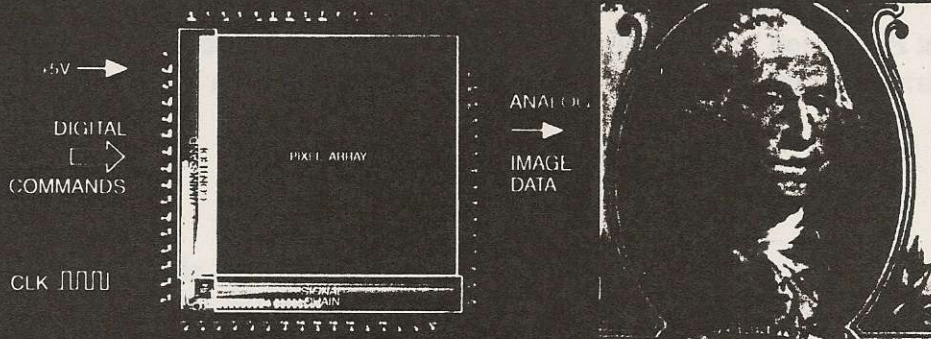
The disadvantages of CMOS APS include the need for 0.5 micron (or less) CMOS processes to achieve small pixel size, the use of standard industry processes that result in non-optimal QE structures, and noise somewhat higher than scientific CCDs.

This paper will recap the state of the art in CMOS APS technology but the main focus of the paper will be to project future successes and difficulties in the development of CMOS APS technology. Scaling issues and technology issues will be quantitatively addressed. A guess-timate for the eventual evolutionary departure of CMOS image sensors from mainstream CMOS will be presented.

As at the last meeting, the major goal of the paper is to stimulate significant discussion and thoughts about this rapidly emerging technology.



256 x 256 ACTIVE PIXEL IMAGE SENSOR WITH ON-CHIP TIMING AND CONTROL ELECTRONICS



256 x 256 ELEMENTS
1.2 μ m CMOS (HP)
20.4 μ m PIXEL
PHOTOGATE APDS DESIGN

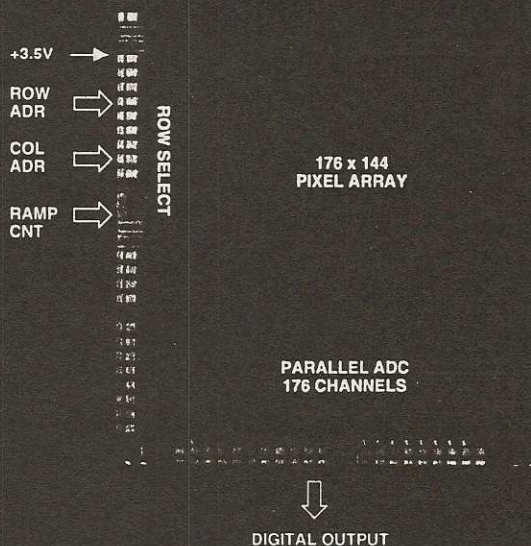
FPN SUPPRESSION
WINDOW READOUT
PROGRAMMABLE INT TIME

SATURATION 850mV
NOISE 13 e⁻
DYNAMIC RANGE 76 dB
CONVERSION 10 μ V/e⁻
FPN 0.24% sat
RT DARK CURR 29 mV/s

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CMOS ACTIVE PIXEL SENSOR WITH ON-CHIP ADC JPL/ATT TECHNOLOGY COOPERATION AGREEMENT



TECHNOLOGY: 0.9 μ m N-WELL CMOS
ACTIVE PIXELS: 20 μ m PHOTOGATE
ADC ARCHITECTURE: COLUMN-PARALLEL
ADC TYPE: 8 BIT SINGLE-SLOPE
SUPPLY VOLTAGE: 3.5 VOLTS
POWER: 35 mW
FRAME RATE: 30 Hz
FIXED PATTERN NOISE: <10 LSBs

PRINCIPAL DEVICE TECHNOLOGY CHARACTERISTICS

YEAR (1st DRAM shipment)	1980	1983	1986	1989	1992	1995	1998	2001	2004	2007	2010
Minimum lithographic feature size (0.7x/gen) [μm]	2	1.5	1.0	0.7	0.5	0.35	0.25	0.18	0.13	0.1	0.07
Isolation	LOCOS	LOCOS	LOCOS	LOCOS	LOCOS	LOCOS, STI	STI	STI	STI	STI	STI
Gate Oxide [nm]	41-71	29-50	20-35	14-24	10-17	7-12	4-6	4-5	2.7	1.9	1.9
Gate Electrode	n+poly	n+poly	n+poly	n+poly	n+poly	n+poly	n+poly	n+poly	n+poly	n+poly	n+poly
Substrate doping [cm^{-3}]	10^{16}	2×10^{16}	4×10^{16}	8×10^{16}	1.2×10^{17}	2.5×10^{17}	3.4×10^{17}	5×10^{17}	7×10^{17}	1×10^{18}	2×10^{18}
Source/drain junction	abrupt	abrupt	LDD	LDD	LDD	LDD, S/D ext	LDD, S/D ext	LDD, S/D ext	LDD, S/D ext	LDD, S/D ext	LDD, S/D ext
Source/drain junction depth [μm]	0.5-0.6	0.45-0.55	0.5-0.5	0.35-0.45	0.3-0.4	0.2-0.3	0.1-0.15	0.05-0.1	0.05-0.1	<0.05	<0.05
Power supply [V]	5	5	5	5	5/3.3	3.3/2.5	2.5	1.2-1.8	1.2-1.5	<1.2	<1.2
Threshold voltage [V]	1.0	0.9	0.8	0.7	0.6	0.5	0.45	0.4	0.3	0.3	0.3
Threshold voltage variation [$\pm$ mV, wafer-wafer]	170	125	80	75	70	60-70	50	40	30	25	20
DRAM bits/chip (4x/generation)	64K	256K	1M	4M	16M	64M	256M	1G	4G	16G	64G
DRAM chip size (1.5x/generation) [mm^2]	27	40	60	90	130	190	280	420	640	960	1400
DRAM cell size (0.4x/generation) [μm^2]	146	58	23	9.4	3.75	1.5	0.6	0.24	0.096	0.038	0.015
SRAM bits/chip (4x/generation)	16K	64K	256K	1M	4M	16M	64M	256M	1G	4G	16G
SRAM chip size (1.5x/generation) [mm^2]	31	47	70	100	150	220	330	490	740	1100	1600
SRAM cell size (0.4x/generation) [μm^2]	781	313	125	50	20	8	3.2	1.3	0.52	0.21	0.08
CMOS APS pixel pitch (0.7x/generation, 20L) [μm]	40	28	20	14	10	7	5	5	5	5	5
CMOS APS image pixel size (0.5x/generation, 20L) [μm^2]	1600	800	400	200	100	50	25	25	25	25	25
CMOS APS fill factor	25	25	25	25	25	25	25	25	25	25	25
Imager format size (HDTV)					1"		2/3"		(1/3")		
Imager format size (NTSC-TV)		1"		2/3"		1/3"	1/4"				

E.R. Fossum and P. H.-S. Wong, *Future Prospects for CMOS Active Pixel Sensors*, 1995 IEEE Workshop on CCDs and Advanced Image Sensors

Scaling Trend for CMOS APS

