Fabrication of epitaxial GaAs/AlGaAs diaphragms by selective dry etching

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A selective dry process is used to fabricate epitaxial diaphragms by etching anisotropic cavities through a GaAs substrate to an AlGaAs stop-etch layer. Active devices are built directly on the layers comprising the diaphragm. The etching process follows the device fabrication sequence, facilitating integration of these structures with pre-existing electronic circuitry. Potential applications in optoelectronic and acoustic wave devices are discussed, and an optical interconnection technique based on the diaphragm structure is described.

I. INTRODUCTION

Advanced semiconductor processing is now utilized in the production of miniaturized sensors and a variety of micromechanical transducer structures. Silicon is well suited to these applications because of its thermal and mechanical properties, and because highly developed electronic fabrication technologies have given rise to a precision micromachining capability.[1] GaAs does not possess all of the advantages of silicon, but it does share many of the fabrication technologies. It also presents similar opportunities for monolithic integration of control electronics. Furthermore, since GaAs is sensitive to a broader class of physical interactions than silicon, it is a very attractive material for transducer applications.

A majority of semiconductor microstructures have been fabricated by orientation-dependent wet etching of silicon,[2] and an increasing number of commercial transducers employing these structures have appeared. One example is the thin diaphragm piezoresistive pressure sensor,[3] which has found applications in the automotive industry and in biomedical research.[4] Highly anisotropic dry etching, generally free of crystallographic constraints, is preferable to wet etching for some types of micromachining. This is demonstrated by the use of reactive ion etching (RIE) in such fields as nanometer-scale fabrication, laser facet etching, and through-wafer via etching.[5–7]

The RIE process described below was developed in order to fabricate a specific structure: a deep backside cavity for coupling an optical fiber to a GaAs photodetector on the overlying epitaxial diaphragm.[8] Arrays of such structures, allowing many optical fiber interconnects to be addressed to a single GaAs integrated circuit, could significantly increase chip-to-chip communication bandwidths. Because the ultimate task of the cavity etching process is to produce a dense array of fiber coupling sites, realization of a minimum footprint for each individual coupler is a major concern.

II. STRUCTURE

Figure 1 shows a schematic diagram of two adjacent epitaxial diaphragms. The uppermost layer (n-GaAs) contains metal–semiconductor field effect transistor (MESFET) circuitry, and the undoped GaAs layer accommodates metal–semiconductor–metal (MSM) photodetectors. These are only representative of the sort of device designs which might be placed on top of the AlGaAs stop-etch layer. The etched substrate is semi-insulating GaAs, oriented 2° off (100) towards [011].

The layers were grown in a barrel-type metal–organic vapor phase epitaxy (MOVPE) system using trimethylgallium, trimethylaluminum, arsine, and disilane. The system was operated at 78 Torr and the substrate temperature was 650 °C. A growth rate of 0.07 μm/min was maintained throughout the run. Aluminum composition was measured by low-temperature photoluminescence and an upper limit on carrier concentration (5×10^{14} cm^{-3}) in the two undoped layers was determined by C–V profiling with evaporated Schottky diodes.

To etch cavities from the backside to the GaAs/AlGaAs diaphragm, a pure CCl_2F_2 rf discharge was used. (Al,Ga)As etch rates in CCl_2F_2 are known to decrease with increasing Al mole fraction, and a selectivity (GaAs/$Al_xGa_{1-x}As$ etch rate ratio) on the order of 200 (for $x = 0.3$) has been achieved by several groups.[9,10] The reduced AlGaAs etch rate is due to the formation of a <30-Å-

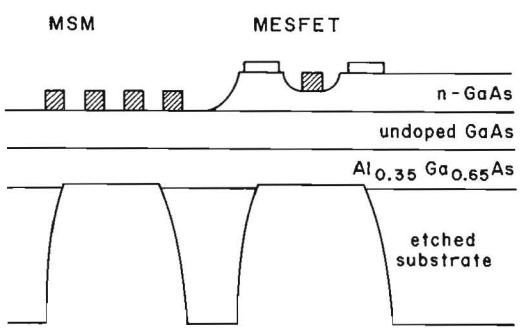

FIG. 1. Schematic diagram of an epitaxial (Al,Ga)As membrane spanning two cavities etched through semi-insulating GaAs. The fabricated structure consists of (from top down): 0.4-μm n-GaAs ($N_{Si} = 5\times10^{16}$ cm^{-3}), 1.0-μm undoped GaAs, and 4.5-μm undoped $Al_{0.35}Ga_{0.65}As$.

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thick layer of nonvolatile reaction products, primarily AlF_3.[11]

The high selectivity permits uniform termination of cavities reaching through several hundred microns of GaAs on a relatively thin AlGaAs layer. Thickness and etch rate variations across a sample must also be controlled to achieve uniformity, and vertical anisotropy is needed to minimize the spacing between adjacent diaphragms in an array. Figure 2 shows a scanning electron micrograph of a single cleaved diaphragm, etched through a circular Ni mask opening 200 μm in diameter.

III. FABRICATION PROCESS

In most experiments, the samples went through a standard device fabrication sequence prior to the RIE processing. MESFET's were fabricated in the uppermost (n-GaAs) layer. The process steps were NH_4OH/H_2O_2 etching of isolation mesas, deposition and annealing of AuGe for Ohmic contacts, and evaporation of Al for Schottky gates. The devices were then protected by mounting the sample face down in glycol phthalate on an oxidized silicon wafer; this wafer served as a sample holder for the remainder of the processing.

Front-to-back alignment was achieved using an infrared ir camera (sensitive up to 1.8 μm) attached to a Karl Suss submicron aligner. This allowed accurate positioning of the cavity etch site with respect to the front-surface circuitry, as the photograph in Fig. 3 demonstrates.

Two separate RIE steps, each less than 2 h in duration, were performed in the course of diaphragm fabrication. A commercial 13.56-MHz system (Electrotech PF 340) with a nitrogen-purged glove box and a base chamber pressure of $\sim 5\times 10^{-5}$ Torr was used. Thermal mass-flow controllers and a butterfly valve/capacitance manometer combination were used to adjust the gas flow and pressure.

First, the sample thickness was reduced from 500 to < 250 μm by etching from the backside under the following conditions: pressure = 8 Pa (60 mTorr), rf power density = 0.5 W/cm^2, CCl_2F_2 flow rate = 35 std. cm^3/min (sccm). The etch rate for this process was 2.5 μm/min; its purpose was to mitigate the effects of lateral undercutting and mask erosion during the cavity etch (second RIE process). After thinning, the back surface of the sample was mechanically polished to a smooth finish and liftoff was used to pattern a Ni mask for the subsequent RIE.

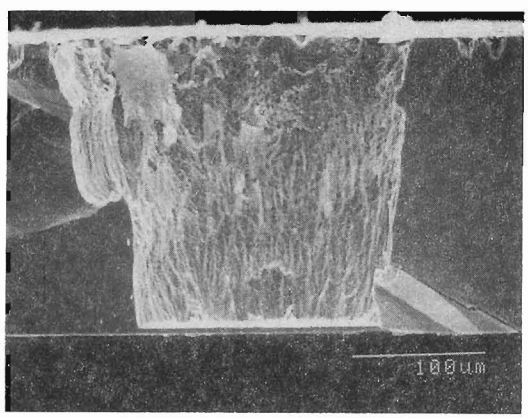

FIG. 2. Cross-sectional scanning electron micrograph of an etched cavity terminating on an epitaxial GaAs/AlGaAs layer membrane (GaAs face down).

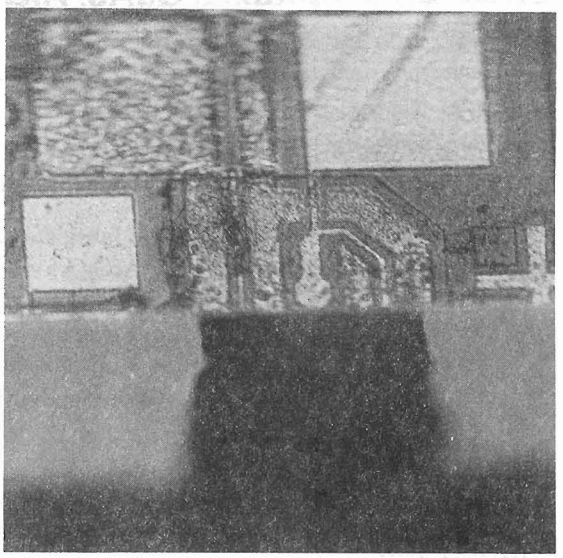

FIG. 3. Cutaway view of a cleaved sample, demonstrating the alignment of a backside fiber-coupling cavity with a photodetector on the front surface.

Wafer thinning, a common procedure among semiconductor manufacturers, is normally done with the aid of expensive mechanical equipment and a supply of abrasive and/or chemically reactive solutions. RIE was found to be a practical alternative, in light of the existing equipment. The maximum variation across a 1-cm^2 sample, due mostly to the polishing step, was typically ~ 30 μm, as measured by a dial thickness gauge.

The cavity etching process was performed at 5-Pa (38-mTorr) pressure, with an applied rf power density of 0.4 W/cm^2 and CCl_2F_2 flow rate of 25 sccm. The self-induced bias on the driven sample electrode was -400 V, and the gas residence time was 0.1 s. A GaAs/$Al_{0.35}Ga_{0.65}$ As etch rate ratio between 30 and 50 was obtained for this process. The average GaAs etch rate in the vertical direction was 2.2 μm/min with a run-to-run variation of $\pm$ 10%. The vertical-to-lateral etch rate ratio was ~ 11, so that after a typical 100-min process, the total undercut at the mask/substrate interface is ~ 20 μm. Lateral etching is difficult to avoid at pressures sufficient to give both a high GaAs etch rate and a good selectivity.

Upon completion of the cavity etch, the AlGaAs surface was cleared of residual GaAs by etching the sample for a few minutes with a pH 7 solution of NH_4OH in H_2O_2. A clean circular diaphragm resulted, with thickness equal to that of the as-grown layers minus the depth etched into AlGaAs. The AlGaAs etch rate for the RIE process was low enough (< 0.06 μm/min) so that even extended overetching (on the order of 20 min) does not reduce the diaphragm thickness by more than ~ 1 μm. The NH_4OH/H_2O_2 solution did not noticeably etch the AlGaAs layer.

IV. DISCUSSION

The technique described in this paper is expected to be useful in several areas of GaAs device fabrication since its only compositional requirement is the inclusion of a stop-etch layer. There exist several potential applications of the cavity/diaphragm structure in the fields of (Al,Ga)As optoelectronics and bulk-acoustic-wave (BAW) devices.

For example, the responsivity of conventional photodetectors is usually reduced due to shadowing by the front surface metallization. This problem can be avoided by backside illumination, but only when the substrate is transparent to the light signal, as in GaInAsP/InP structures. In the (Al,Ga)As system this is not the case, and limited-area removal of the opaque GaAs substrate was thus suggested as a means of improving optical coupling.[12] The wet etching process used for this purpose wastes considerable on-chip real estate, but the highly anisotropic RIE process does not.

The technique should also allow practical realization of new optoelectronic device concepts. A number of high-performance (Al,Ga)As devices described recently have been mounted as ultrathin membranes on glass substrates.[13,14] The selective RIE process offers a more reliable means of accessing the active layers.

BAW devices are used for precision frequency control in VHF communications. Most hybridized acoustic wave sources use quartz resonators. GaAs, because of its piezoelectric properties, is an alternative material, and there has been interest in the monolithic integration of electronic and acoustic wave devices on GaAs substrates.[15] In quartz, mechanical polishing techniques are used to fabricate BAW devices with thicknesses down to $\sim 30\,\mu$m; these oscillate at ~ 50 MHz. More sophisticated processes, including reactive ion beam etching,[16] are used to achieve ultrathin diaphragms (membrane BAW's) with higher oscillation frequencies. This approach may now be applied to GaAs-based devices, with precise thickness control made possible by epitaxial growth and selective etching of multilayer diaphragms.

V. CONCLUSION

A technique for micromachining GaAs-based epitaxial diaphragms has been developed. The reactive ion etching process used allows these microstructures to be integrated with device electronics in a flexible and real-estate efficient manner. Potential applications in the areas of optoelectronic and acoustic wave devices have been identified.

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