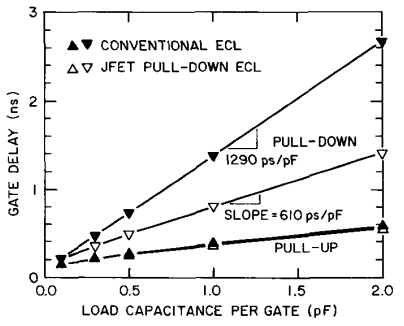

Fig. 10. Simulated delay versus load capacitance at 1 mW/gate for the JFET pull-down ECL circuit and the conventional ECL circuit (FI = FO = 3).

Notice that the pull-down current of the new circuit has a sharper peak. The pull-down current contours of the new and conventional ECL circuits versus output voltage during transitions are shown in Fig. 9 for both the high-power (4 mW/gate) and low-power (0.5 mW/gate) cases. As expected, the contours for the JFET pull-down circuit show that a higher current modulation is obtained at 0.5 mW/gate than at 4 mW/gate due to the longer delay in the output stage.

The superior load driving capability of the new ECL circuit is illustrated in Fig. 10. As can be seen, at 1 mW/gate, the pull-up capability is essentially identical while the slope of the pull-down delay for the new circuit is 610 ps/pF, an improvement of 53% compared with 1290 ps/pF for the resistor pull-down circuit.

V. Conclusion

In conclusion, an active pull-down ECL circuit using a "free" p-channel JFET in n-p-n bipolar technologies has been described. The JFET pull-down output stage operates as a push–pull follower stage and enhances both the speed and driving capability. For a loaded gate at 1-mW power consumption, the enhancement is about 24% and 53%, respectively. Because the JFET pull-down ECL circuit will neither degrade the circuit density nor complicate the fabrication process, it is suited for low-power high-speed applications. The JFET pull-down technique can also be applied to other logic circuits such as NTL circuits and, more broadly, to any emitter-follower drivers.

Acknowledgment

The authors would like to thank M. Arienzo, R. Isaac, and L. M. Terman for the encouragement.

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Digitally Programmable Gain Control Circuit for Charge-Domain Signal Processing

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***Abstract*—A simple, nearly passive circuit for programmable gain control of charge-domain signals is described. The circuit is functionally equivalent to a multiplying digital-to-analog converter (MDAC) and is implemented in a 3-μm double-poly, double-metal CCD process. Two implementations of the circuit are reported: a single-stage recursive converter, and a ten-stage pipeline converter. The latter occupies 0.4 mm² of chip area and consumes approximately 2 μW for a 1-kHz conversion rate. The circuit is shown experimentally to have an 8-b equivalent accuracy in both differential and integral linearity and is expected to find application in focal-plane image processing for both detector nonuniformity correction (NUC) and convolution weighting.**

Manuscript received August 10, 1990; revised November 8, 1990. This work was supported by an Analog Devices Career Development Award and the NSF/ERC program at Columbia University.

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IEEE Log Number 9042338.

I. Introduction

FOCAL-PLANE image processing is the integration of image acquisition and image preprocessing functions on the same or an adjacent chip, and has recently become of increasing interest to both the aerospace and robot vision communities. The realization of a focal-plane image processor can be achieved in a variety of ways employing both monolithic integration and hybridization. The major emphasis in focal-plane image processing is the preprocessing of

detector array signals in the analog domain prior to analog-to-digital (A/D) conversion, thus reducing throughput requirements on subsequent downstream digital electronics. The realization of such processing requires analog circuits that are efficient in their use of chip area and power, though in most applications, accuracy of the order of one part in 256 (eight equivalent digital bits) is adequate. CMOS and CCD technologies are employed for their low power and chip area requirements, as well as their compatibility with detector signal multiplexing circuitry [1].

For several applications of focal-plane image processing, programmable gain of the analog signals would be useful. For example, in convolution operations, pixel values are weighted and summed over a local neighborhood. To conserve chip area, the same gain control circuit could be time multiplexed for different weights, if that gain control circuit were digitally programmable. In this application, approximately 5 equivalent bits of resolution are required. A second example is detector nonuniformity correction (NUC). Detector arrays fabricated from nonsilicon materials typically suffer from nonuniformity in illumination response, and thus require both offset and gain correction to provide high-quality imaging performance. The nonuniformity is usually of the order of 10–20% and is due primarily to material imperfections. While presently performed off-chip in the digital domain following A/D conversion, gain and offset correction can be performed on-chip if the correction coefficients are stored following imager calibration. Such correction is necessary for performing subsequent image preprocessing functions to avoid erroneous results. In this case, approximately 8 equivalent bits of resolution are required. In both applications, gain less than unity and single-quadrant operation are sufficient, with conversion rates in the kilohertz range.

Few, if any, prior MDAC designs are appropriate for these applications. The signal is usually in the charge domain, and conversion to the voltage domain would typically require a power-consuming source-follower circuit. Furthermore, chip area is of prime concern so that MDAC approaches requiring area-ratioed capacitors are undesirable.

In this paper, a novel approach using charge splitting, routing, and summing is presented which achieves the performance goals described above.

II. Programmable Gain Control Circuit

The charge-domain programmable gain control circuit consists of three primary elements. These are a charge-packet splitter [2], a charge-packet router [3], and a charge-packet summing buffer. The elements are interconnected using the wire transfer technique [3], which allows a systematic design approach to charge-domain circuits and subsequent signal crossing. In this technique, charge is virtually transferred across a wire whose capacitance is kept small and whose voltage is kept constant. Wire transfer efficiency is approximately 0.998. The splitter divides a charge packet in two equal portions by splitting the active channel with a tapered field oxide. The accuracy of this element is expected to exceed one part in 1000. The router circuit selectively steers charge packets into one of two receiving wells using complementary electrodes. The router error is less than one part in 600. The summing buffer is a simple receiving well with hard-wired summation performed using the wire transfer technique.

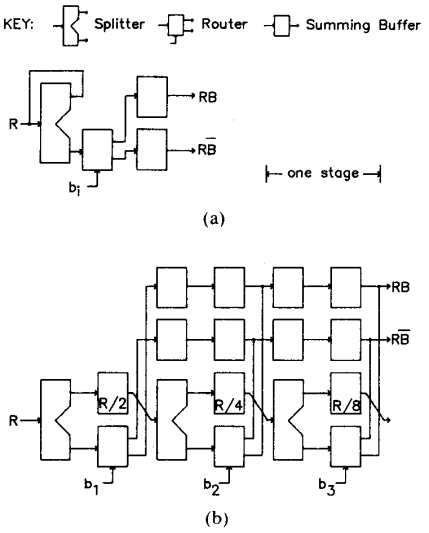


Fig. 1. Block diagram of programmable gain control circuit. (a) Serial recursive circuit. (b) Pipeline circuit.

A block diagram of the serial recursive MDAC is shown in Fig. 1(a). It consists of a splitter, router, and two complementary summing buffers. A reference charge packet R is transferred to the splitter and divided into portions of size $R/2$. One portion is rerouted to the splitter input, and the second is fed forward to the router. The latter portion is routed to one of the two summing buffers as selected by digital bit b_i (the MSB of the digital gain word in this case). The former portion is split again to form quantities of $R/4$ and the procedure is repeated using the next bit of the digital gain word to steer the charge packet. This process of forming output packets by serially splitting and steering n packets is the basis of the serial recursive MDAC. The output packet RB is given by

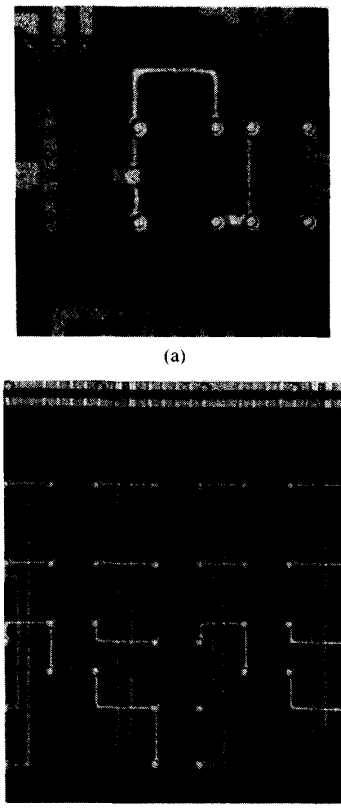
$$RB = \sum_{i=1}^{n} b_i R/2^i.$$

The complementary output $R\bar{B}$ is simply

$$R\bar{B} = R - RB - R/2^n$$

where the last term represents the charge remaining in the pipeline. The resolution of the converted data is thus limited by the number of repetitions of the process, and the accuracy by the intrinsic accuracy of the circuit elements.

The pipeline implementation of the programmable gain control circuit trades chip area for increased throughput and is suited for NUC [4]. A block diagram of the pipelined MDAC is shown in Fig. 1(b). In this implementation, the packet portion fed back in the serial recursive MDAC is instead fed forward to a second splitter stage. The accumulated signal in the summing buffers is also fed forward to a pipeline of summing buffers. Each stage of the pipeline corresponds to a successive bit in the digital gain word and consists of two substages. Each substage contains successive input charge packets. The first substage consists of two summing buffers and a splitter, and the second substage consists of three summing buffers and a router. The two upper summing buffers maintain the accumulated signal and



(a)

(b)

Fig. 2. Photograph of (a) serial recursive circuit and (b) single stage of pipeline circuit.

its complement, respectively. Thus, in this circuit, if the input packets are R_k, and if each packet is to be multiplied by a digital word B_k consisting of bits $b_{k,i}$, then with analog signal R_k entering the MDAC, the digital bit at stage j must be $b_{k-2j+1,j}$.

III. Experimental Results

Both the serial and the pipeline circuits were realized using a 3-μm double-poly, double-metal, surface n-channel process in a commercial CCD foundry process. The nominal channel width of the circuit elements was 50 μm. The wire transfer interconnect structure had a first barrier gate length of 3.0 μm and a second barrier gate length of 2.5 μm. The CCD electrode transfer length was 3.5 μm leading to a characteristic diffusion limited transfer time of 20 ns. Substrates were p/p^+ epitaxial layers with a nominal doping of $1.5\times10^{15}/cm^3$ and the effective gate dielectric thickness was 86 nm. The devices were implanted for a threshold voltage of 0.5 V.

The pipeline implementation was built as a ten-stage device with simple cross-coupled NMOS flip-flop circuits used to latch the digital data and provide complementary drive signals to the router elements. A fill-and-spill input structure was used to generate the input charge packets, and a floating-diffusion dual-stage source-follower output amplifier (with on-chip load and sample/hold) was used for output.

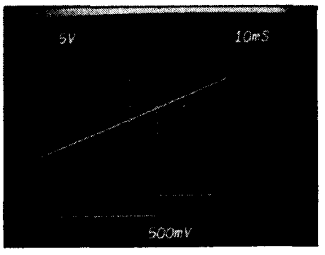


Fig. 3. Oscilloscope photograph showing analog output of pipeline programmable gain control circuit in response to a digital ramp (upper trace) and MSB of digital control word (lower trace).

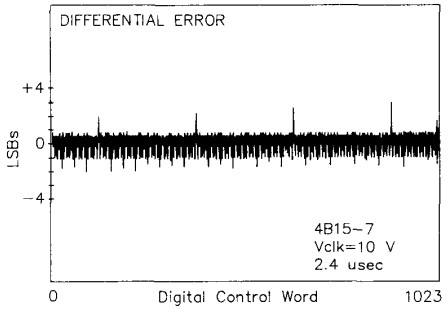


Fig. 4. Differential linearity error of pipeline circuit. Note that the 1-LSB tic mark corresponds to 1/1024th of full scale.

Integral nonlinearity introduced by the output amplifier is an artifact of charge-to-voltage conversion, but in practice was negligible. The size of each stage of the pipeline circuit (excluding flip-flop) was 130 μm$\times$300 μm, but could be reduced by at least 50% with little effort, as can be seen in Fig. 2(a).

The serial implementation takes considerably less chip area, and the circuit was approximately 100 μm$\times$130 μm, as seen in Fig. 2(b). The output summing buffer of Fig. 1(a) was omitted, and the signal was summed on the floating diffusion of the output amplifiers.

Fabricated parts were tested using a programmable data generator for timing and level shifters to form the clock drive signals. A laboratory IBM PC/XT was used to apply digital gain control words and digitize (12 b) the MDAC analog output. Scaling and dc offset were performed by a preamplifier. All codes were applied to the circuit and it was characterized in accordance with published standards [5]. The circuits were operated with quasi-two-phase clocks and 10-V buckets, corresponding to a maximum charge handling capability of 5×10^6 electrons and a power dissipation of 0.2 μW/stage/kHz.

The analog ramp output of the pipeline circuit in response to a digital ramp is shown in Fig. 3. The dynamic range of the analog input (R) was approximately 30 dB with maximum resolution (10 b) obtained for a full bucket and decreased resolution for smaller buckets as would be expected. The circuit was tested at frequencies as high as 8×10^6 conversions/s with results limited by test station drive capability. Computer data acquisition was made at a test frequency of 0.4×10^6 conversions/s. The differential linearity of the circuit is shown in Fig. 4. Note that the error is

TABLE I
CCD PROGRAMMABLE GAIN CONTROL CIRCUIT PERFORMANCE SUMMARY

	Pipeline	Serial
Technology	3-μm CCD	3-μm CCD
Circuit Size	0.4 mm^2	0.013 mm^2
Resolution	10 b	variable
Integral Linearity	8 b	6 b
Differential Linearity	8 b	6 b
Clock Voltage	10 V	10 V
Bucket Cap. (electrons)	5×10^6	5×10^6
Power (10^3 conv/s)	2 μW	2 μW
Max. Conversion Rate	$>8\times10^6$/s	$>0.5\times10^6$/s

characterized in terms of number of LSB's (10th bit), i.e., an error of 4 LSB's corresponds to an 8-b differential linearity. Integral linearity was also 8 b. The major error occurs for code changes corresponding to the third stage splitter and can yield nonmonotonicity. This error could be shifted to higher or lower bits, depending on clock transition times. This sensitivity to transition time is attributed to the trapping effects in the nitride-oxide dielectric.

The serial recursive MDAC circuit was tested using a TTL circuit to multiplex (serialize) the digital control word. The performance of the serial MDAC was limited to approximately 6-b differential and integral linearity with 7-b resolution. This reduced performance (compared to the pipeline implementation) also implicates the dielectric structure, since the interconnect node sees a strongly time-varying charge compared to that of the pipeline circuit. Accumulation of process- and device-induced errors (canceled out in the pipeline MDAC) may also contribute. It is expected that a buried-channel implementation of the serial circuit would achieve significantly better performance, due to the improved operation of the wire transfer process [3]. The performance of the circuits is summarized in Table I.

IV. CONCLUSIONS

A simple, nearly passive circuit for digitally programmable gain control of charge-domain signals has been presented. For focal-plane image processing applications, the circuit meets the performance requirements with low chip area and power dissipation. The circuit may find application in other charge-domain circuits as well.

ACKNOWLEDGMENT

The technical assistance of S. Mendis and P. Ronen and discussions with Prof. Y. Tsividis are gratefully acknowledged.

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