DETECTOR ARRAYS FOR DIGITAL HOLOGRAPHIC STORAGE APPLICATIONS

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Introduction

This chapter discusses detectors for holographic data storage applications. While it may be possible to use a single detector or linear array of detectors, the focus here is on 2-D arrays of pixels. There are many considerations for the detector array when designing a complete system that arise from the intimate relationship between the holographic storage system, optical readout technique and the sensor pixels. The chapter begins with a discussion of these considerations, based on the assumption that commercially viable digital holographic data storage (DHDS) systems must be "smaller than a breadbox," be affordable, have data capacities in the hundreds of gigabytes arena, and have readout rates in the regime of hundreds of megabytes per second. Today there are two primary technology choices for realization of the sensor array, charge-coupled devices (CCDs) and CMOS (complementary metal-oxide-semiconductor) active pixel sensors (APS). Both will be introduced and their relative merits presented. In fact, the CMOS APS, a much newer technology, will be shown to offer significant advantages over its predecessor, the CCD, when applied to digital holographic data storage systems.

A 816x616 element, 17 μm pixel pitch CMOS APS detector array designed for DHDS applications[1].

General considerations for detector arrays

In digital holographic data storage (DHDS) systems, the sensor array plays the critical role of converting optical data signals into electronic data signals. These optical data signals generally come in the form of a "page," or two-dimensional array, of bright and dark spots of light. The sensor array must then be aligned and physically matched with the optical system such that each spot of incoming (readout) light is incident on one, or a small collection of, prespecified sensor array

pixel(s). Such a criterion places stringent demands on the sensor array's linear and angular attitudes, as well as pixel pitch. The sensor array must also be highly sensitive to the particular wavelength(s) of the readout light, as average light levels will typically be quite low (< 10,000 photons per pixel per read). Furthermore, the sensor array must be capable of converting and delivering 10 – 100 user megabytes per second. These and other considerations will be addressed in the following three sub-sections.

Size, power and cost

Because it is preferred to have memory systems that are small, low power, and affordable, there are certain systems considerations that must be addressed in choosing or designing a sensor array for DHDS.

Perhaps the most inclusive system-based concern to consider is that of overall size. High performance sensor array solutions must be found that are truly compact and/or self-contained (on the order of one to ten cubic centimeters).

In parallel with system size concerns are system power concerns. Most DHDS systems will want their complete sensor array subsystems to consume less than one or two watts. Beyond the general system-level requirement for low power consumption is the vital requirement for low heat generation within the sensor array and its housing. Material dimensions are thermally dependent and sensor array alignment must be maintained to within a few microns for good system performance. In most systems, just a few degrees of temperature change at or near the sensor array plane can shift the sensor array out of alignment with the incoming optical data page.

There is at least one point of relief for sensor array requirements. Since DHDS systems expect the "images" they are receiving to be rather noisy, containing perhaps hundreds to thousands of data bit errors in every page, pixel defects in the sensor array are not much of a problem. Embedded error correction codes (ECC) in the data pages will also correct for pixel defects. Thus, the effective yield in the manufacturing of the sensors will be higher, reducing sensor manufacturing cost.

Number of pixels, readout rate, and pixel size considerations

Because it is preferred to have memory systems with high storage densities (for high capacity in small volumes) and fast data readout rates, there are certain data density and data rate considerations that must be addressed in choosing or designing the sensor array.

One element that must be considered in designing sensor arrays is their space bandwidth product (SBP). For a sensor array, the SBP is equal to the total number of pixels. (The "space" part has to do with the total photosensitive array area, and

the "bandwidth" part has to do with the solid diffraction angle of the incoming light cone required to focus to a pixel-size spot). Typically, DHDS systems are designed for use with megapixel arrays (commonly, 1024 x 1024 arrays are used as a benchmark). There are two main reasons for this choice. First, accessing data consists of a seek step and a read step. If the seek step is relatively long, then one wants to read as much data as possible per step. The second reason has to do with storage density; the higher the sensor array's SBP, the more data bits one can store in a single hologram.

The readout rate of the sensor is also very important, and needs to be in the hundreds of megapixels/sec range. It can be shown that with a megapixel sensor array, a good performance holographic storage material, a 100 mW laser source, and a holographic storage density on the order of 500 channel bits per square micron, it is possible to achieve sustained user data recall rates in excess of 100 megabytes per second. At these impressive storage densities and data rates (e.g., 300 gigabytes read out at 100 user megabytes per second) it would still take nearly one hour to read a single disk.

Pixel size affects the optical design as well as the sensor cost. For a given SBP, sensor array cost scales approximately as the fourth (4^{th}) power of the linear dimension of the pixel since chip areal size affects not only how much silicon is used per chip but also chip yield. Thus, smaller pixels generally result in a less expensive chip. On the other hand, once some critical dimension is reached (say, 5-10 μm for a megapixel image sensor) the cost of the optics starts to climb rapidly. Small, random (<1%) lens distortion could be disastrous in mass-produced systems. Furthermore, 1:1 pixel-size matching between the "write" SLM and the sensor pixels simplifies optical system design. Thus, pixel sizes of the order of 5-20 μm are best. Of course, it may prove worthwhile in some systems to design sub-spot size sensor array pixels. In this manner, "oversampling" can be performed (detecting each data spot over several sensor array pixels).

Noise, dynamic range, and analog-to-digital converter resolution

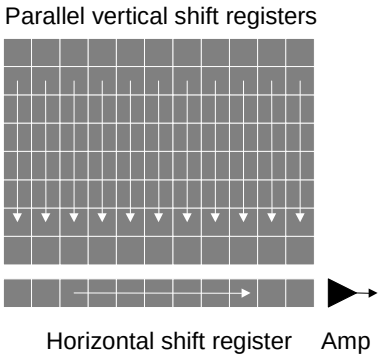
One of the pacing items in DHDS design is the uniformity of the read out image. A variation of 10:1 in page intensity across the array is possible, as well as page-to-page intensity variations. In this case it is possible to have 5000 photons incident on one pixel, and 500 photons on another, resulting in signals in the 100-1500 electrons level. For detector arrays more photons is almost always better but for DHDS systems this means high power dissipation and/or slower access times. Thus, the read noise of the sensor needs to be in the sub-20 electrons rms level, with lower noise floors yielding lower power dissipation and/or faster access times.

In the real world, the optical data page emanating from the holographic storage medium will contain various forms of noise. These noise sources include inter-

page cross-talk, intrapage cross-talk, point defect scattering (due to pits, protuberances, dust, or smudges on the various optical surfaces, or bubbles, density gradients, dopant gradients, or debris in the bulk of the optical elements), and harmonics due to nonlinear effects in recording and/or readout. They will generate optical noise that must be discriminated from the optical signal. Generally, these noise sources will contribute up to 50% of the total light reaching the sensor array. Because of these noise sources, and the page intensity non-uniformity, there is a useful limit on the resolution of the ADC used in the sensor array. Generally, that limit is roughly five to eight bits.

Detector Array Choices

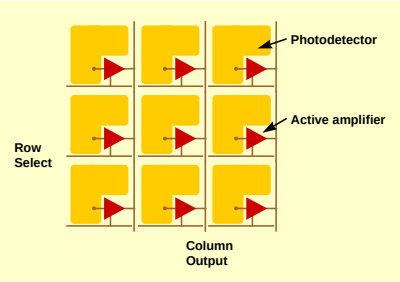
There are several types of detector arrays that can be considered for DHDS systems. These are charge-coupled devices[1] (CCDs), photodiode arrays, charge-injection devices (CIDs), and CMOS (complementary metal-oxide-semiconductor) active pixel sensors[2] (APS). Of these, the two leading contenders are CCDs and CMOS APS. The others suffer from a combination of high readout noise and slow speed.



CCDs work by shifting out photogenerated charge to a common amplifier.

In both CCDs and CMOS APS, incident photons are absorbed in the silicon and converted to electrons. The main difference between CCDs and CMOS APS is in the readout technique. In addition, CMOS APS, being fabricated from mainstream microelectronics technology, is readily integrable with other on-chip circuits to form a "camera-on-a-chip" that has many significant advantages over a CCD-based system[3].

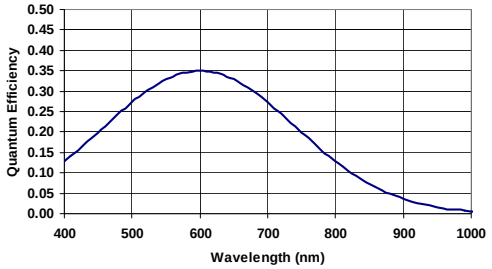
For a CCD, after the signal is collected and integrated, it is shifted out in a series of thousands of steps, each shifting the collected electrons one pixel at a time until the signal reaches the corner of the array. There the electrons are converted to a voltage by an output amplifier that has a *conversion gain*, typically in the range of 10-20 μV per electron. Access to a particular pixel is serial, that is, to read a particular pixel, all pixels before it must be read out first. Furthermore, to avoid losing electrons in the shifting process, the readout speed is limited to typically 10 Mpixels/sec, and a maximum value of approximately 30 Mpixels/sec. The voltage from the output amplifier is then driven off-chip to ancillary electronic chips that may perform noise reduction and analog-to-digital conversion (ADC).



Active pixel sensors contain an amplifier in each pixel, and the signal is read out over X-Y wires

In the CMOS APS, each pixel contains an amplifier than converts the electrons to a voltage within the pixel. The voltage signal is readout through a matrix of X-Y wires, allowing independent access to each pixel. Thus, any pixel can be selected for read out. In practice, an entire row of pixels is addressed at a time and their output voltages transferred to an analog signal processor located at the bottom of the array where noise reduction and ADC takes place. This on-chip circuitry in addition to on-chip timing and control circuitry permits the realization of an electronic camera-on-a-chip.

Quantum Efficiency



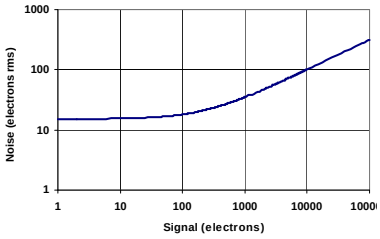
Representative QE of typical CCDs and CMOS APS detector arrays.

Quantum efficiency (QE) measures the ratio of collected signal carriers to incident photons across an entire pixel. Thus, if the quantum efficiency is, say 30% at 550 nm for a pixel, and 1000 photons are incident on the pixel, then 300 electrons are collected. Since both CCDs and CMOS APS are made from the semiconductor silicon, they have similar quantum efficiencies and are generally responsive from ultraviolet to the near infrared (e.g. 300 – 1000 nm). The peak value of QE typically occurs between 500 and 600 nm and can vary from as high as 70% in specialized (expensive) CCDs to perhaps 20% in commercial CCDs. CMOS APS devices typically peak at about 30%-40%, but this can also vary significantly with design.

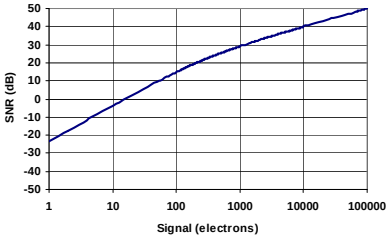
The sensitive portion of the pixel is typically less than the entire pixel size. The ratio of sensitive area to total pixel area is called *fill-factor* and is often less than 50%. It is possible to put an array of microlenses over the pixel array to concentrate the incident light on the sensitive area as a backend step to the normal device fabrication process, but microlenses work best for normally incident photons, and their efficiency drops rapidly for non-normal incidence.

Noise

Noise is an important consideration, especially when power and throughput need to be optimized. Temporal noise in detector arrays come from photon shot noise (inherent in the photonic signal incident on the array) which varies as the square root of the number of incident photons or collected electrons, and readout noise introduced in the readout and conversion of the signal to a voltage. The latter is often independent of the signal. In a CCD, all the signal charge is converted by a single amplifier so it must operate at a higher frequency and consequently its noise is higher, e.g., 20-40 electrons rms at 10-30 Mpixels/sec. (Very low noise, e.g., 1-5 electrons rms can be obtained in scientific CCD systems, but only at very low readout rates of 0.05-0.5 Mpixels/sec). In a CMOS APS, low noise of 5-15 electrons rms can be achieved even at high readout speeds because each column may have its own amplifier. This *column-parallel* architecture reduces the frequency of the amplifier and the noise is lower. Additional noise can be introduced in the analog-to-digital converter (ADC). Again, a column-parallel architecture for on-chip ADC also reduces noise at the expense of complicated chip design. High-speed column-parallel ADCs with resolution up to 10b have been demonstrated with CMOS APS devices4.



Noise as a function of signal.



SNR as a function of signal.

Another source of noise is dark current. This is the signal detected by the pixel in the absence of light and is due to thermally generated electrons rather than optically generated electrons. Like optical shot noise, the noise in this dark signal varies like the square root of the number of carriers. Dark signals in high speed CCDs and CMOS APS are of the order of 500-5000 electrons/sec/pixel so for 1 msec integration times (1 kHz frame rates) dark noise is only of the order of 1-3 electrons rms, but can be substantially more for slower operation.

Shown above is noise vs. signal and signal-to-noise ratio (SNR, expressed in dB as 20log[SNR]) vs. signal where read noise is taken to be 15 electrons rms and dark noise 2 electrons rms. Each curve has two parts – for lower signals, noise or SNR is dominated by read noise, and for higher signal levels, noise and SNR is dominated by photon shot noise. Typically it is SNR that is important in detection.

Readout rate

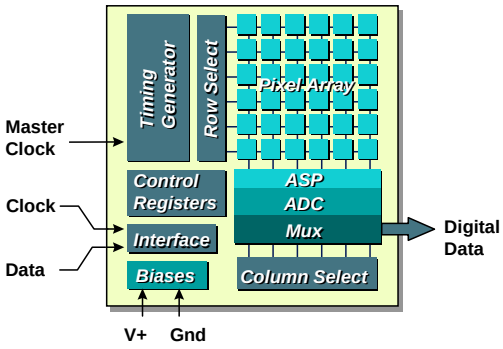
In a CCD, readout rate is typically limited to 10-30 Mpixels/sec per readout channel. High speed CCDs have been built with multiple readout channels per chip to achieve high frame rates. Kodak has built and demonstrated, in conjunction with IBM, a 1024x1024 element CCD operating at nearly 1000 frames per second using 64 parallel readout channels each operating at 15 Mpixels/sec[5].

In CMOS APS, the analog signal chains (typically one per column) and ADCs (also one per column) are integrated on chip. To date, the highest throughput CMOS APS device has been demonstrated by Photobit Corporation. That device, developed for the US Government, has 1024x1024 elements and has been operated at over 500 frames/sec with 8b digital output (524 Mpixels/sec) and dissipates approximately 0.350 W at 3.3 volt operation[6]. It is expected that 1000 Mpixels/sec can be achieved in the next generation.

System Implementation

In a CCD, it is difficult to have so many parallel readout channels without the channels introducing crosstalk between themselves. In addition, each output channel requires a separate off-chip analog signal chain and ADC, corresponding to at least one printed circuit card per channel. Each channel needs to be well matched and to stay matched over system temperature variations.

CCDs also require many different voltage supply levels to allow them to operate with good charge transfer efficiency. Each CCD also requires a separate timing generator chip, and driver circuits for each "clock" signal – and often 10-16 different clock signals are required. Power dissipation of a high speed CCD system is of the order of 200 W and a separate cooling system is also required. Making a compact system (e.g., smaller than a breadbox) with this approach has not yet been demonstrated.



The CMOS APS lends itself to integration with timing generators, ADCs and other functions to reduce system component count and power.

For CMOS APS –based systems, the integration of the timing generator, drivers, analog signal chain and ADC significantly advances the ability to build a compact DHDS system. The use of a single supply voltage (e.g., 5V or 3.3V) and the full digital interface to the chip (no analog signals) greatly enhances faster readout, system design ease and increases system reli-

ability. Furthermore, the integration of additional circuits to perform 'smart' pre-processing of the output data (e.g., error correction) also greatly simplifies system design.

On-chip signal processing is a feature that can be invaluable in DHDS sensor arrays. As mentioned, one form of on-chip processing is that of analog-to-digital conversion. In addition to ADC, numerous other processes can be implemented such as error correction codes (ECC), localized auto-exposure, data decoding, calculations of bit value statistics, auto-start triggering, and data formatting (in preparation for data export). For example, in the case of on-chip differential data decoding, it has been demonstrated that sensor array readout rates can increase by a factor of more than 100[7].

Conclusion

While both CCDs and CMOS APS can be used for DHDS detector arrays, the actual and potential advantages of the CMOS APS technology are overwhelming. The major disadvantage of the high speed CMOS APS technology is a lack of widespread availability, although high speed, high performance CCDs are also not widely available. The availability of CMOS APS technology through off-the-shelf supply as well as custom design is expected to improve greatly in the next few years.

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