Cryogenic GaAs JFETs

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Abstract

Gallium arsenide junction field-effect transistors (GaAs JFETs) are promising for deep cryogenic (<10 K) readout electronics applications. This paper presents the structure and fabrication of GaAs (JFETs) and their performance at 4 K. It is shown that these JFETs operate normally at 4 K, with no anomalous behavior such as kinks or hysteresis. The noise voltage follows a $1/\sqrt{f}$ dependence and is approximately 1 $\mu V/\sqrt{Hz}$ at 1 Hz for a ring JFET that is 1250 μm in circumference and 20 μm long. The gate leakage current reaches 1 pA at a gate voltage of -6 V, and increases exponetially at approximately 1 decade per volt. The noise is within the limits of the requirements for typical VLWIR readout applications; the extrapolated gate leakage current at typical operating biases is higher than the required limit by two orders of magnitude. Planned improvements to reduce the leakage current are discussed.

1. Introduction

Future imaging instruments for very long wavelength infrared (VLWIR) will use detector arrays cooled to deep cryogenic temperatures (below 10 K), and will require readout electronics that operate at the detector temperature. For previous cryogenic arrays of only a few pixels, it had been possible to isolate the electronics in a warm compartment and run wires to each detector in the array. The large heat load carried by these wires, and their susceptibility to crosstalk and noise pickup makes this approach impractical for larger array formats that are planned for future space-based VLWIR imagers. For this reason, NASA has actively been exploring readout electronics which can be functional below 10 K. Typically, VLWIR detectors have very high impedance and low dark currents, so the readout input currents must be low. Also, the expected signals are small, requiring low amplifier noise to preserve the sensitivity. For example, the Space Infrared Telescope Facility (SIRTF) plans to use detectors cooled to 2 K that will require amplifiers with less than 10^{-17} amp input current, and with a noise of less than 1 $\mu V/\sqrt{Hz}$ at 1 Hz.

Readout electronics for the deep cryogenic temperature range is challenging because of the phenomenon of carrier freeze-out. It takes a small but finite energy to liberate carriers from dopant atoms in lightly or moderately doped semiconductors. At sufficiently low temperature the carriers lack the thermal energy to remain free, and are recaptured by the dopant atoms. Freeze-out results in transistor performance degradation including excess noise, current-voltage anomalies such as kinks and hysteresis, or even complete device failure.

For higher temperature operation, silicon-based electronics exist that are completely adequate for most read-out applications. However, silicon is not well suited to deep cryogenic operation. Moderately doped silicon freezes out above 40 K,[1] causing silicon bipolar transistors and JFETs to fail by that temperature. Conventional silicon MOSFETs, which use highly doped source and drain regions, can operate down to somewhat lower temperatures by inducing an inversion charge in the frozen out channel. Below about 20 K, however, the noise becomes excessive for many applications, and kinks and hysteresis often become apparent.

In addition, the sensitivity of silicon CMOS to radiation damage is increased at cryogenic temperatures, and high doses of radiation often occur in space-based applications. The radiation sensitivity increases because holes generated in the oxide by radiation are almost completely immobile, even at temperatures as high as 77 K, while electrons are rapidly removed from the oxide. Therefore, every one of the electron-hole pairs generated in the oxide by radiation results in permenently trapped positive charge. This is particularly a problem under the relatively thick field oxide, which can trap enough charge to invert the surface, and actually short circuit the transistors.

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Therefore, a transistor technology must be developed for deep cryogenic applications. One approach is to optimize silicon MOSFET readout electronics by carefully tailoring the doping, in order to reduce the noise and anomalies at deep cryogenic temperatures. This has been undertaken at TRW,[2] and is presently underway at other silicon foundries. Another approach is to develop readout electronics in a materials system which has already demonstrated good deep cryogenic performance, such as gallium arsenide junction field-effect transistors (GaAs JFETs).[3,4]

GaAs JFETs are well suited to deep cryogenic applications because of the very small electron effective mass in GaAs. This small mass results in the donor states being very shallow, that is, it requires a very small energy to liberate electrons from donor atoms in GaAs. Also, the small effective mass implies that the radius of the bound donor states are very large, and it requires a relatively low doping concentration before the mean distance between dopant atoms is smaller that the bound state radius. When this occurs, the semiconductor becomes degenerate, that is, the dopant atoms states merge with the free carrier bands, and the semiconductor becomes immune to freeze-out. In n-type GaAs, degeneracy occurs for doping concentrations of less than $1x10^{16}$ cm^{-3}, which is low enough to allow depletion at reasonable voltages. Holes in GaAs have a much larger effective mass, but by doping to concentrations above $5x10^{18}$ cm^{-3} p-type GaAs can still be made degenerate.[1] A GaAs JFET constructed using a heavily doped p-layer on top of a moderately doped n-layer is therefore immune to freeze out, and is expected to have good performance at deep cryogenic temperatures. In addition, since JFETs do not use a dielectric insulator, they are inherently less susceptible to radiation damage.

2. Fabrication of Cryogenic GaAs JFETs

GaAs JFETs with the structure shown in Fig. 1 have been fabricated at the Jet Propulsion Laboratory MicroDevices Lab. Starting on a semi-insulating GaAs substrate, molecular beam epitaxy (MBE) is used to epitaxially grow an undoped spacer layer, a moderately doped n-type channel layer, and a degenerately doped p-type gate layer. A tri-layer gate metal of titanium, platinum, and gold is deposited and patterned by liftoff, using image reversal photolithography. The structure is then wet chemically etched using a $NH_4OH:H_2O_2:H_2O$ (25:1:6250) solution with the gate metal acting as a self aligned mask. This removes the p-type GaAs everywhere except directly under the gate metal. Devices are isolated by a mesa etch protected by photoresist, and using the same etchant as the gate etch. A tri-layer ohmic contact metalization consisting of nickel, germanium, and gold is deposited and patterned by liftoff. The structure is then sintered at 410 °C for 13 seconds to alloy the ohmic contacts. Lastly, an overlayer of gold is deposited on the ohmic contacts and gate metal, in order to facilitate wire bonding.

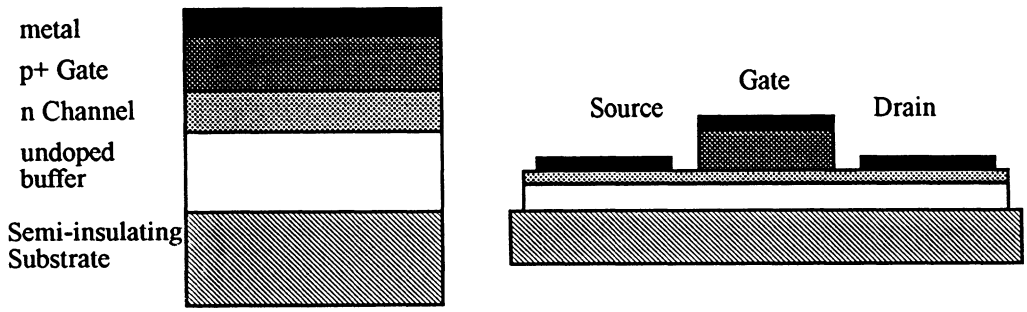

Fig. 1. The layer structure and the device structure of the GaAs JFETs.

Three different chips have been fabricated and are referred to as J3, J4, and J5, respectively. Each chip had different thicknesses and doping concentrations of the p and n layers, as listed in Table 1. All were grown by MBE. Chip J5 duplicated the layer structure previously used by Aerojet to fabricate GaAs JFETs that had good deep cryogenic performance.[4] Chips J3 and J4 have higher and lower doping concentrations, respectively, in the n-type channel layer. The channel layer thickness was chosen to make each device pinch off at approximately 5 V.

On each chip, several devices of different geometries were made. These included a set of ring JFETs in which a ring gate separates the central circular source from the surrounding drain. JFETs were made with gate ring diameters of 200 μm and 400 μm, with a corresponding circumference of approximately 625 and 1250 μm, respectively. The JFET length, that is, the thickness of the gate ring, varied from 5 to 50 μm.

Chip	N-type Channel Layer		P-type Gate Layer	
	Doping Concentration	Layer Thickness	Doping Concentration	Layer Thickness
	(cm^{-3})	(nm)	(cm^{-3})	(nm)
J3	$1x10^{16}$	850	$>5x10^{18}$	50
J4	$1x10^{17}$	265	$>5x10^{18}$	50
J5	$5x10^{16}$	375	$5x10^{18}$	500

Table 1: The layer structure of the JFET chips.

3. Measurements of GaAs JFETs at 4 K

The JFET chips were epoxied into 68-pin leadless chip carriers. The chip carriers were then mounted on the coldfinger of an evacuated LakeShore MTD-150 flow-through dewar, and were cooled to 4 K. The electrical properties of the JFETs at 4 K were measured using an HP4145B semiconductor parameter analyzer. The devices behave normally at 4 K. The transistor curve is shown in Fig. 2 for a typical device, the 20x1250 (length x circumference) ring JFET on chip J3.

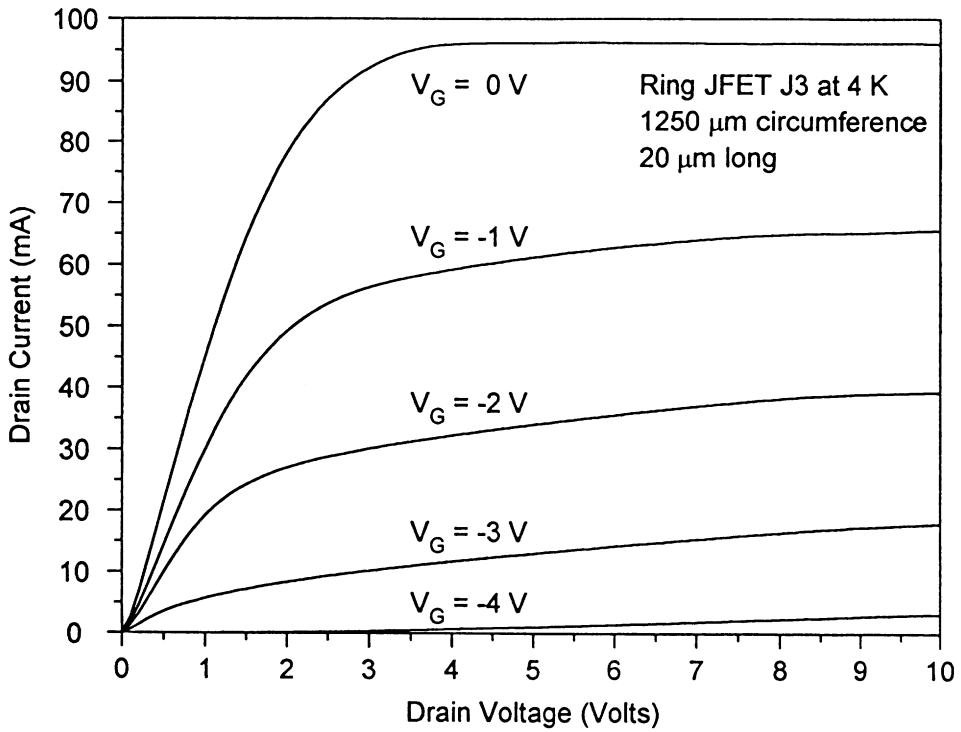

Fig. 2: The transistor curve at 4 K for a 20x1250 μm (length x circumference) ring JFET from chip J3.

The gate leakage current varies widely from transistor to transistor and from chip to chip, though in general, the gate current exhibits an exponential dependence on the gate voltage. There was no systematic dependence on the gate area or perimeter. All of the transistors on chip J4, which has the highest channel doping concentration, have very high gate leakage current. The gate leakage of the transistors on chip J5, however, are typically less than that of those on chip J3, even though chip J5 had a higher channel doping concentration. The exponential nature of the gate leakage current is characteristic of field emission. This is consistent with the fact that it increases for high doping concentrations. The large variation and lack of a systematic geometry dependence suggests that the current is highly process dependent. The gate leakage currents are compared in Fig. 3 for the 20x1250 (length x circumference) ring JFET on each chip. The plot cuts off at 1 pA, which is the sensitivity limit of the HP4145B used for the measurement.

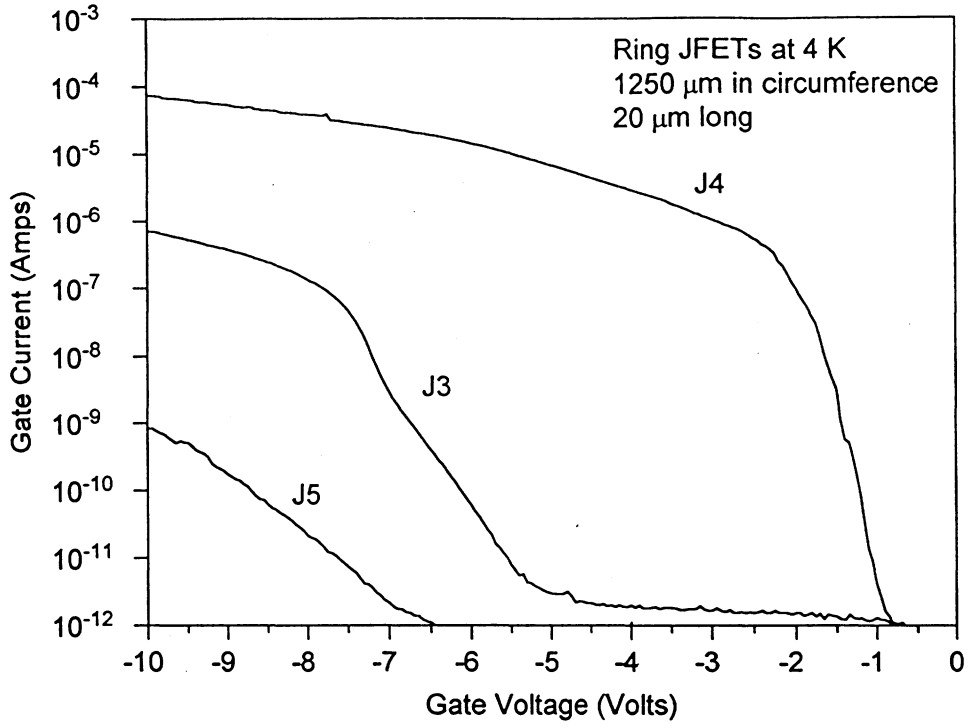

Fig. 3: The gate leakage current as a function of gate voltage at 4 K for 20x1250 μm (length x circumference) JFETs on chips J3, J4, and J5.

Since readout electronics applications require low power dissipation, typically limited to the order of 1 μW per channel, the transistors must operate at low bias currents, in or near the subthreshold region. A plot of the subthreshold current as a function of gate voltage for the 20x1250 (length x circumference) ring JFET on each chip is shown in Fig. 4. Curves are shown for drain voltages of 0.6 V and 1.0 V. The high gate leakage of the transistor on chip J4, which had the highest n-channel doping, dominates the transistors behavior before it even reaches the subthreshold region. The transistors on chips J3 and J5 exhibit good subthreshold behavior, however, with a subthreshold current slope of approximately 60 mV/decade and 160 mV/decade, respectively. The current transistor on chip J5 shows a much large dependence on the drain voltage than that for the transistor on chip J3. The reason for this is unknown, but it is of concern, since it lowers the output impedance of the device.

4. The input-referred noise voltage at 4 K

The noise of the transistors was measured using the circuit shown in Fig. 5. The circuit uses a EG&G model 113 differential pre-amplifier in a feedback circuit. The amplifier gain was set at 100, and the frequency response was set from d.c. to 3 kHz (at the 3 dB point). The voltage applied on the 1 MΩ resistor sets the current through the resistor, as the other end is a virtual ground. The amplifier adjusts the gate voltage in order to keep the source current equal to the resistor current. When any fluctuation occurs in the source current due to noise, the amplifier adjusts gate voltage to compensate. The output of the amplifier then is identically the input-referred noise.

The input-referred noise for the 20x1250 (length x circumference) ring JFETs on chip J3, J4, and J5 are shown in Fig. 6. The spike at 60 Hz is due to pickup of power line noise; the spike at 80 Hz is due to an intentionally injected calibration signal. The noise for the JFET on chip J5 is just above 1 $\mu V/\sqrt{Hz}$ at 1 Hz, and is approximately a factor of 2 higher for the JFET on chip J3. Both follow a $1/\sqrt{f}$ dependence reasonably well. The noise for the JFET on chip J4 has a noise voltage almost two orders of magnitude greater. It is not known if the high noise level is correlated with the high level of gate leakage current in this device. None of the transistors exhibited a systematic dependence on the bias current. The transistors on chips J3 and J5 did

not show any systematic size dependence. The transistors on J4, which had higher noise that those on the other chips did show a noise that approximately scaled with the inverse of the area.

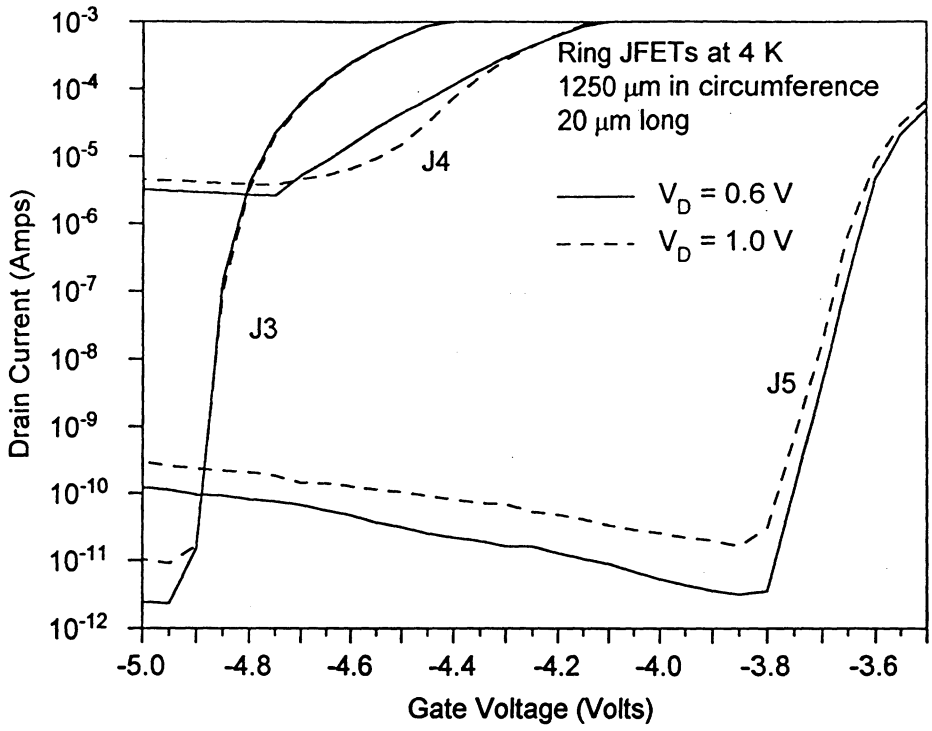

Fig. 4: The subthreshold drain current as a function of gate voltage at 4 K for for 20x1250 μm (length x circumference) JFETs on chips J3, J4, and J5.

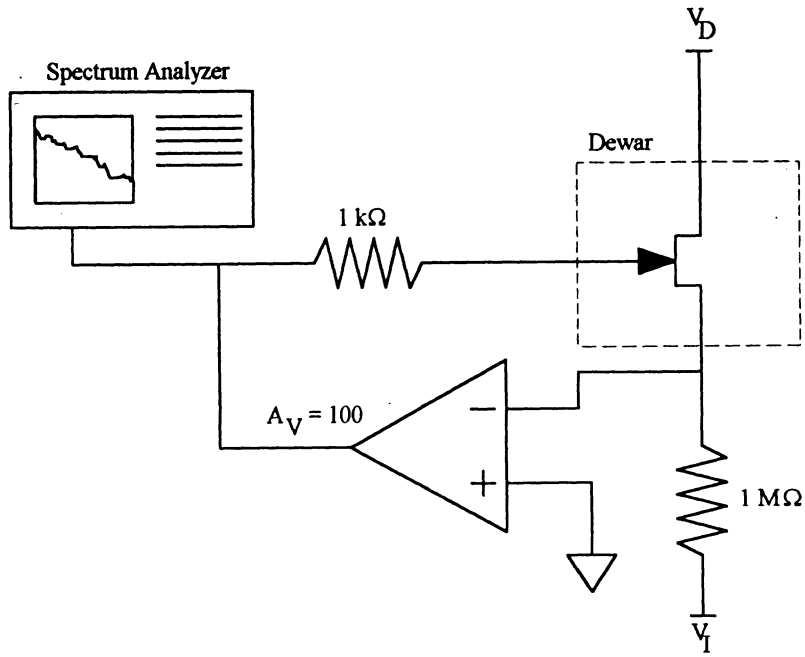

Fig. 5: The circuit used for measuring the input-referred noise.

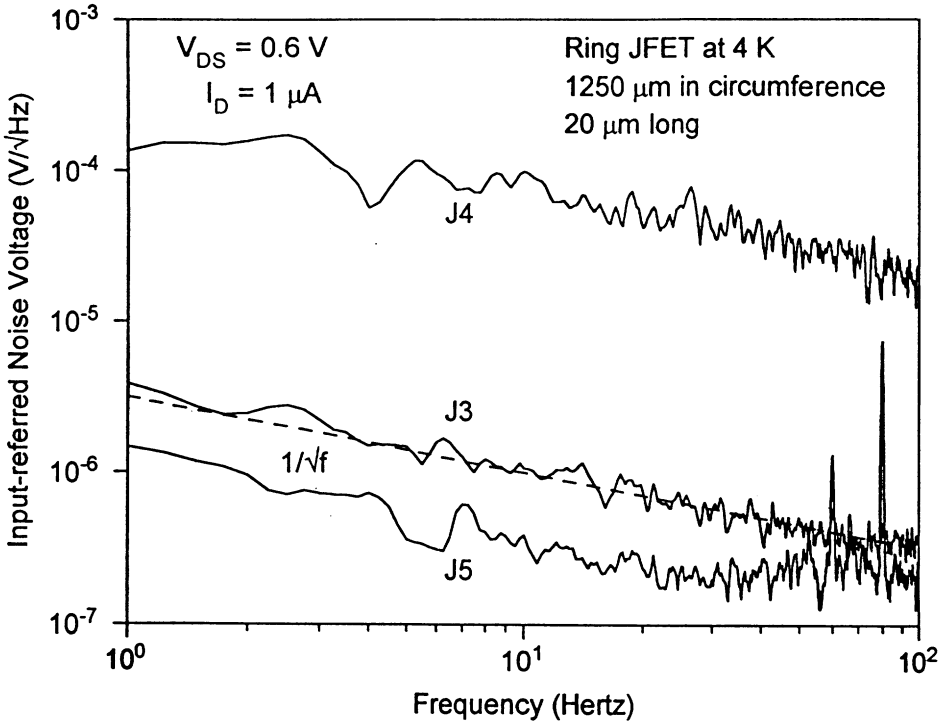

Fig. 6: The input-referred noise voltage as a function of frequency at 4 K for 20x1250 μm (length x circumference) JFETs on chips J3, J4, and J5.

5. Future Research

The noise of the best transistor of this series of chips is approximately 1 $\mu V/\sqrt{Hz}$ at 1 Hz. There is a wide variation in the noise between different types of GaAs JFETs, but the best exhibit input-referred noise as low as 10 $nV/\sqrt{Hz}$ at 1 Hz.[3,4] By proper tailoring of the device geometry, structure, and processing it should be possible to at least duplicate these results.

It is also desirable to reduce the gate current, which can be approached in several ways. First, the JFET can be redesigned so that the pinch off voltage is less, which lowers the typical operating voltage and electric field. Second, the doping concentration and position can be tailored so as to reduce the peak electric field. Third, the large transistor to transistor variation suggests that it is process dependent, and is probably very sensitive to the exact nature of the gate edge region. Changes in the processes, such as the gate etching method, will likely have a strong effect on the gate leakage. The design and fabrication of JFETs for improved performance is underway.

Further study of the geometry and doping dependence of the noise will be done. Several open issuses, such as the dependence of the noise on the gate leakage current, and the low output impedance of the devices on chip J5, will also be examined. A fundamental physical study of the noise processes in GaAs JFETs is also planned. To this point, most studies have been phenomenological.

In parallel with the improvement of discrete JFETs, the development of simple amplifier/multiplexer circuits is also underway. These will initially be simple 1x32 linear arrays of switched source followers. Later, more complex circuits such as capacitive trans-impedence amplifiers (CTIAs) will be designed and fabricated.

6. Summary

GaAs JFETs have been fabricated that operate normally at 4 K, and demonstrate good performance. For a good transistor, the noise is on the order of 1 $\mu V/\sqrt{Hz}$ at 1 Hz, which is just within the limit of the requirement for typical VLWIR imaging array readout applications. The gate leakage is approximately 1 pA at a gate voltage of -6V, and increases exponetially at approximately 1 decade per volt. The extrapolated gate current for typical operating currents in readout circuits is on the order of 10^{-15} A. VLWIR applications typically require input currents on the order of 10^{-17} A. The fabrication of GaAs JFETs designed for a lower pinch off voltage, and lower gate leakage current, as well as a study of the noise and the design of GaAs JFET-based readout circuits, are underway.

7. Acknowledgment

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