Computational Image Sensors for On-Sensor-Compression

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Abstract

In this paper, we propose novel image sensors which compress image signal. By making use of very fast analog processing on the imager plane, the compression sensor can significantly reduce the amount of pixel data output from the sensor. The proposed sensor is intended to overcome the communication bottle neck for high pixel rate imaging such as high frame rate imaging and high resolution imaging.

The compression sensor consists of three parts; transducer, memory and processor. Two architectures for on-sensor-compression are discussed in this paper that are pixel parallel architecture and column parallel architecture. In the former architecture, the three parts are put together in each pixel, and processing is pixel parallel. In the latter architecture, transducer, processor and memory areas are separated, and processing is column parallel.

We also describe a prototype chip of pixel-parallel-type sensor with 32 × 32 pixels which has been fabricated using 2 μm CMOS technology. Some results of examinations are shown in this paper.

1: Introduction

In order to read out image signal which is inherently two dimensional, usually, image signal is firstly scanned into one dimensional signal and read out. When the pixel rate gets higher, it becomes more difficult for conventional image sensors to read out signals. The bandwidth to transfer data from sensor in the scan-and-read-out process is a fundamental limitation for very high pixel rate imaging such as very high frame rate imaging or very high resolution imaging.

Image acquisition is also critical for real-time image processing. Real-time image processing system proceeds in three steps; transducing, read-out and processing. The high bandwidth required to transfer data from the sensor to the processor is also a fundamental disadvantage of the paradigm because it leads to high latency when pixel rate gets higher. In addition to the disadvantage, the paradigm demands expensive, large computation units in order to perform real-time application.

Tightly combining image acquisition and signal processing is an approach to overcoming the above communication bottle necks. We have been investigating novel image sensors on which video signal is compressed using conditional replenishment algorithm [1]. This on-sensor-compression significantly reduces the image data output from the sensor. Thus, on-sensor-compression especially benefits high pixel rate cameras and processing systems. The proposed sensors mainly consists of transducer, memory and processor. In this paper, we discuss two architectures for on-sensor-compression. They are pixel parallel and column parallel architecture.

The pixel-parallel-type sensor has transducer, memory and processor together in each pixel; processing in pixels is parallel so that processing of the sensor is very fast because it makes use of the two dimensional nature of image signal. However , its fill factor has to be small by current implementation technology, and the sensitivity of the sensor is not enough. On the other hand, the column-parallel-type sensor has the transducer area, the memory area, the processor area separately. The fill factor of the sensor is substantially improved because of the separate architecture, the power consumption is reduced. A prototype chip of pixel-parallel-type compression sensor has been designed and fabricated using $2 \mu m$ CMOS process. Some results of the tests are shown in this paper.

Related works in terms of integration of signal pro-

cessing and sensing are found in those areas of machine vision applications and neural network researches [2][3][4][5]. By integrating processing and sensing, the parallel nature of the image signal can be exploited and the processing gets remarkably faster. In those works, for example, a silicon retina that is a device which computes spatial derivatives of an image and an analog network that calculates optical flow have been developed. Most of those works are focused on how to execute early-vision processing in analog processing.

As for imaging devices, CCDs have been dominating. However, different from CCDs, CMOS-based sensors have been investigated. Recent CMOS based sensors have several amplifier transistors in each pixel. One of those CMOS sensor has a differential operation mode, that is, it outputs pixel values when the difference between adjacent frames are large[6].

Our proposed sensor is also CMOS-based. One of the essential differences between our sensor and the CMOS sensor[6] is that our proposed sensor has a frame buffer in each pixel. Thus, it can compress current image by using the last reproduction stored in the buffer. On the other hand, the CMOS sensor[6] does not have a frame buffer in each pixel, so it can not detect changes if the difference between adjacent frames is not large enough, and the detection errors can be accumulated.

Compared to the conventional digital compression, on-sensor-compression reduces the pixel rate output from the sensor, while the digital compression methods does not. Processing of on-sensor-compression is very fast by making use of parallel nature of image signal.

2: On-Sensor-Compression by Using Conditional Replenishment

2.1: Conditional Replenishment

Conditional replenishment [7] is employed for the video compression algorithm on a imager. Conditional replenishment is based on detection and coding of the moving areas so that it makes use of temporal redundancy to compress image signals.

As shown in Fig.1, current pixel value is compared to that in the last replenished frame which is stored in the memory. The values and addresses of that pixels are output when the magnitudes of the differences are greater than a threshold which is fixed or controlled by feedback of the number of flag signals.

Fig.2 shows the example of the detected moving pixels. The resolution of the image is 256 × 240 pixels and compression ratio is 10:1 and 5:1 for threshold 20 and 5 respectively. Although conditional replenishment is rather simple, it can achieve about 10:1 compression
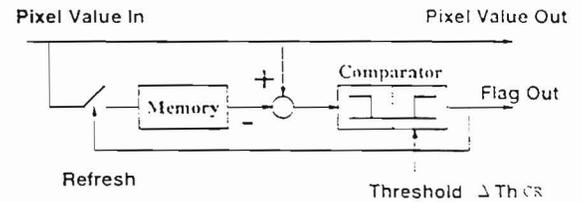
Figure 1. Description of coding algorithm in each pixel by conditional replenishment
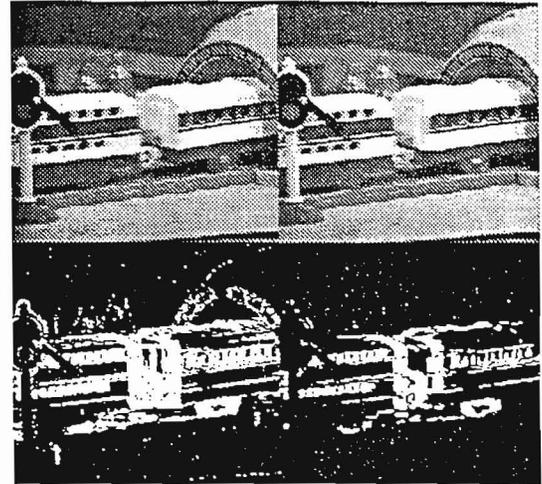
Figure 2. Detection of moving pixels top: two frames of an image sequence (256 levels), bottom: pixels detected as moving (left: threshold 5 compression ratio 5:1, right: threshold 20 compression ratio 10:1)

ratio without significant degradation under the ordinary circumstance.

2.2: Pixel Rate Control

The threshold for rate control is fixed (VPR) or controlled by the number of flag signals (CPR). In case of a fixed threshold, the SNR of the reconstructed image is kept about some value, but the number of activated pixels significantly changes when the scene is changed. The transition of pixel rate is examined by computer simulation using the image sequence which is composed of three different monochrome sequences: Train, Miss. America and Rabbit. Fig.3 shows the experimental result when the threshold are 30 and 6, respectively.
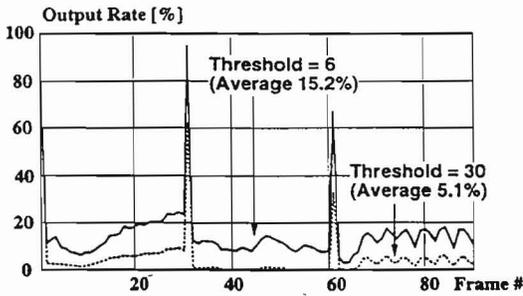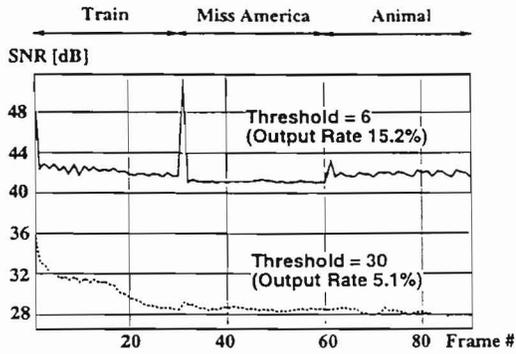
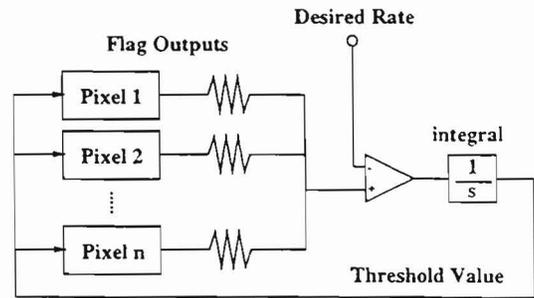Figure 3. Coding performances under fixed threshold control

Figure 4. Diagram of rate-control
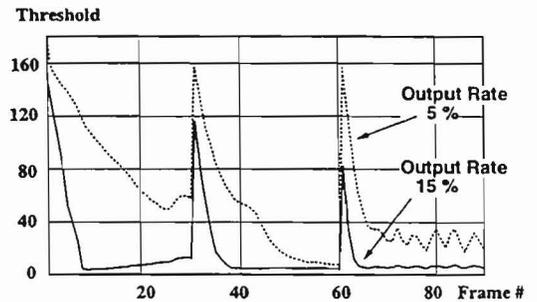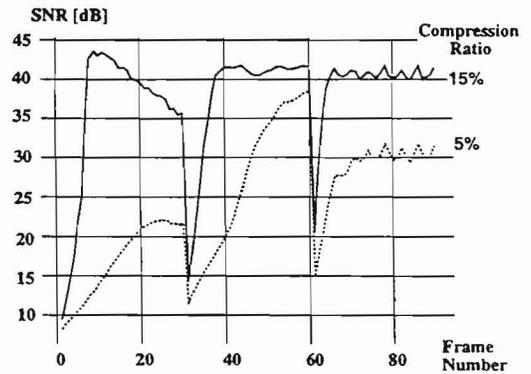
Figure 5. Coding performances under the CPR control

The coding rate can be controlled using analog processing circuit. Since the very fast processing is available on the imager plane, rate control can be fully finished in a single frame. As shown in Fig.4, the number of the detected pixels as moving is computed by totaling the activated flag signals using a resistive network. In order to control pixel rate, the threshold is adaptively changed until the number of detected pixels is less than desired rate. Fig.5 shows the experimental result when the ratio of the activated pixels are 15% and 5%. Experiments show degradation of SNR when the scene is changed. However, quality of the reconstructed image recovers in a few frames.

3: Architecture of On-Sensor-Compression

The proposed compression sensor using conditional replenishment consists of transducer, memory and processing elements and there are various ways to implement three elements on image sensor. In this paper, we discuss two architectures of on-sensor-compression shown in Fig.6.

(a) Pixel parallel architecture   (b) Column parallel architecture

Figure 6. Description of the architecture for on-sensor-compression

In pixel parallel architecture, each pixel has three elements so that it is able to make full use of two dimensional nature of image signal. However, pixel parallel architecture is complex and it inherently has disadvantages of low fill factor and relatively high power dissipation.

Column-parallel architecture separates into three elements and processing is column parallel. Fill factor is much improved compared to the pixel-parallel architecture because photodiode is separated in this column parallel architecture. Power dissipation is reduced because processing element is assigned to each column. But, column-parallel-type sensor makes sacrifice of processing speed.

4: Pixel-Parallel-Architecture

The analog processing circuit for each pixel is designed for a prototype of the pixel-parallel-type sensor. Fig.7 shows the circuit designed for a pixel. The pixel unit cell consists of a photodiode(PD), a sample & hold circuit, two differential amplifiers and a flag generation circuit.

Firstly, the input pixel value is sampled and held in the capacitance $C1$ when Vsmp is on. Then the magnitude of the difference is calculated by the two differential amplifiers between the current pixel value in $C1$ and the last replenished value held in the capacitance $C2$ (memory). The difference is immediately

compared to the threshold (V_{th}). The pixel is detected as moving if the difference is larger than the threshold, then this pixel value is held in the capacitance $C2$.

Fig.8 shows the entire prototype sensor architecture. Using horizontal and vertical shift registers, the pixels are scanned line by line. The vertical shift register selects the line in order. Only the activated pixels are selectively read out and non-activated pixels are skipped without reading by the horizontal shift register shown in Fig.9, which is controlled by the flag signals. The horizontal shift register also outputs the addressing information.

4.1: Prototype Chip of Pixel-Parallel-Type Sensor

A prototype chip of the on-sensor-compression has been fabricated using $2\mu m$ CMOS process. Fig.10 shows the prototype sensor. The chip has 32×32 pixels with $170\mu m \times 170\mu m$ pixel size. The total size of the chip is approximately $7.3mm \times 6.8mm$. In this first prototype, the address encoder and A/D converter are not implemented.

Fig.11 shows an image output from the sensor, when all of the pixel values are forced to be read out. Although sensitivity variation was clearly observed, the chip was successfully operated.

A test circuit of a single pixel unit cell has been also fabricated to examine its behavior. Fig.12 shows one of the results when using a LED driven by a sinusoidal wave as a light source. The sampling rate is set to 1kHz. As shown in Fig.12, the flag signal is activated and the pixel circuit correctly works.

Fig.13 shows the transfer characteristic of the comparator circuit. When the differential value ranges from -0.5V to +0.5V, the circuit calculates the absolute value with enough precision.

5: Column-Parallel-Architecture

Fig.14 shows an analog circuit of the column-parallel-type sensor. Each pixel has only a transducer and a separate corresponding memory. The processing element is for each column. The processing elements consists of three differential amplifiers and a flag generation circuit.

Firstly, when V_{row} is on, the magnitude of the difference is calculated by the two central differential amplifiers between the current pixel value and the last replenished value held in the capacitance C_m. The difference is immediately compared to the threshold (V_{th}). The pixel is detected as moving if the difference is larger than the threshold, then the flag signal is

Table 1. Comparison between pixel-parallel and column-parallel-type sensor

	pixel-parallel	column-parallel
Number of transistors	25 / pixel	transducer : 3 / pixel
		memory : 4 / pixel
		processing : 35 / column
Fill factor	about 1.4 %	under designing layout
Power dissipation	1.4mW / pixel	0.2mW / column
	(Vdd = 7V)	(Vdd = 5V)
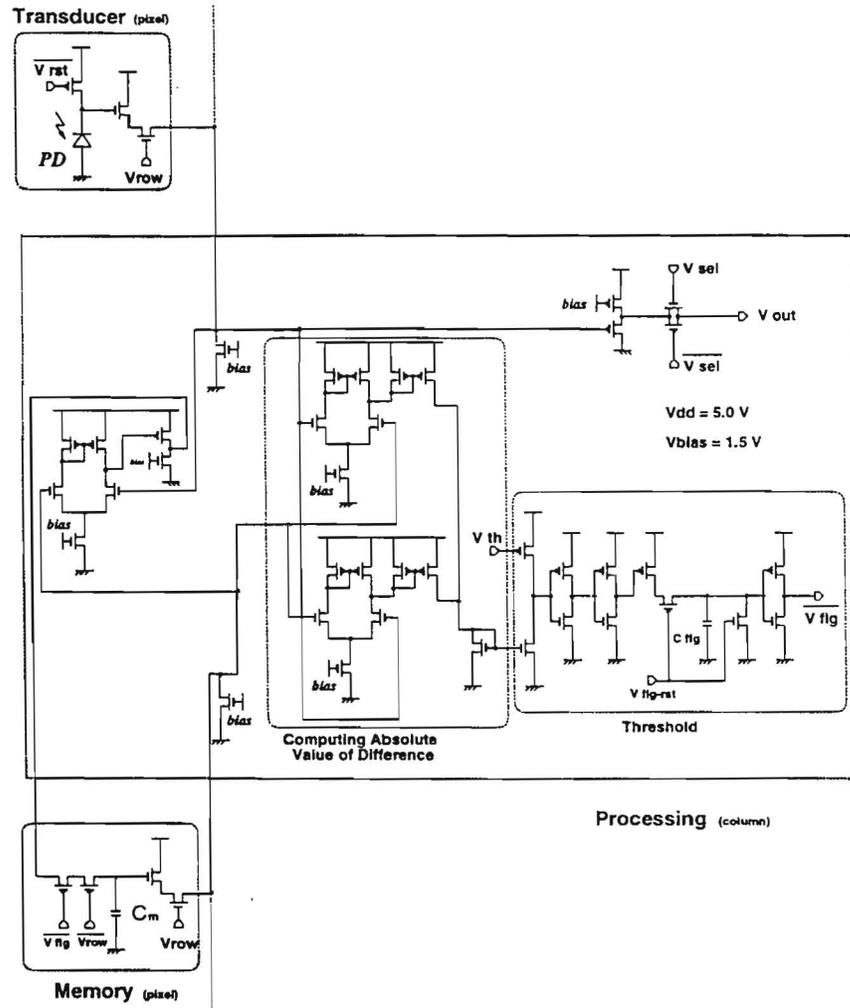
Figure 14. An analog circuit of a pixel for column-parallel-architecture

Flag

Output of Photo Diode
after S & H (0.2V/DIV)

Current of LED
(10mA/DIV)

5ms/DIV
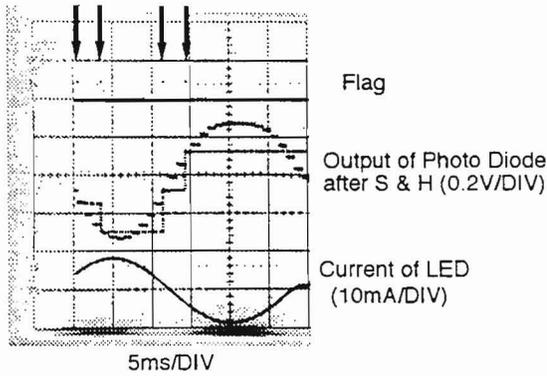
Figure 12. Behavior of the VLSI of a single pixel. Bottom: LED driving current, Middle: Sampled output of photo diode, Top: Activated flag signal (arrows are written to point the activated flags. Sampling rate (integration time) is 1ms. The dotted line in the middle is an estimated reconstruction in the replenished memory.
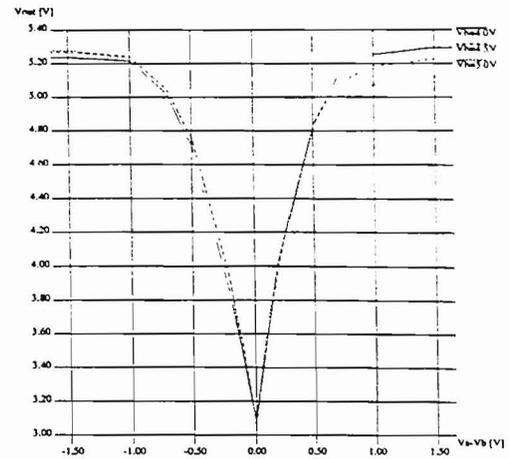

Figure 13. Transfer characteristics of the circuit for calculating absolute value

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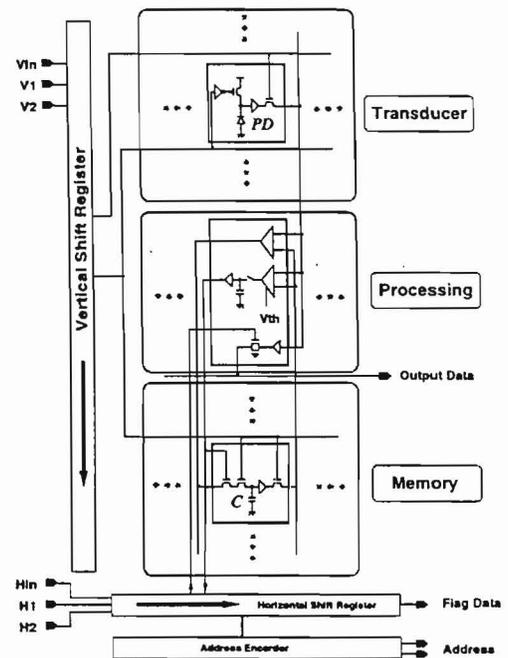
Figure 15. Block diagram of column-parallel-type sensor