CMOS Active Pixel Sensor with On-Chip Successive Approximation Analog-To-Digital Converter

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***Abstract*—The first CMOS active pixel sensor (APS) with on-chip column-parallel successive-approximation analog-to-digital converter (ADC) is reported. A 64×64 element CMOS APS implemented in a 1.2-μm n-well single-poly, double-metal process with 24-μm pixel pitch is integrated with a 64×1 array of column parallel successive approximation 8-b ADC's. Good image quality was observed. The capacitively-coupled ADC's dissipate approximately 1 μW-s/ksample and occupy 0.05 mm^2 of chip area.**

I. Introduction

RECENTLY, CMOS active pixel sensors (APS) have shown promise for use in the implementation of a camera-on-a-chip [1]. An analog output camera-on-a-chip with on-chip timing and control with low noise and high dynamic range was recently reported [2]. To implement a camera on-a-chip with a full digital interface requires an on-chip analog-to-digital converter (ADC). There are many considerations for on-chip ADC. The ADC must support video rate data that ranges from 0.92 Msamples/s for a 320×288 format sensor operating at 10 frames/s for videoconferencing, to 55.3 Msamples/s for a 1280×720 format sensor operating at 60 frames/s. The ADC must have at least 8-b resolution with low integral nonlinearity (INL) and differential nonlinearity (DNL) so as not to introduce distortion or artifacts into the image. The ADC can dissipate only minimal power, typically under 100 mW, to avoid introduction of hot spots with excess dark current generation. The ADC cannot consume too much chip area or it will void the economic advantage to on-chip integration. The ADC cannot introduce noise into the analog imaging portion of the sensor through substrate coupling or other crosstalk mechanisms that would deteriorate image quality.

CMOS image sensors with on-chip single-slope ADC have been reported previously [3], [4] and related work on on-chip ADC's for infrared focal-plane array readout has also been reported [5]–[7]. There are several approaches for implementation of on-chip ADC [8], [9]. The ADC can be implemented as a single serial ADC (or several ADC's, e.g., one per color) that operate at near video rates [10 Msamples/s]. The ADC can also be implemented in-pixel [10], [11] and operate at frame rates [e.g., 30 samples/s]. We have been pursuing column-parallel ADC's where each (or almost each) column in the pixel array has its own ADC so that each ADC operates at the row rate [e.g., 15 ksamples/s]. In this architecture, single-slope ADC's work well for slow-scan applications but dissipate too much power for video-rates. Oversampled ADC's require significant chip area when implemented in column-parallel formats [12]. A successive approximation ADC has a good compromise of power, bit resolution, and chip area.

In this paper, a capacitively-coupled, column-parallel, successive-approximation ADC architecture is explored for use with a CMOS APS. This is the first report of such an ADC integrated with an image sensor.

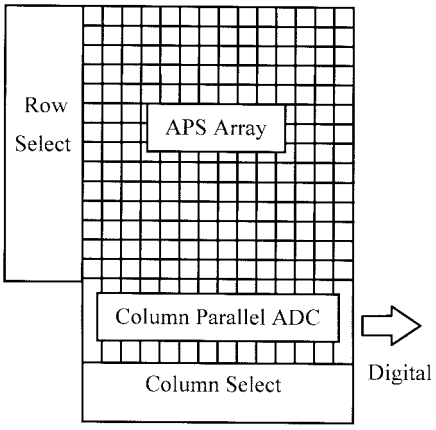

Fig. 1. Architecture of CMOS APS with on-chip column-parallel ADC.

II. Sensor Design

A block diagram of the sensor is shown in Fig. 1. The imaging portion of the sensor is a 64×64 element array of photogate-type CMOS active pixels. To the side of the array is the row decoder that selects rows and applies the readout control signals to the pixel. The photogate pixel and its readout sequence have been well reported previously [13]. The pixel delivers two sequential voltages to the vertical column bus—a reset reference level followed by the pixel photosignal.

At the bottom of the imaging array is the 64×1 array of ADC's that are described in greater detail below. The ADC's convert the difference between the reference level and photosignal level into an 8-b digital word. The digital words representing a row of pixel data are stored as an array of 64 8-b registers. A column-select decoder is used to address a particular register for readout. When selected, the eight bits

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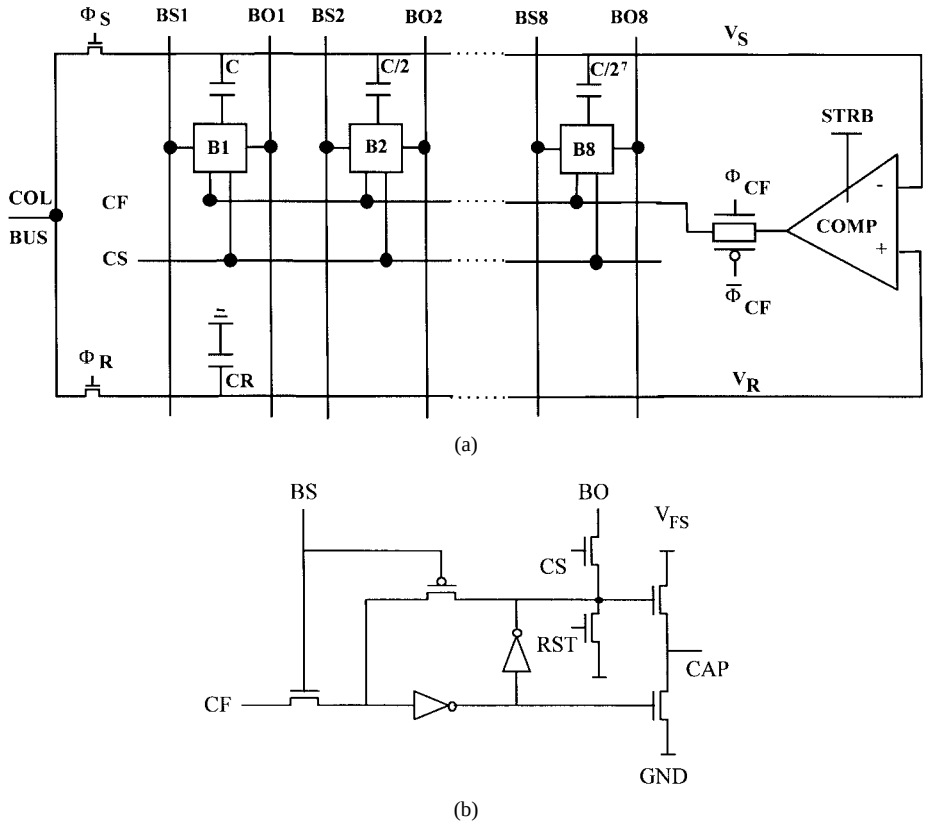


Fig. 2. Schematic of (a) successive approximation ADC with (b) detail of in-cell logic.

from the register are read out in parallel. After readout, the next row in the imaging array can be selected for readout. Rows need not be selected sequentially, nor do all rows need to be readout. The same applies to the readout of columns.

A. ADC Design

As was discussed above, there are many constraints on the implementation of the on-chip ADC. In this work, a column-parallel successive approximation ADC architecture was chosen. The ADC must be quite narrow in width, but can extend for several millimeters in the vertical direction. A capacitively-coupled approach similar to a charge redistribution ADC [14]. was used. The ADC requires only capacitors, switches, and a comparator and does not require an op-amp. The comparator consumes power only when strobed so that the overall power dissipation of the ADC can be quite low. A schematic diagram of the ADC is shown in Fig. 2(a) and (b). Within each ADC there is minimal logic to control the capacitor switching. Internal to the ADC, comparator flag (CF) is used to set the bit latch B_N. Additional global logic located outside the region of the ADC is required for sequencing the ADC's and for digital readout including generation of sample pulses Φ_R and Φ_S, bit select (BS), comparator strobe (STRB), and column select (CS). In the prototype sensor, some of these signals were not generated on chip and were applied externally.

The ADC consists of an upper bank of capacitors and a lower capacitor (C_R). The lower plates of the upper bank are connected to a set of 8-b registers labeled $B1$ through $B8$. The other plates are connected together and feed the

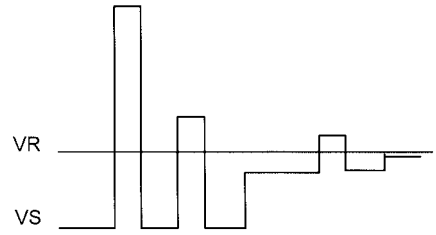


Fig. 3. Illustration of voltage convergence in successive approximation ADC.

negative comparator input. Each capacitor in the bank is sized in a geometric series, such that each succeeding capacitor is half as large as the preceding one. The lower capacitor C_R is referenced to ground and is also attached to the positive comparator input. The comparator output is a logic signal that is fed back to the latched switches in the capacitor bank.

Operation of the ADC proceeds as follows. All register bits are initially set to logic zero. This causes the lower plates of the capacitor bank to be set to ground. When the reset reference voltage is present on the column bus, switch Φ_R is used to sample the reference voltage onto the lower capacitor C_R. When the photosignal is present on the column bus, the switch Φ_S is used to sample the photosignal voltage onto the upper bank of capacitors. It is assumed that the photosignal voltage is lower than or equal to the reset reference voltage.

The successive approximation begins with register bit $B1$ set to a logic one. This causes $V_{\rm ref}$ to be applied to the bottom plate of the first (largest) capacitor. The voltage on the upper plate rises to a value of $V_s + V_{\rm ref}/2$. The comparator

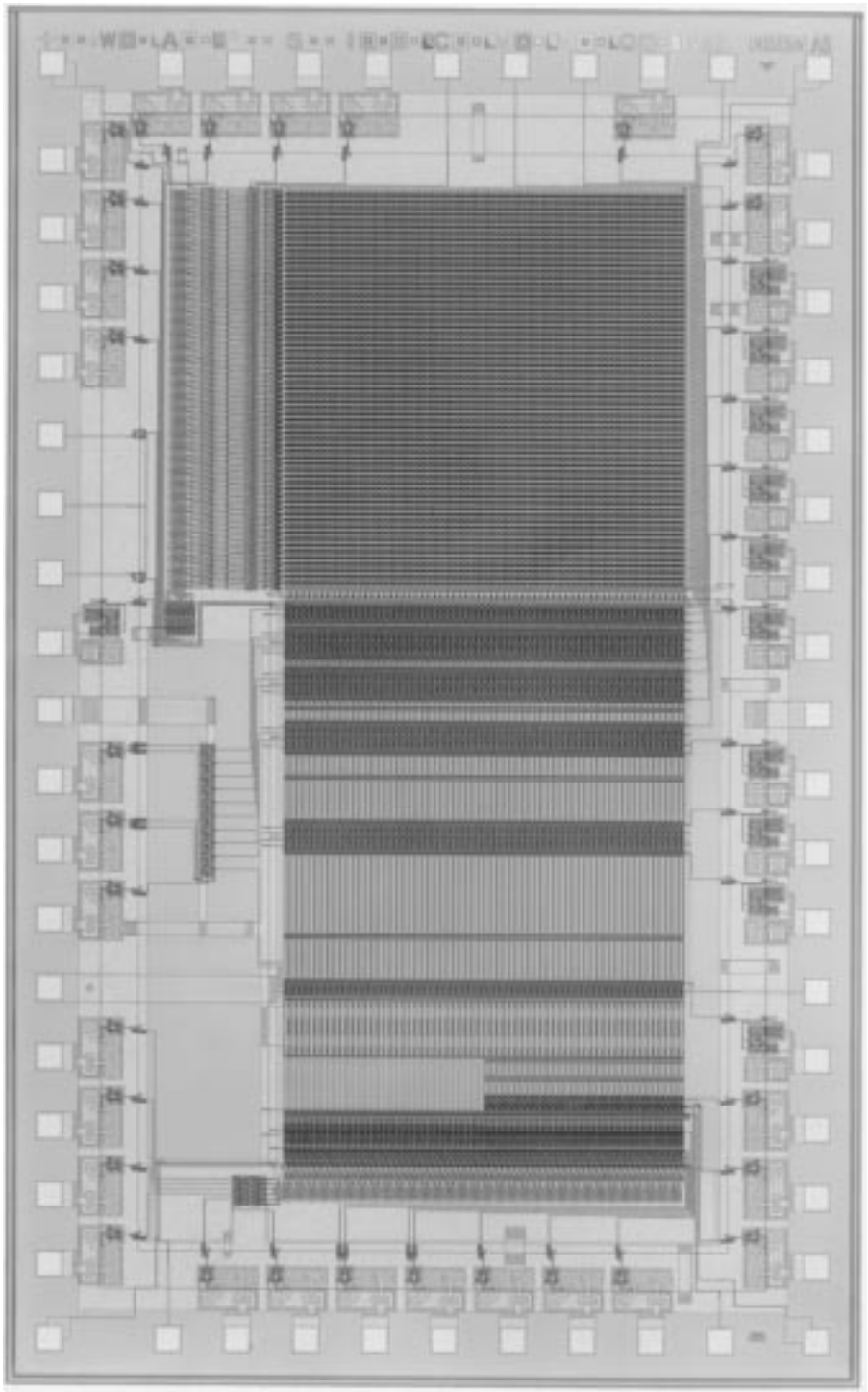


Fig. 4. Photograph of 64×64 element CMOS APS with on-chip column-parallel ADC.

is strobed comparing $V_s + V_{\rm ref}/2$ to V_r. If the result is true $(V_s + V_{\rm ref}/2 < V_r)$ then bit $B1$ is fixed at a value of logic one; otherwise bit $B1$ is returned to logic zero.

For the next approximation, register bit $B2$ is set to a logic one. The voltage on the upper plate rises to a value of $V_s + B1{\cdot}V_{\rm ref}/2 + V_{\rm ref}/4$. The comparator is strobed and if the result is true, bit $B2$ is fixed at logic one; otherwise, it returns to logic zero.

The process continues for as many bits as desired up to the number of capacitors. The voltage on the upper plate as a function of time is shown in Fig. 3 as each successive bit is tested in the logic one state, and then conditionally returned to logic zero, depending on the comparator outcome. As time progresses, the voltage on the upper plate becomes successively closer to V_r. After all eight bits have been activated, the ADC algorithm is complete and the register bits are ready for readout.

There are several design considerations for the ADC. Inaccuracy in capacitor sizing will cause DNL errors. Inaccuracy is greatest for the smallest value capacitors but inaccuracy

Fig. 5. Raw digital image of George Washington obtained from half the sensor.

in the larger capacitors causes the most DNL. Comparator input offset will result in fixed pattern noise between columns. Substrate coupling into the capacitors will results in temporal noise in the ADC output. Careful attention to layout is required to minimize these deleterious effects.

III. Experimental Results

The prototype sensor was implemented in the HP 1.2-μm n-well single-poly, double metal process with the linear capacitor option. The photogate pixels were sized at 24×24 μm, with a designed fill factor of 29%. The conversion gain of identical pixels measured in other analog-output sensors was found to be 8 μV/e$^-$ [15]. (It is difficult to assess conversion gain in digital sensors with 8-b resolution and referenced to the saturation voltage because the temporal noise is typically less one LSB using conventional techniques. Separate pixel test structures are required.)

The column parallel ADC's were laid out in a 24-μm pitch and were 2.1 mm in length (0.05 mm^2). The minimum capacitor size was 5 fF. The capacitor bank was implemented using the linear capacitor option easing constraints on operating voltage range. The 64 ADC bank was divided into two banks of 32 ADC's each. The first bank contained the ADC described above. The second included a modification to improve fixed pattern noise. However, this second bank performed poorly and is not reported here. The ADC bank occupies approximately 58% of the core area of the chip. The sensor is shown in Fig. 4.

The sensors were operated using a 5 V supply. Power dissipation in the ADC was estimated to be 50 μW when operating up to a 50 ksamples/s continuous conversion rate. This power is nearly all due to the biasing of the comparators each at 20 μA and 5 V (50% duty cycle). The time to readout a row consists of the pixel sampling time (16 clock cycles), the A/D conversion time (48 clock cycles), and the digital readout time for the 32 columns (32×6 clock cycles). Thus, the required ADC rate is typically much higher than the row rate, and in this case only 23% of the row readout time is available for ADC. For 24 frames/s readout, the row rate is 1536 Hz, and the required ADC time is 150 μs. The average ADC power dissipation can be reduced by only applying current bias during conversion interval. Thus, the total power dissipation for all the ADC's can be calculated as $20\ \mu\text{A} \times 5\ \text{V} \times 0.23 \times 32 = 736\ \mu\text{W}$.

Quantitative data was acquired by using a separate digital-to-analog converter (DAC) to convert the sensor's digital output back to analog format to make it compatible with the existing analog sensor data acquisition system. The nominal operating readout rate was an average of 100 kpixels/s corresponding to 24 frames/s readout rate. Column-wise FPN with V_{ref} set at 1 V was less than 2 LSB's. Fig. 5 shows a raw image corresponding to a 32×64 element portion of the array (due to the problem described above) with V_{ref} set to 1 V. Good gray scale reproduction was observed in various images.

The sensor was operated up to a rate of 1000 frames/s corresponding to 4 Mpixels/s average output rate and 37 μs conversion time. Full 8-b resolution appeared to be maintained but quantitative sensor measurement was not performed. No crosstalk effects from the column-parallel ADC architecture were observed in the image though detailed quantitative measurements were not made. No anomalous dark current (global or local) was observed. Dark current in these pixels is typically 12–13 LSB counts/s (50 mV/s), output referred.

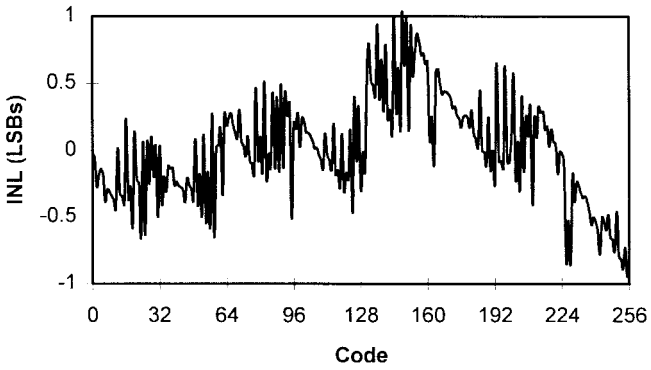
A separate ADC test circuit was quantitatively measured at 50 ksamples/s conversion rate. Fig. 6(a) and (b) shows the measured INL and DNL using a slowly varying input signal [16]. Both are below 1 LSB indicating the ADC's have both 8-b resolution and 8-b accuracy. Capacitor sizing inaccuracy is thought to be the dominant source of error and may be improved in the future.

IV. Discussion

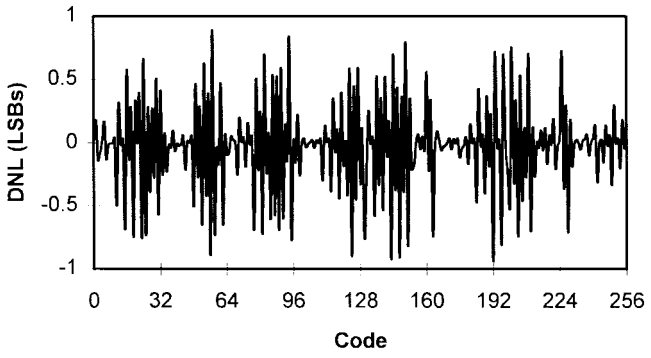
The capacitively-coupled ADC approach shows promise for incorporation in larger arrays operating at high frame rates. With an ADC energy/conversion figure of 1 μW-s/ksample and a small size of 0.05 mm^2, the circuit is one of the highest performance 8-b ADC's in this class. Residual FPN can be corrected with appropriate on-chip noise cancellation circuits. An extension in resolution to at least 10 bits is believed reasonable. After this work was performed, the ADC has been incorporated with modification in a several higher resolution digital camera-on-a-chips. Performance has been satisfactory and will be reported elsewhere [17], [18].

V. Conclusion

A prototype CMOS active pixel sensor with on-chip column-parallel successive approximation 8-b ADC has been



(a)



(b)

Fig. 6. (a) Integral nonlinearity and (b) differential nonlinearity of ADC operating at 50 ksamples/s as a function of output digital code in LSB's.

demonstrated for the first time. Satisfactory image quality was obtained from the sensor with good gray scale reproduction and low power dissipation

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Bedabrata Pain (M'95), for a photograph and biography, see this issue, p. 1757.

Eric R. Fossum (S'80–M'84–SM'91), for a photograph and biography, see this issue, p. 1698.