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CMOS active pixel image sensors[1]

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Abstract

CMOS active pixel sensors (APS) have performance competitive with CCD technology and offer advantages in on-chip functionality, system power reduction, cost and miniaturization. This paper briefly discusses recent advancements.

1. Introduction

Over the past five years, there has been a growing interest in CMOS image sensors. The major reason for this interest is customer demand for miniaturized, low-power, and cost-effective imaging systems. CMOS-based image sensors offer the potential opportunity to integrate a significant amount of VLSI electronics on-chip and reduce component and packaging costs. It is now straightforward to envision a single-chip camera that has integrated timing and control electronics, sensor array, signal processing electronics, analog-to-digital converter and full digital interface. Such a camera-on-a-chip will operate with standard logic supply voltages and consume power measured in the tens of milliwatts [1,2].

2. Historical background

The earliest MOS image sensors used a passive pixel structure [3] and the first MOS active pixel image sensor was described in 1968 [4]. The announcement of the CCD in 1970 shifted the emphasis of most image sensor R&D to CCDs. Significant advancement in CCD technology took place in the 1970s and the 1980s.

It is interesting to note that while CCDs predominated in visible imaging in the second-half of the 1980s, two related fields started to turn away from the use of CCDs. The first was hybrid infrared focal-plane arrays that initially used CCDs as a read-out multiplexer. Due to limitations of CCDs, particularly in low-temperature operation and charge handling, CMOS read-out multiplexers were developed that allowed both increased functionality as well as performance compared to CCD multiplexers [5]. A second field was high-energy physics particle/photon vertex detectors. Many workers in this area also initially used CCDs for detection and read out of charge generated by particles and photons. However, the radiation sensitivity of CCDs and the increased functionality offered by CMOS has led to subsequent abandonment of CCD technology for this application.

In the early 1990s, two independently motivated efforts led to a resurgence in CMOS visible image sensor development. The first effort was to create highly functional single-chip imaging systems where low cost, not performance, was the driving factor. The second independent effort grew from NASAs need for highly miniaturized, low-power, instrument imaging systems for next-generation deep space exploration spacecraft. Such imaging systems are driven by performance, not cost. The convergence of the efforts has led to significant advances in CMOS image sensors and the development of the CMOS active pixel sensor (APS). It has performance competitive with CCDs with respect to read noise, dynamic range and responsivity but with vastly increased functionality, substantially lower system power (10–50 mW), and the potential for lower system cost.

Contributing to the recent activity in CMOS image sensors is the steady, exponential improvement in CMOS technology. The rate of minimum feature size decrease has outpaced similar improvements in CCD technology (see Fig. 1). Furthermore, sensor pixel size is limited by both optical physics and optics cost, making moot the CCDs inherent pixel size advantage for most applications. Recent progress in on-chip signal processing (and

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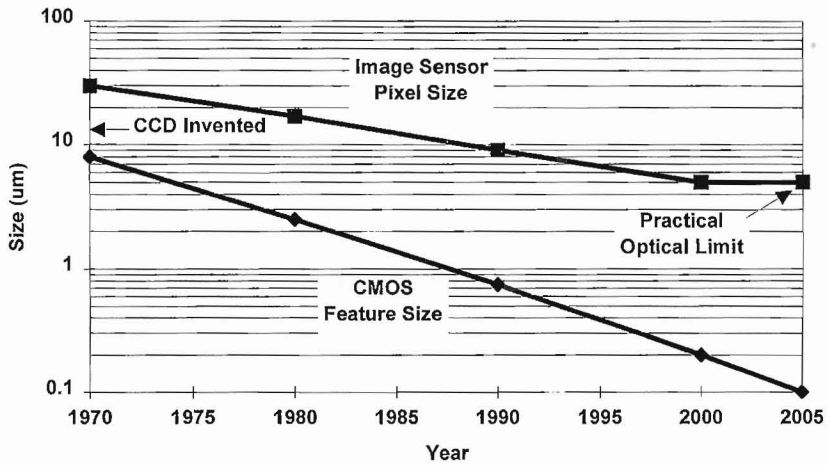

Fig. 1. The steadily increasing ratio between pixel size and minimum feature size permits the use of CMOS circuitry within each pixel.

off-chip DSP) has also reduced CMOS image sensor fixed pattern noise (FPN) to acceptable levels. In addition, the transition from analog imaging and display systems to digital cameras tethered to PCs permits digital FPN correction with negligible system impact.

3. Overall architecture

The overall architecture of a CMOS image sensor is shown in Fig. 2. The image sensor consists of an array of pixels that are typically selected a row at a time by row-select logic. This can be either a shift register or a decoder. The pixels are read out to vertical column busses that connect the selected row of pixels to a bank of analog signal processors (ASPs). These ASPs perform functions such as charge integration, gain, sample and hold, correlated-double-sampling and FPN suppression.

More advanced CMOS image sensors contain on-chip analog-to-digital converters (ADC). In Fig. 2, the ADCs are shown as column-parallel ADCs, i.e., each column of pixels has its own ADC. The digital output of the ADCs (or analog output of the ASPs) is selected for read out by column-select logic that can be either a shift register or decoder. A timing and control logic block is also integrated on-chip.

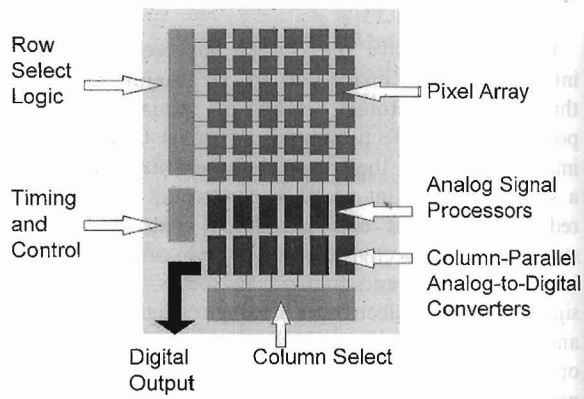

Fig. 2. CMOS APS integrates timing and control, ADC and other circuitry on the same chip.

4. Pixel circuits

The CMOS APS trades pixel fill factor for improved performance compared to passive pixels using the in-pixel amplifier. Pixels are typically designed for a fill factor of 20–30%, similar to interline-transfer (ILT) CCDs. Loss in optical signal is more than compensated by reduction in read noise for a net increase in the signal-to-noise ratio and the dynamic range. Microlenses are commonly employed with low-fill factor ILT CCDs [6,7] and can recover the lost optical signal. The simple, polyimide microlense refracts incident radiation from the circuitry region of the pixel to the detector region. The microlense can improve optical fill factor by 3-fold so that the net optical aperture for the detector is 60–80%.

A. Photodiode-type APS

The photodiode-type (PD) APS was described by Noble in 1968 [4] and has been under investigation by Andoh at NHK in Japan since the late 1980s [8–10] in collaboration with Olympus, and later, Mitsubishi Electric. A diagram of the PD-APS is shown in Fig. 3.

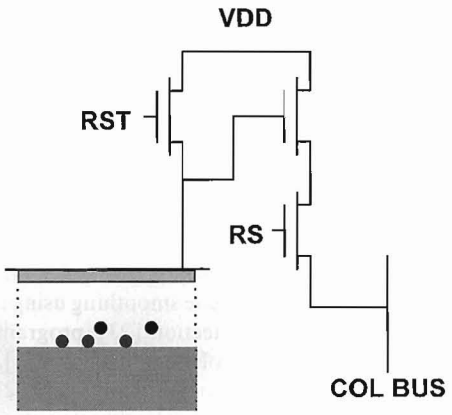

Fig. 3. A photodiode-type active pixel sensor (APS). The voltage on the photodiode is buffered by a source follower to the column bus, selected by RS-row select. The photodiode is reset by transistor RST.

A high-performance PD-APS was demonstrated by JPL in 1995 in a 128×128 element array that had on-chip timing, control, correlated double sampling and fixed-pattern noise suppression circuitry [11]. The chip achieved 72 dB dynamic range with FPN less than 0.15% saturation. A 640×480 PD-APS with $5.6\,\mu m \times 5.6\,\mu m$ pixels and on-chip color filter arrays and microlenses was described by Toshiba in 1997 [12], and a 800×1000 element PD-APS was reported by VLSI Vision also in 1997 [13].

Photodiode-type APS pixels have high-quantum efficiency as there is no overlying polysilicon. The read noise is limited by the reset noise on the photodiode since correlated double sampling is not easily implementable without frame memory, and is thus typically 75–100 electrons rms. The photodiode-type APS uses three transistors per pixel and has a typical pixel pitch of $15 \times$ the minimum feature size (see Fig. 4). The photodiode APS is suitable for most mid-to-low-performance applications, and its performance improves for smaller pixel sizes since the reset noise scales as $C^{1/2}$, where C is the photodiode capacitance. A trade-off can be made in designed pixel fill-factor (photodiode area), dynamic range (full well) and conversion gain ($\mu V/e^-$). Lateral carrier collection permits high responsivity even for small fill-factor [14].

B. Photogate-type APS

The photogate APS was introduced by JPL in 1993 [15–17] for high-performance scientific imaging and low-light applications. The photogate APS combines CCD benefits and X–Y readout, and is shown schematically below in Fig. 5. Signal charge is integrated under a photogate. For read out, an output floating diffusion is

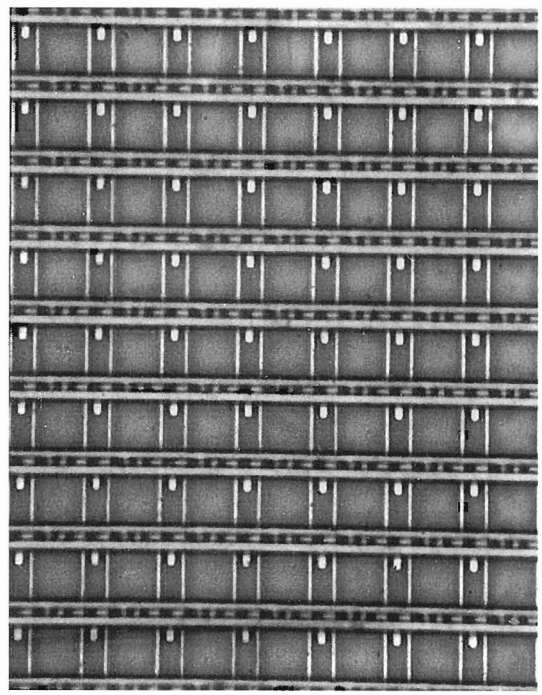

Fig. 4. Close-up of the $11.9\,\mu m$ pixel photodiode-type active pixels used in the 1024×1024 array shown in Fig. 8.

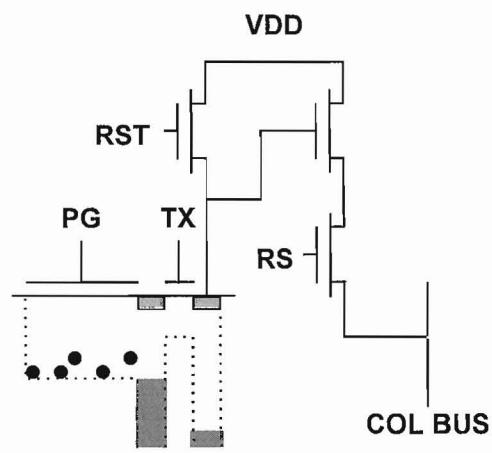

Fig. 5. Photogate-type APS pixel schematic and potential wells. Transfer of charge and correlated double sampling permits low-noise operation.

reset and its resultant voltage measured by the source follower. The charge is then transferred to the output diffusion by pulsing the photogate. The new voltage is then sensed. The difference between the reset level and the signal level is the output of the sensor. This correlated double sampling suppresses reset noise, $1/f$ noise, and fixed-pattern noise due to threshold voltage variations.

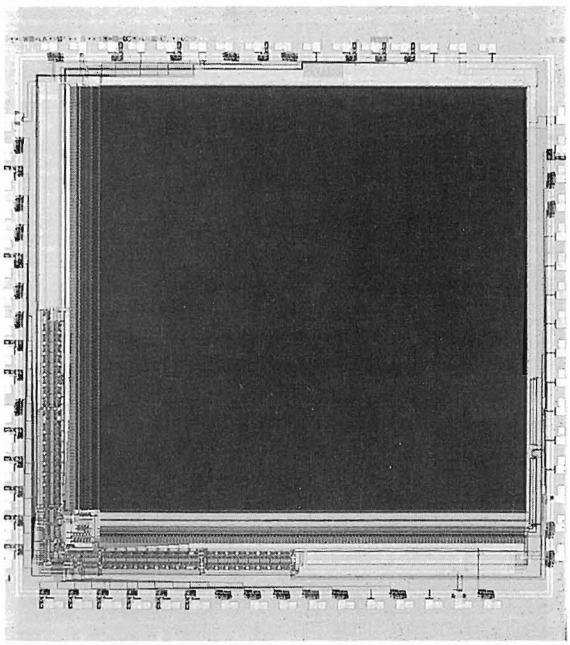

Fig. 6. A JPL 256 × 256 element PG-APS with on-chip timing and control circuits (left-hand side) and analog signal chain including fixed pattern noise suppression (bottom).

The photogate and transfer gate ideally overlap using a double poly process. However, the insertion of a bridging diffusion between PG and TX has minimal effect on circuit performance and permits the use of single poly processes [18]. (Approximately 100 e^- of lag has been attributed to the bridging diffusion [19]). A 256 × 256 element CMOS APS with 20.4 μm pixels implemented using a 1.2 μm *n*-well process with on-chip timing and control logic with 13 e^- rms read noise was reported by JPL [20]. This sensor required only 5 V and clock to produce analog video output (see Fig. 6). Variable integration time and window of interest read out is commanded asynchronously. Arrays as large as 1024 × 1024 with 10 μm pixel pitch in a 0.5 μm process have been developed by a JPL/AT&T collaboration [21].

The photogate-type APS uses five transistors per pixel and has a pitch typically equal to 20 × the minimum feature size. Thus, to achieve a 10 μm pixel pitch, a 0.5 μm process must be employed. A 0.25 μm process would permit a 5 μm pixel pitch. The floating diffusion capacitance is typically of the order of 10 fF yielding a conversion gain of 10–20 μV/e^-. Subsequent circuit noise is of the order of 150–250 μV rms, resulting in a read-out noise of 10–20 electrons rms, with the lowest noise reported to date of 5 electrons rms [14]. The advantage in read noise for the photogate pixel is offset by a reduction in quantum efficiency, particularly in the blue, due to overlying polysilicon.

5. Analog signal processing

On-chip analog signal processing can be used to improve the performance and functionality of the CMOS image sensor. A charge integration amplifier is used for passive pixel sensors and sample and hold circuits typically employed for active pixel sensors. JPL has developed a delta-difference sampling (DDS) approach to suppress FPN peak-to-peak to 0.15% of saturation level [11]. Other examples of signal processing demonstrated in CMOS image sensors include smoothing using neuron MOSFETs [22], motion detection [23], programmable amplification [24], multiresolution imaging [25], video compression [26], dynamic range enhancement [27], discrete cosine transform (DCT) [28], and intensity sorting [29]. Continued improvement in analog signal processing performance and functionality is expected. Other computational-type optical sensors have been demonstrated that use CMOS analog signal processing [30,31].

6. On-chip analog-to-digital converter (ADC)

CMOS image sensors with on-chip single-slope ADC have been reported [32–34] as has related work in on-chip ADCs for infrared focal-plane array read out [35–37]. There are many considerations for implementation of on-chip ADC [38,39]. The ADC can be implemented as a single-serial ADC (or several ADCs, e.g.

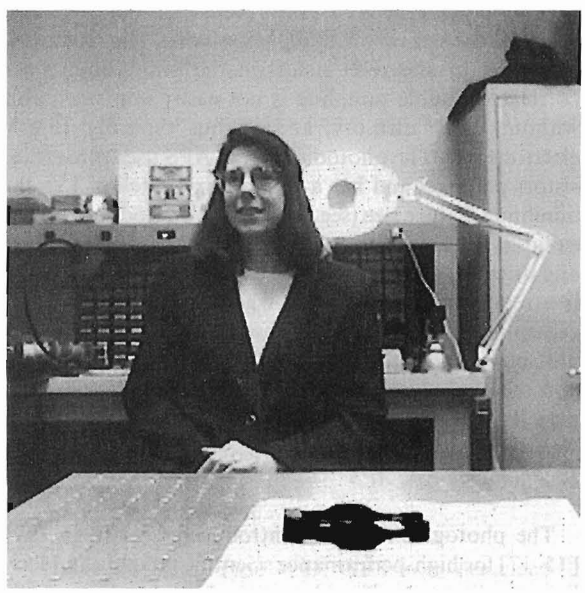

Fig. 7. Unprocessed image taken from a Photobit 256 × 256 element sensor with on-chip ADC operating at 30 fps. Note no blooming from light and lack of other artifacts.

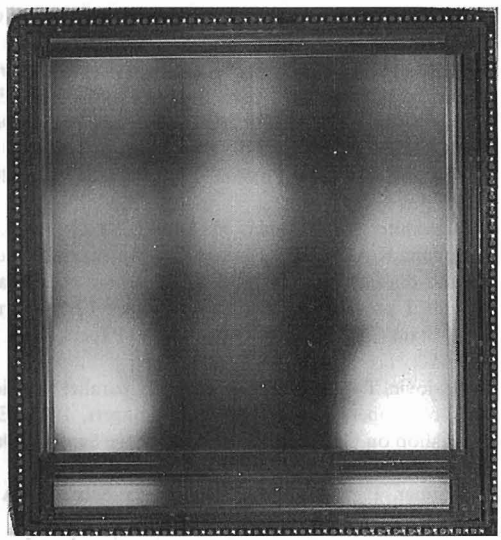

Fig. 8. A JPL 1024 × 1024 photodiode-type CMOS APS with 1024 column-parallel single-slope ADCs for slow-scan scientific applications.

one per color) that operate at near video rates (10 Msamples/s). The ADC can also be implemented in-pixel [40–42] and operate at frame rates (e.g. 30 samples/s). We have been pursuing column-parallel ADCs where each (or almost each) column in the pixel array has its own ADC (see Fig. 7) so that each ADC operates at the row rate (e.g. 15 ksamples/s). In this architecture, single-slope ADCs work well for slow-scan applications (Fig. 8) but dissipate too much power for video-rates. Oversampled ADCs require significant chip area when implemented in column-parallel formats [43]. A successive approximation ADC has a good compromise of power, bit resolution, and chip area. On-chip ADC enables on-chip DSP for sensor control and compression preprocessing.

7. Future outlook

The future prospects for CMOS image sensors are bright. There has been rapid progress in realizing cost-effective pixel sizes (see Fig. 9). The effect of predictable trends in CMOS technology, based on the industry standard technology roadmap, were examined by Fossum and Wong of JPL/IBM [44,45]. To at least 0.25 μm minimum feature sizes, it appears that the standard CMOS process will permit the fabrication of high-performance CMOS image sensors.

Highly miniaturized imaging systems based on CMOS image sensor technology are emerging as a competitor to CCDs for low-cost visual communications and multimedia applications. The CMOS active pixel sensor (APS)

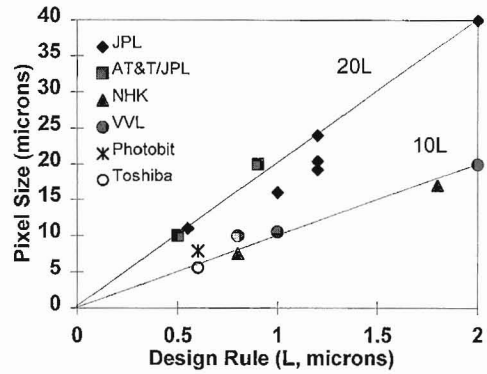

Fig. 9. Scaling trend in pixel size versus design rule. It is expected that pixel pitch must be between 5 and 10 μm to be competitive.

technology has demonstrated noise, quantum efficiency, and dynamic range performance comparable to CCDs with greatly increased functionality and much lower system power. CMOS image sensors with on-chip timing and control, and analog-to-digital conversion are enabling one-chip imaging systems with a full digital interface. Such a "camera-on-a-chip" may make image capture devices as ubiquitous in our daily lives as the microprocessor.

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I. INTRODUCTION