Briefs

CMOS Active Pixel Image Sensor with Simple Floating Gate Pixels

Jun-ichi Nakamura, Sabrina E. Kemeny, and Eric R. Fossum

Abstract—**A new pixel structure using a simple floating gate (SFG) has been proposed. The pixel consists of a coupling capacitor, a photogate, a barrier gate and a MOS transistor. It features complete reset that results in no kTC noise and no image lag, high blooming overload protection, nondestructive readout (NDRO), and CMOS compatibility. Its basic operation has been confirmed with a 32(H) × 27(V) pixel area array. Since the pixel structure is relatively simple, small pixel size is feasible.**

I. Introduction

An active pixel sensor (APS) is defined as an image sensor with one or more active transistors located within each pixel [1]. High signal-to-noise ratio is expected due to its signal amplification and buffering capability. Its x–y addressing scheme provides flexible readout modes, including random access, windowing and electronic shuttering. These features are desirable for smart sensor applications.

The purpose of this brief paper is to report a new APS pixel structure and the characterization of a prototype sensor array. The pixel consists of a coupling capacitor, a photogate, a barrier gate, and a MOS transistor. Due to the floating gate charge sensing scheme and the relatively simple structure, the pixel is referred to as the Simple Floating Gate (SFG) pixel.

II. Operation and Design

A. Operation of the SFG Pixel

A schematic diagram and potential diagrams of the SFG pixel are illustrated in Fig. 1. During the image sensor operation, the barrier gate BG and the drain diffusion are dc biased. The latter acts as the reset drain during the reset period and lateral overflow drain during the integration period for the signal electrons, as well as the drain of the MOSFET. The photogate (PG) is capacitively coupled to the row address line through the coupling capacitor C_0 and is connected to the gate of the MOSFET. The source diffusion is coupled to the vertical signal line and the load transistor is located at the bottom of the imaging area.

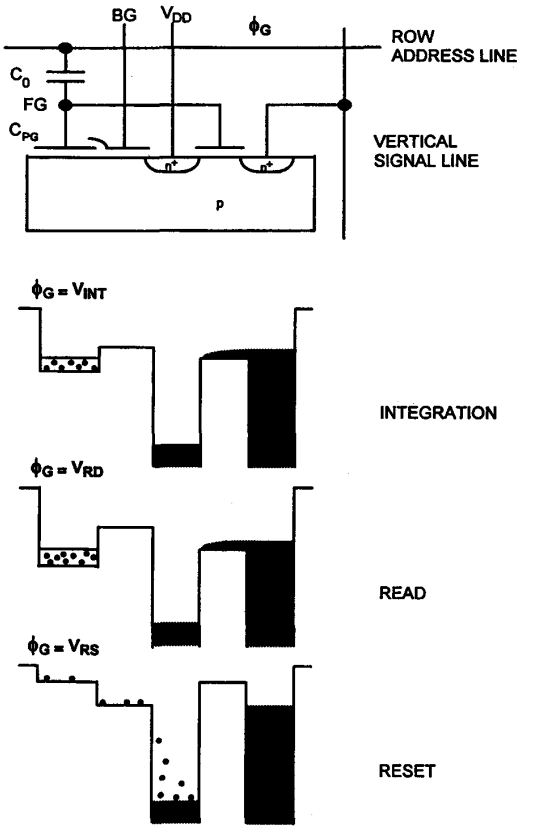

Fig. 1. A schematic diagram and potential diagrams of the SFG pixel.

During the integration period, the row address line is biased at the integration voltage V_{INT}. The photon-induced signal electrons are accumulated in the potential well under the PG. When the row address line is pulsed to the readout voltage V_{RD}, the floating gate potential, which depends on the amount of the accumulated signal charge, is sensed by the source follower. When the row address line is biased at V_{RS} (which is usually the ground), the signal charge accumulated under the PG is drained to the drain diffusion.

The charge-to-voltage conversion factor at the photosite S and the voltage swing ratio, which is defined as the ratio between the voltage change of the row address pulse and the voltage change of the floating node are given by

$$S = \frac{1}{(1+\alpha)\beta + \alpha + \alpha\gamma + \gamma} \cdot \frac{q}{C_{PG}} \tag{1}$$

$$\frac{V_{FG}}{\phi_G} = \frac{1}{\left(\frac{\alpha}{1+\alpha} + \gamma\right)/\beta + 1} \tag{2}$$

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J.-i. Nakamura is with Olympus America Inc. and is presently a Distinguished Visiting Scientist at the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA.

S. E. Kemeny and E. R. Fossum are with the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA.

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where $\alpha = C_{dep}/C_{PG}$, $\beta = C_0/C_{PG}$, $\gamma = (C_g + C_{ol})/C_{PG}$, C_{dep} the depletion capacitance of the PG, C_g the gate capacitance of the MOSFET in the pixel, and C_{ol} the overlap capacitance coupled to the floating gate, respectively. There is a trade off for the β value between the charge-to-voltage conversion factor and the voltage swing ratio that determines the dynamic range, as is shown in the above equations. The β value was set at 0.5 for the prototype sensor array. Resulting fill factor was 45% for PG area and 16% for PG area without the second poly Si.

B. Image Sensor Architecture

Since the purpose of this chip is to confirm the basic operation of the proposed pixel, the conventional peripheral readout circuitry reported elsewhere [2], [3] was used with only one modification. The modification is that a level mixing circuit is placed between the row decoder and the row address lines, in order to generate row address pulses with three voltage levels, each of which corresponds to V_{INT}, V_{RD}, and V_{RS} in Fig. 1. The sensor array consists of 32(H) × 27(V) pixels with a pixel size of $40 \times 40\,\mu m^2$ The chip was implemented in a 2 μm double-poly n-well CMOS process.

During the horizontal blanking period, the following operations are performed. The readout voltage V_{RD} is applied to the selected row and the signal level is sampled and held on a holding capacitor. After this signal level sampling, the row address line is biased at the reset voltage V_{RS}, thereby resetting the PG. Then, the row address line is again biased at the readout voltage V_{RD} and the reset level is sampled and held on the other holding capacitor. During the succeeding horizontal scanning period, the signal level and the reset level, which are held at the holding capacitors, are read out in parallel. The FPN is suppressed by subtracting the reset level from the signal level.

A vertical signal line is coupled to an n-channel MOSFET which acts as an active load. This load transistor and a MOSFET within a pixel form a source follower. Since MOSFET's within pixels on a column are coupled to the common load, this configuration acts as a winner-take-all circuit. During the readout period, the voltage on the floating gate of the selected pixel must be higher than the floating gate voltage of all nonselected pixels.

III. Experimental Results

The output saturation voltage was measured to be 180 mV under the condition where $V_{DD} = 5$ V, $V_{INT} = 4.0$ V, $V_{RD} = 5$ V, $V_{RS} = 0$ V, and $V_{BG} = 1.25$ V. This low value is consistent with the operation of a capacitively biased floating gate. In general, larger V_{INT}, V_{RD} and lower V_{BG} increases the saturation voltage. Good linearity (gamma = 1.0) was obtained. FPN was suppressed to 1 mVp-p by use of the crowbar sampling (CBS) operation [3]. Read noise was measured to be 215 μV_{rms}. Noise sources include 1/f and thermal noise of MOSFET's in the pixel and column sample-hold circuits and kTC noise at the holding capacitors. Reducing the 1/f component of MOSFET, which was measured to be higher than anticipated, will reduce the random noise.

A reproduced image is shown in Fig. 2. No blooming was observed. "Dark clipping" is prevented by choosing V_{RD} sufficiently higher than V_{INT} to ensure that a saturated pixel yields a higher floating gate voltage during readout than a dark pixel in integration mode. Dark clipping leads to an apparent lower saturation signal.

IV. Discussion

Since the reset operation of this pixel is considered to be complete, no kTC noise and no image lag appear. The lateral overflow drain structure suppresses blooming phenomena. The floating gate pixel allows nondestructive signal readout. This nondestructive readout (NDRO) capability is useful for image processing and extending the sensor dynamic range by multiple readout. The relatively simple pixel structure is suitable for high-density arrays. When it is scaled, the charge-to-voltage conversion factor increases as is predicted by (1), which effectively reduces input referred read noise.

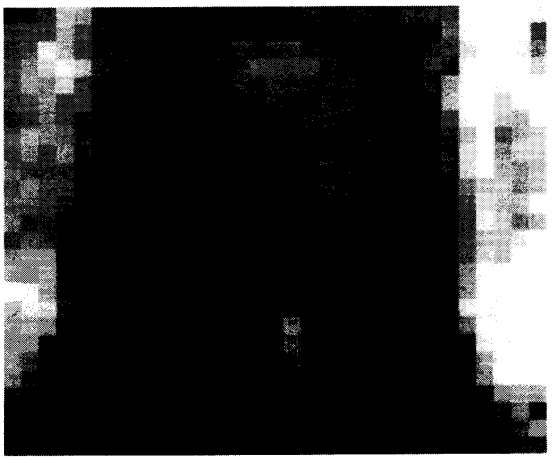

Fig. 2. A reproduced image of the 32(H) × 27(V) area array.

There are drawbacks inherent to the floating gate structure. One is poor response in short wavelength region of the spectrum due to the poor transmission rate through the poly-silicon layer(s). The other is poor charge handling capacity. They must be improved in future work where smaller pixel size will be pursued. Also, the effective fill factor will be increased by use of a microlens.

V. Conclusion

A new simple floating gate pixel has been proposed. It features complete reset that results in no kTC noise and no image lag, high blooming overload protection, nondestructive readout (NDRO), and CMOS compatibility. Its basic operation has been confirmed with a 32(H) × 27(V) pixel area array. Since the pixel structure is relatively simple, smaller pixel size is feasible. When it is scaled, the charge-to-voltage conversion factor increases, which effectively reduces input referred read noise. Blue light response and charge handling capacity must be improved in future work.

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