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CCD FOCAL PLANE IMAGE PROCESSING

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ABSTRACT

A charge-coupled device (CCD) based analog VLSI circuit containing 576 digitally programmable pixel processors arranged in a 24 X 24 array is described. The use of this array as a single-instruction, multiple-data (SIMD) parallel image processor for real-time applications is discussed. The low power, high throughput nature of the array may make it attractive for missile seeker applications.

1.0 INTRODUCTION

In high velocity intercept applications, the real-time preprocessing of image data can be a severe bottleneck in system design, particularly when low power and low weight are critical issues. These preprocessing functions include non-uniformity correction, smoothing, thresholding, and edge detection. Acquisition of target information at frame rates on the order of several hundred hertz for modest imager sizes (128 X 128) can result in the required preprocessing of approximately one million pixels per second. If each pixel takes 100 elementary operations to process, processing throughput on the order of 100 MIPs is required. Conventional digital image preprocessing approaches using accuracies of the order of 8 bits are hard pressed to achieve this throughput, even with advances in VHSIC hardware. In this paper, an analog approach to image preprocessing which exceeds these throughput requirements using charge-coupled device (CCD) structures is described.

2.0 CHARGE-COUPLED COMPUTING

The use of CCD structures to perform image processing functions on the focal plane (image plane) of an imager has been described previously.[1,2] In this approach, a digitally programmable CCD structure is used to effect analog arithmetic operations. A collection of CCD circuits to perform various arithmetic functions in discrete time is referred to as a charge-coupled computer. These functions are chosen to enable image processing tasks such as convolution to occur on the focal plane. Arithmetic functions include addition, differencing[3], magnitude comparison[4], splitting[5], and a local pixel multiplexer[6]. Typically, these circuits perform the arithmetic functions in 25 clock cycles or less with accuracies generally exceeding 1 part in 256 or eight equivalent bits. This accuracy is generally more than sufficient for image preprocessing. The real-estate required to implement each function is typically $100L^2$, where L is the design rule. In any CCD, charge transfer is initiated by clocking electrodes, and in charge-coupled computing this translates into the arithmetic functions being controlled by timing. Since the routing of signals is also controlled by electrode clocking, the order of arithmetic functions in a charge-coupled computer is digitally programmable through appropriate electrode clocking. The drawback of this approach is that a large number of wires for control signals is associated with each charge-coupled computer, and the real-estate required by wiring often exceeds that required by the computer itself.

3.0 IRET - A FOCAL PLANE IMAGE PROCESSOR

An analog VLSI circuit consisting of an array of simple charge-coupled computers has been designed and fabricated. A functional block diagram of an individual charge-coupled computer is shown in Fig. 1. It consists of a charge splitter, a differencer, a bidirectional stack (parallel load, serial out) for local detector multiplexing, a comparator-controlled differencer, and a

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1. J.D. Joseph, P.C.T. Roberts, J.A. Hoschette, B.R. Hanzal, and J.C. Schwanebeck, "A CCD-based parallel analog processor," Proc. SPIE vol. 501, pp. 238-241 (1984).
2. E.R. Fossum, "Charge-coupled computing for focal plane image preprocessing", Opt. Eng. vol. 26(9), pp. 916-922 (1987).
3. E.R. Fossum and R.C. Barker, "A linear and compact charge coupled chage packet differencer/ replicator", IEEE Trans. Electron Devices vol. ED-31(12), pp. 1784-1789 (1984).
4. R.E. Colbeth, N.A. Doudoumopoulos, E-S. Eid, S.E. Kemeny, A. Montalvo, and E.R. Fossum, "High performance charge packet comparison for analog CCD applications", Columbia University, CTR Tech. Rep. (1987).
5. S.S. Bencuya and A.J. Steckl, "Charge packet splitting in charge domain devices", IEEE Trans. Electron Devices ED-31(10), pp. 1494-1501 (1984).
6. E-S. Eid and E.R. Fossum, "CCD focal plane array analog image processor", Proc. SPIE vol. 977, paper 32 (1988).

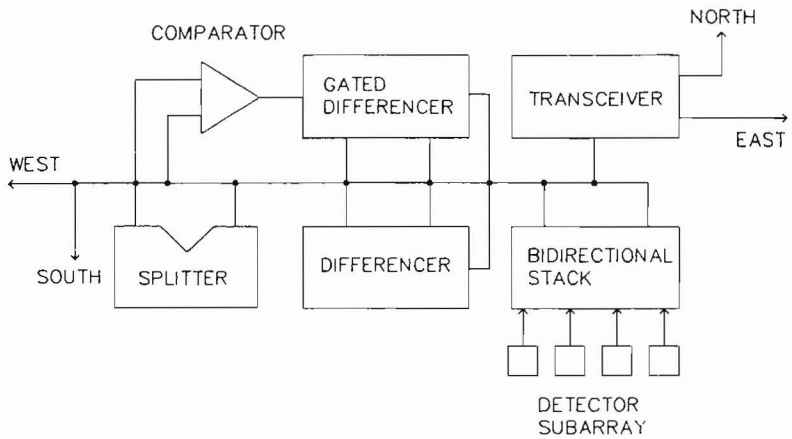

Fig. 1. Block diagram of charge-coupled computer used in IRET unit cell.

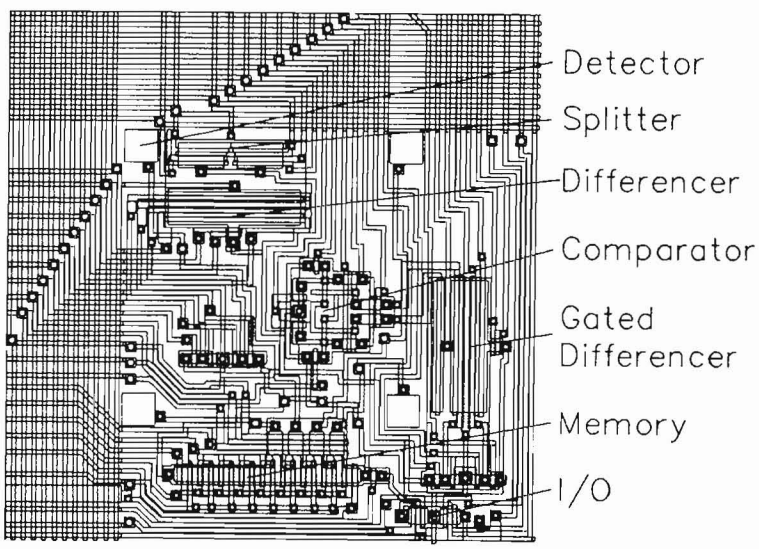

Fig. 2. Layout of charge-coupled computer used in IRET unit cell.

transceiver for nearest neighbor communication of processors. The splitter takes in a charge packet Q_i and forms two quantities each $Q_i/2$. The differencer forms an output charge packet Q_{12} equal to $Q_{i1}-Q_{i2}$, where Q_{i1} and Q_{i2} are input charge packets. Note that Q_o cannot be less than zero, so that absolute value of difference can be formed by $Q_{12}+Q_{21}$. The comparator compares two input quantities, Q_{ia} and Q_{ib} and controls the adjacent gated differencer such that the difference output is unchanged for $Q_{ia}>Q_{ib}$ but is zero for $Q_{ia}<Q_{ib}$. Thus, the gated differencer performs differencing

conditionally on the output of the comparator. The bidirectional stack, in addition to serving as a multiplexer for the detector subarray, has four empty storage wells for short term memory or accumulator functions. The transceiver routes an input charge packet to the computer to the north or east. Note that the computer functional blocks are connected by a low capacitance analog "unibus" over which all charge packets pass. Charge is passed over this bus in a manner analagous to the operation of bucket brigade devices[7] but with improved transfer efficiency. The west and south nearest neighbor processors communicate directly to this bus. The layout of the charge-coupled computer used in IRET is shown in Fig. 2. The fabrication process used is a double metal, double poly CCD foundry process. Second level metal is used for light shielding of the computing circuitry.

The detectors used in the current implementation of IRET are simple photodiodes with primary response in the visible wavelengths. The photodiodes are each 22 X 22 um^2 and are located on a 180 um pitch. Since each processor serves four photodiodes, the pixel array size for IRET is 48 X 48 or 2,304 elements. For IR seeker applications, a hybrid approach is considered optimal with the detector pitch remaining at 180 um but with 100 % fill factor. Hybridizing "bumps" would be placed where the photodiodes are presently located. Non-uniformity correction of IR detectors is not provided for in the current implementation of IRET. The use of non-volatile long term memory would be required to provide long term correction capability.

IRET is designed to operate with clock widths of at least 40 nsec. With a maximum of 25 clock cycles required to execute any arithmetic function, the corresponding throughput of an individual processor is on the order of one million instructions per second (1 MIPs). Operations such as smoothing, thresholding, and edge detection typically require 250 instructions per pixel. Since each processor serves four pixels, the total processing rate of IRET may be expected to be 1000 frames per second, or 576 MIPs. In practice, IRET will be limited by its output multiplexer (CCD serial register) so that demonstrable frame rates may be of the order of 100 frames per second. Due to the capacitive nature of CCDs, power scales with operating frequency. Thus, at 100 frames per second, processed imagery (250 instructions/pixel) will only cost approximately 2 mW for the entire

7. F.J. Sangster, IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers, XIII p. 74 (1970).

48 X 48 array throughput of 57.6 MIPs - an extremely low value. The use of focal plane image processing with cooled imagers is not expected to contribute significantly to the total thermal budget.

The total noise associated with computation is calculated to not exceed that introduced by detector shot noise. The overall dynamic range is estimated to be 54 dB.

Improved image resolution can be achieved with a trade-off. A lower degree of parallelism on the focal plane can used to obtain a higher detector pitch. Currently, four detectors are served by one processor. Raising this to 81 detectors (subarray size 9 X 9) per processor will yield an estimated detector pitch of 55 um. The throughput of IRET will drop, however, to a maximum of 50 frames per second with 250 instructions/pixel/frame.

4.0 CONCLUSIONS

The design and performance of a CCD focal plane image processor has been described. The processor, currently under test, is expected to yield high throughput with low power consumption. Such a processor is well-suited for missile seeker applications. Results of testing will be published when available.

5.0 ACKNOWLEDGMENTS

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