Supplement to

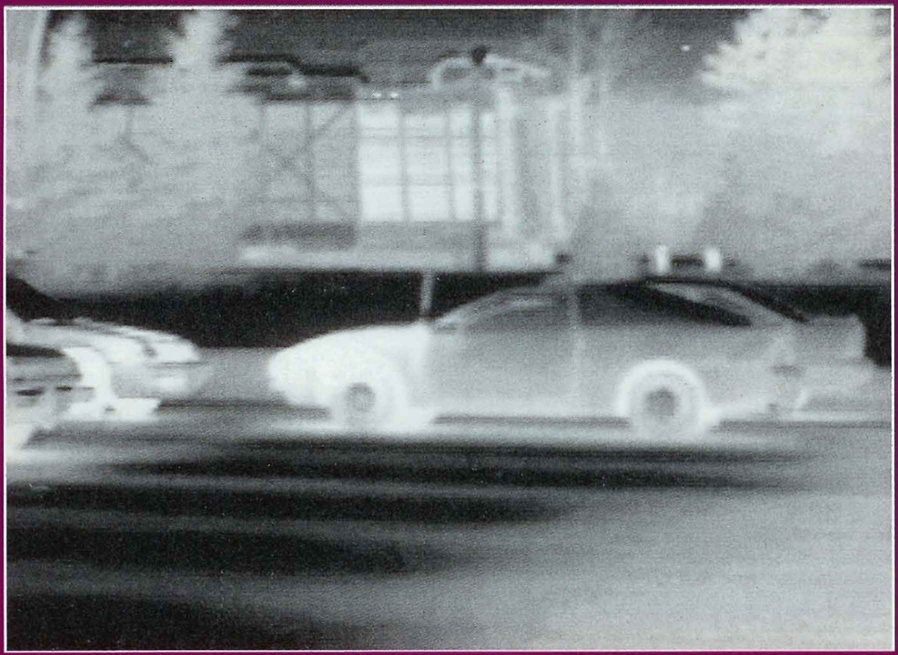
Laser Focus World

GLOBAL ELECTRO-OPTIC TECHNOLOGY AND MARKETS

June 1993

- Active-pixel sensors
- Multiplexers
- Thermography
- Night vision
- Thermal imaging

# DETECTOR HANDBOOK
## Imaging Systems



# Active-pixel sensors challenge CCDs

**With random access, nondestructive readout, and easy integration with on-chip electronics, active-pixel sensors may supplant CCDs in imaging applications.**

*Eric R. Fossum*

The active-pixel sensor (APS) is a new type of sensor device emerging from the most advanced image-sensor research and development laboratories in Japan. These sensors may one day supplant charge-coupled devices (CCDs) in many imaging applications. A CCD relies on the shifting of charge to read out the image. In contrast, an APS acts similarly to a random access memory (RAM) device, wherein each pixel contains its own selection and readout transistors. The signal readout then take place over metallic wires rather than by shifting charge, giving the APS advantages such as random access, nondestructive readout, and integrability with on-chip electronics.

This article looks at active-pixel sensors within the framework of current CCD operating characteristics. It summarizes activities in various laboratories and describes applications for APS devices, such as high-definition television (HDTV) and imaging systems for high-radiation environments.

### CCD versus non-CCD image sensors

Charge-coupled devices were invented around 1970 at AT&T Bell Telephone Laboratories (Murray Hill, NJ). Since then, CCDs have become the primary technology used in scientific image sensors. The technology is complex, even for students of semiconductor device physics. Readers interested in CCD operation are referred to texts by Yang[1] or Tompsett.[2]

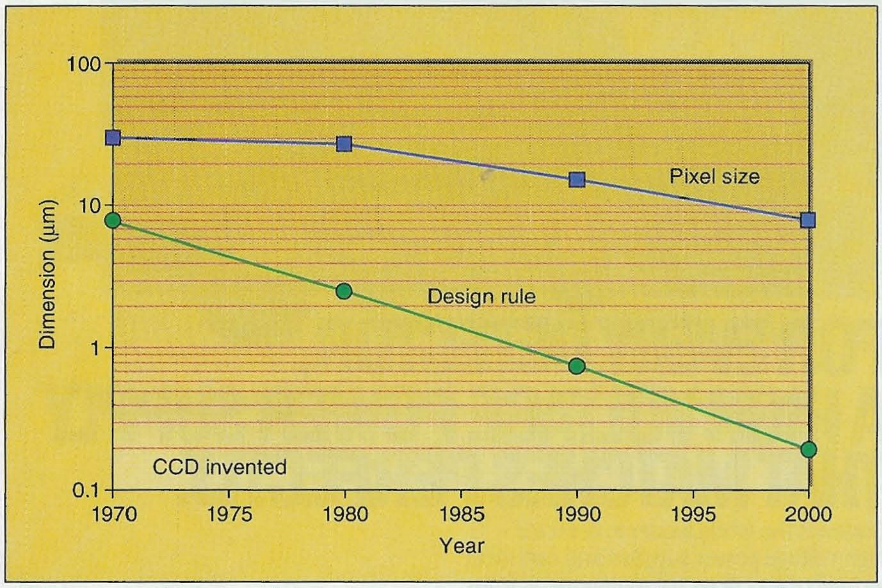


FIGURE 1. Logarithmic chart of device feature size versus pixel size tracks the advance of microlithographic technology. Future miniaturization trends call for higher resolution from APS devices.

Various non-CCD-based image sensor technologies are also on the market, including the photodiode array, the charge-injection device (CID), and hybrid infrared image sensors. The first two have large input-referred noise floors, typically several hundred electrons (rms) for a single read; they are not covered in this article.

Hybrid infrared sensors could, in principle, be adapted for visible use. The hybrid approach, in which a detector is bump-bonded, pixel by pixel, to a readout multiplexer is an expensive technology and is limited in size to approximately 512 × 512 formats. Typical noise floors of such hybrid focal-plane arrays are in the 30 electrons rms range.

In the active-pixel sensor, several active transistors are monolithically integrated in the pixel for readout purposes. These transistors are used for pixel readout selection and for amplifying or buffering the pixel output signal. Twenty years ago, an active-pixel sensor with a practical pixel size was not possible because of microlithography limitations. The technological push of the semiconductor industry has since driven microlithography to the submicron regime, and 1.25-µm CMOS is practically an industry standard.

In the 1970s, CCDs were attractive because only three electrodes/pixel were required for operation and a 30-µm pixel was possible. Today, the fundamental advantage CCDs had over any other imaging technology has been eclipsed by the shadow of microlithography fabrication. Pixel size is now determined more by scientific imaging optics than by microlithography constraints. Thus, a new window of opportunity exists to take advantage of microlithography advances because the

ERIC R. FOSSUM is a research technologist and assistant manager, Imaging Systems Section, Jet Propulsion Laboratory, Pasadena, CA 91109.

digital microelectronics industry, driven by needs for speed and miniaturization, continues its inevitable evolution (see Fig. 1).

### CCD strengths and weaknesses

The virtues of the CCD include its high sensitivity, high fill-factor, and large-format capability. High sensitivity follows from a net quantum efficiency of around 40%, the high fidelity of CCD readout, the low-noise-output amplifier (typically, five electrons rms). The high fill factor of a CCD pixel (80%–100%) arises because the metal-oxide-semiconductor (MOS) photodetector is also used for signal readout. The large format of CCDs—typically 1024 × 1024, but it can be as large as 5120 × 5120—is possible because of the concurrent drive of semiconductor memory-chip manufacturers to improve silicon wafer quality and fabrication yield.

The need for nearly perfect charge transfer is the Achilles' heel of CCD technology; it is also fundamental to the device operating principle. The CCD relies on the transfer of charge (usually electrons) from under one MOS electrode to the next through sequencing of voltages on the electrodes. The electrons are transported through the bulk silicon material over macroscopic distances—up to centimeters—before reaching the output sense node. A typical CCD has three electrodes/pixel, so in a 1024 × 1024 imager, the electrons may be shifted, on the average, several thousand times. The ratio of electrons successfully transferred to the number left behind per electrode is the charge-transfer efficiency (CTE). The CTE of a CCD needs to be as close to 100% as possible for acceptable scientific performance. A single defect in bulk silicon can trap electrons and degrade the efficiency.

For example, if the CTE is given by $\eta$, the net fraction of signal transferred after $m$ transfers is simply $\eta^m$. Thus, if a CCD is operating with a CTE of 0.9999 (1 electron lost out of 10,000), then a typical pixel signal in a 1024 × 1024 image sensor undergoes a fidelity degradation of nearly 20% by the time it reaches the output amplifier.

Because this performance is unacceptable in most applications, large-format CCDs have been developed within CTEs ranging from 0.99999 to 0.999999. For a CCD charge packet of 1000 electrons, a CTE of 0.99999 implies that only one electron is lost for every 100 transfers. It is remarkable that CCDs have been developed with such a high level of transfer efficiency and that the number of defects in a silicon wafer has dropped to essentially zero.

The need for nearly perfect charge transfer leads to a number of performance weaknesses in CCD technology. For example, CCDs are susceptible to bulk radiation damage. In space applications, CCD image sensors are continuously bombarded by energetic particles and photons, which can cause significant bulk displacement damage. Damaged silicon traps electrons and reduces transfer efficiency. Typical dose tolerance for a scientific CCD is around 10 krads, depending somewhat on the source. Radiation softness of CCDs is a significant issue for long-duration plan-

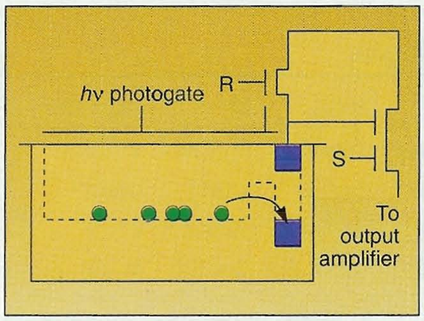


FIGURE 2. Schematic of a simple CMOS-compatible APS shows the charge integration relationship between the photogate, the selection transistor S, and the reset transistor R. The output signal from each pixel is the change in voltage levels at the output node.

etary instruments and certain earth orbits, as well as in many terrestrial applications such as x-ray and electron imaging.

To get high transfer efficiency, CCDs are often driven with relatively large voltages (by microelectronics standards). They also represent high-enough capacitance loads to driving electronics to make on-chip integration of clocks and drivers nearly impractical. Yet, on-chip integration is the key to achieving future camera miniaturization.

The CCD fabrication process is quite different from the complementary metal-oxide-semiconductor (CMOS) process—the preferred technology for implementation of on-chip signal processing—creating a further impediment to miniaturization. Although some integrated CMOS/CCD processes have been demonstrated, undesirable compromises in the performance of CMOS or CCD technology must be made.

Other weaknesses that stem from nearly perfect CTE requirements include the limited spectral sensitivity range (that of silicon), the difficulty of achieving large array sizes (because CTE requirements increase with array size), the difficulty of implementing CCDs with large pixel sizes at high data rates, and limited readout rates.

### Developing APS technology

An example of a simple active-pixel sensor that resembles a short CCD is shown in Fig. 2. Charge is integrated under the photogate PG. To read out the signal, the pixel is selected using transistor S. The output node is reset using transistor R. The signal charge is then transferred from under the PG into the output node.

The change in the source-follower voltage between the reset level and final level is the output signal from the pixel. The source follower might drive a column line terminated with clamp and/or sample-hold circuits. These column-parallel circuits could then be scanned for serial readout of the sensor. Because the illustrated APS requires only a single intra-pixel charge transfer, many of the problems associated with charge transfer in CCDs are eliminated.

If implemented in 0.8-µm CMOS, a 16 × 16-µm pixel could have an intrinsic fill factor of more than 50%. To improve the fill factor to the levels typically associated with CCDs, the emerging microlens technology must be used (see Fig. 3). At Jet Propulsion Laboratory (JPL, Pasadena, CA), this approach is being pursued in conjunction with on-chip analog-to-digital conversion to explore cameras-on-a-chip for future microspacecraft applications.

Much more sophisticated APS structures are being developed elsewhere in order to achieve small pixel size and high fill factors (see table). Toshiba (Kawasaki, Japan) uses a double-gate floating-surface transistor to increase the sensitivity of the output amplifier to 200 µV/electron.[3] To reduce the pixel size, the charge storage area can be located vertically under or over the readout transistor.

The presence or absence of photogenerated charge can be used to modulate the readout transistor output signal of

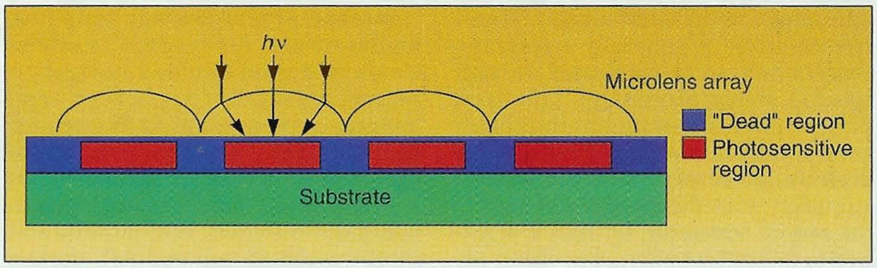
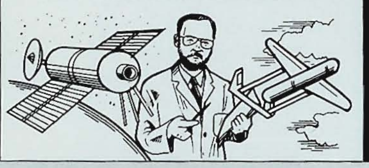
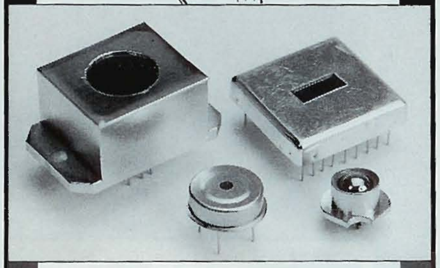


FIGURE 3: Microlenses placed directly above an APS direct more incoming photons (*hν*) to the photosensitive areas, thereby increasing the signal fill factor.





### Attributes of various APS technologies

| | DGFSPT | CMD | BCMD | BASIS | SIT | CMOS APS |
|---|---|---|---|---|---|---|
| Developer | Toshiba | Olympus | Texas Instr. | Canon | Olympus | JPL/Caltech |
| APS Type | Lateral | Vertical | Vertical | Vertical | Lateral | Lateral |
| Output | Lateral | Lateral | Lateral | Vertical | Vertical | Lateral |
| Pixel size (µm) | 13 × 13 | 7.3 × 7.6 | 10 × 10* | 13.5 × 13.5 | 17 × 13.5 | 40 × 40 |
| Sensitivity | 200 µV/e- | 250 pA/e+ | 15.4 µV/e- | 3.5 µV/e+ | 3.0 µV/e+ | 4.0 µV/e- |
| Input-referred noise | 0.8 e- rms | 20 e+ rms | 15 e- rms | 60 e+ rms | 69 e+ rms | 22 e- rms |
| Dynamic range | 75 dB | 70 dB | 72 dB | 76 dB | 86.5 dB | 76 dB |
| Fixed-pattern noise (p-p) | 10% | 5% | 2% | 0.03% | 1.1% | <2% |
| Anti-blooming | Vertical | Vertical | Vertical | none* | none* | Lateral |
| Lag | 0 | 0 | 0 | <0.1% | 70% | 0 |
| Comments | FPN may be reducible by read/reset/ resample | Noise dominated by dark current. Improved by cooling. | *Hexagonal layout | *Can be reduced using clipping operation. | *SIT turns on | Uses 2-µm CMOS design rules. |

an APS. This technique is used by Olympus (Nagano, Japan) in its charge-modulation-device (CMD) approach to APS.[4] Texas Instruments (Tokyo, Japan) created a bulk charge-modulated device (BCMD) in a hexagonal packing format.[5]

A further reduction in pixel size is possible if the current flow in the output transistor is vertical rather than horizontal, so the substrate acts as one of the transistor terminals. Olympus uses this technique in its static induction transistor (SIT) active-pixel-sensor device.[6] A vertical bipolar approach is used by Canon in its base-stored image sensor (BASIS).[7]

Each of the these technologies has advantages and disadvantages. Fixed-pattern noise is generally a common concern but can be eliminated through on-chip signal processing. The fixed pattern noise arises due to threshold-voltage nonuniformities across a large-area image sensor. Because output amplifiers track the threshold voltage of the output transistor, an APS is sensitive to this offset pattern, but clamp circuits can be used to nearly eliminate this phenomenon.

### APS applications

Numerous applications for active-pixel sensors are being explored. Some APS work is driven by HDTV; signal gain prior to readout is desirable in high-bandwidth HDTV applications. Electronic still cameras are another area of interest because the APS is more amenable to camera miniaturization and power minimization than the CCD.

Imaging systems operating in high radiation environments represent another application area of APS technology. These include laboratory and spaceborne scientific APS-based cameras, medical instrumentation, nuclear instrumentation and space-based surveillance systems.

Because APS technology simplifies region-of-interest readout, machine vision and guidance and navigation sensors are another application area. Imaging devices operating in extended spectral ranges may also benefit from the active-pixel concept. Because CCDs are notoriously hard to implement in nonsilicon materials, near-infrared and short-wavelength infrared APS devices may be easy to develop. Ultraviolet APS sensors made from materials such as silicon carbide (SiC) might also be possible with the APS approach.

Admittedly, it is difficult to displace CCD technology, which has had nearly 25 years to mature, and any incumbent technology has its ardent supporters. Some operations, such as time-delay-and-integration (TDI) and pixel binning will be harder to achieve with APS devices than with CCDs.

> *Given the high level of performance already achieved, it is highly likely that active-pixel sensors will have a profound impact on imaging systems of the future.*

The APS concept has, however, generated much discussion among domestic image sensor manufacturers. Several have already indicated an interest in exploring this emerging technology. Therefore, given the relative immaturity of APS technology and the high level of performance it has already achieved, it is highly likely that active-pixel sensors will have a profound impact on imaging systems of the future. ☐

REFERENCES

1. E. S. Yang, *Microelectronic Devices*, McGraw-Hill, NY, NY (1988).
2. C. Sequin and M. Tompsett, *Charge Transfer Devices*, Academic Press, NY, NY (1975).
3. Y. Matsunaga et al., *IEEE Trans. Electron Devices 38*(5), 1044 (1991).
4. M. Ogata et al., *IEEE Trans. Electron Devices 38*(5) 1005 (1991).
5. J. Hynececk, *IEEE Trans. Electron Devices 38*(5), 1011 (1991).
6. T. Mizoguchi et al., *IEEE Trans. Electron Devices 38*(5), 1021 (1991).
7. Y. Nakamura et al., *IEEE Trans. Electron Devices 39*(6), 1341 (1992).

*Bulk reprints of all* LFWorld *articles can be ordered from June Bozarth, reprints manager, PennWell Publishing Co., at (800) 331-4463 or (918) 835-3161.*

**YOUR RATING, PLEASE...**
Is this article of value to you? Please circle appropriate number on the Reader Service Card.
YES—367 NO—368