A Linear and Compact Charge-Coupled Charge Packet Differencer/Replicator

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Abstract—A new charge-coupled circuit for creating a charge packet equal to the difference of two input charge packets is analyzed. The circuit features inherent linearity through the use of quasi-three-dimensional charge-coupling, and can be implemented in a compact way. Depending upon the areal ratio of the circuit's primary electrodes, various fixed gains in the transfer characteristic may be obtained. The signal charges are transferred to the circuit through remote and possibly multiple floating diffusion collectors which may also function as summing nodes. Multiple copies of the output charge packet may be regenerated without refreshing the circuit input.

A large geometry prototype device has been fabricated and characterized. The device demonstrates the operation of the circuit and features less than -40-dB linearity distortion over a dynamic range which exceeds 70 dB. Improved performance is expected in smaller geometry devices.

I. Introduction

CHARGE-COUPLED devices (CCD's) have been used for analog signal processing almost since their inception. In the majority of the applications, the charge transfer mode of charge coupling is utilized for signal delay or for signal readout multiplexing. In more recent applications, the signal charge is manipulated to effect preprocessing of information. Arithmetic operations typically performed on the charge packet include summation with other charge packets, dynamic splitting into sub-packets, and differencing.

Although charge packet summation is relatively straight forward to implement in a CCD, charge packet differencing has been more difficult. In the latter case, it is desired to create a charge packet equal in magnitude to the difference in two input charge packets. To obtain linearity and balance, the differencing operation is often implemented through an active analog differential amplifier circuit which is costly in terms of real estate consumption and power. The input signal charges are sensed either by floating diffusion or floating gate means and transduced into a pair of voltages. These voltages are then used in the active differential circuit to produce an output voltage proportional to the difference of the two input charge packets. This voltage may then be used to generate a charge packet of the desired magnitude.

Manuscript received April 18, 1984; revised July 11, 1984. This work was supported by the Hughes Aircraft Company Missile Systems Group, Canoga Park, CA, and by a Howard Hughes Ph.D. Fellowship for E. R. Fossum.

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For more computationally intensive circuitry, such as that which might be employed in a focal plane imaging device for image preprocessing, a premium is placed on computing accuracy and real estate consumption. For these applications, the approach described above for charge packet differencing is cumbersome and undesirable.

In this work, a circuit which utilizes vertical charge-coupling between the electrodes and semiconductor surface in addition to the usual lateral charge-coupling (hence the term quasi-three-dimensional) performs the differencing operation. The input charge packets are coupled to precharged electrodes through a gate charge subtraction cycle. Using the charge on the electrodes, an output charge packet is formed through surface potential equilibration, though not in the electrode voltage mode normally associated with this charge setting method [1].

II. Theory of Operation

The operation of the charge packet differencing circuit is schematically illustrated in Fig. 1(a)-(c). The basic charge packet differencer consists of two primary electrodes, which are labeled A and B, an input diode (V_{D2}), an input transfer gate (V_{X2}), an output transfer gate (V_{XO}), and a pair of MOSFET precharge switches. The primary electrodes are also connected to two p^+ diffusions which act as collectors for the signal charge input. Also illustrated are two charge packets Q_{SA} and Q_{SB} which are retained in storage wells for future input into the differencer circuit. In the discussion below, it is assumed that the MOS capacitors are nearly ideal and that the primary electrodes are of equal area. In addition, it is assumed that the oxide thicknesses are equal as well as the semiconductor doping profiles. For this p-channel implementation, all the applied biases are negative.

In Fig. 1(a), the primary electrodes are precharged to voltage V_0 by momentarily pulsing the precharge MOSFET's on through V_{PCS}. Following the precharge phase, the potential on the two primary electrodes remains at V_0 as long as the negative gate charge does not leak away through the reverse biased p-n junctions. The application of the negative electrode charge results in the formation of two deeply depleted MOS potential wells. In Fig. 1(a), the input transfer gate bias V_{X2} is also set equal to V_0 so that with the input diode reverse biased by V_{D2}, any charge thermally generated under the primary electrodes is collected by the input diode. The major purpose of the input transfer gate is to avoid an overlap capacitance of the input diode and a primary electrode.

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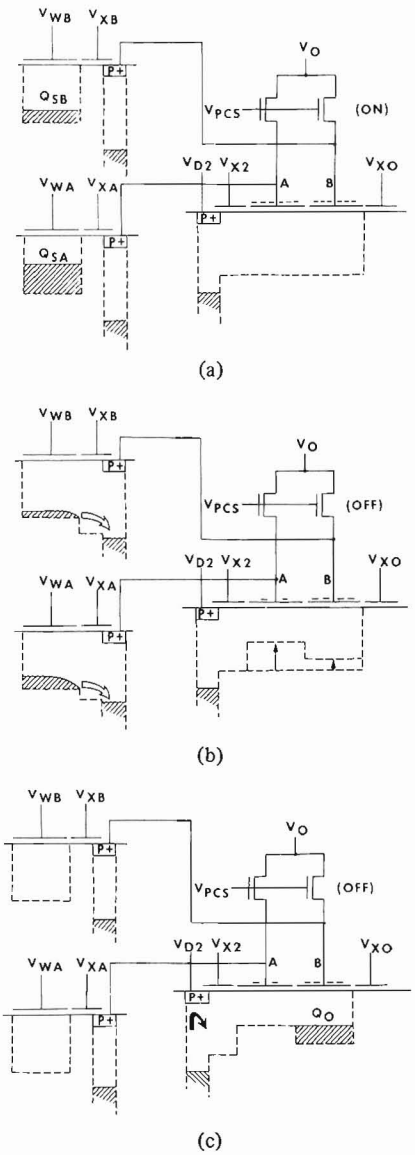

Fig. 1. Basic operation of charge packet differencer. (a) Precharge phase. Electrodes A and B precharged to V_0 by pulsing V_{PCS}. (b) Gate charge subtraction phase. Signal charge transferred to differencer by floating diffusion collection. (c) Output charge packet formation using a surface potential equilibration technique. $Q_0 = Q_{SA} - Q_{SB}$.

In Fig. 1(b), the two input charge packets are collected by the floating diffusions when transfer gates V_{XA} and V_{XB} are pulsed. The positive minority-carrier signal charge collected by the floating diffusions results in a partial discharge or subtraction of the negative charge on the primary electrodes. The change in electrode charge is accompanied by an equal but opposite change in deeply depleted semiconductor space charge, which may also be viewed as a change in potential well depth as shown in the figure. Note that if the initial gate charge is sufficient, multiple gate charge subtraction cycles may be effected so that the primary electrodes function as summing nodes. Alternatively, the gate charge may be subtracted as an integrated discharge current, perhaps provided by an illuminated photodiode. Note also that the "wire" which connects the collector diffusions to the primary electrodes may pass through a MOSFET channel without significantly changing the discharge process, though care must be taken if this channel is clamped off to avoid channel charge feedthrough to the differencer circuit.

In Fig. 1(c), the input diode has been momentarily pulsed to near substrate potential so as to forward bias the diode with respect to the adjacent surface and consequently inject minority carriers into the potential wells under the differencer electrodes. When the input diode is returned to a reverse biased condition, some of the surface charge spills out and is collected by the diode, with the exception of charge which is trapped under electrode B due to the shallower potential well under electrode A. This fill and spill process is wholly analogous to surface potential equilibration method of setting CCD charge, except that the potential well depth under electrode B changes as the spill process proceeds. The charge trapped under electrode B is determined by the difference in input signal charges and the areal ratios of the primary electrodes.

The captured output charge packet may be transferred from the differencer circuit through the use of the output transfer gate. Once Q_0 has been transferred out, the fill and spill process may be repeated to create a second output charge packet equal to the first. If subsequent output charge packets are summed, then the device can be used as a time domain integer multiplier. For example, such a feature is useful for charge packet doubling. Note that if the circuit is constructed with the B input left out, the circuit acts as charge packet replicator and can be used as charge packet "copying machine."

The transfer characteristic of the differencer circuit is now calculated including the effects of stray capacitance, unequal primary electrode areas and fixed oxide charge. The lumped stray capacitance arises from the floating collector diffusion capacitance, the precharge MOSFET source diffusion capacitance, wiring capacitance, and other miscellaneous effects. Electrode areal ratios other than unity are useful for implementing fixed gain or attenuation. It will be seen that fixed oxide charge has a null effect if it is the same under each electrode.

Following the precharge cycle, the A and B primary electrodes are charged with charge Q_A and Q_B respectively. Let the fixed oxide charge under electrode A be Q_{OXA} and the fixed oxide charge under electrode B be Q_{OXB}. Let the charge stored on the stray capacitance associated with electrode A be Q_{SCA} and the charge stored on the stray capacitance associated with electrode B be Q_{SCB}. Following gate charge subtraction, let the A electrode gate charge be Q'_A, and the stray capacitance charge be Q'_{SCA}. Let the B electrode gate charge be Q'_B and stray capacitance charge be Q'_{SCB}. With the A and B input charges being Q_{SA} and Q_{SB}, respectively, charge conservation yields

$$Q'_A + Q'_{SCA} = Q_A + Q_{SCA} + Q_{SA} \tag{1a}$$

and

$$Q'_B + Q'_{SCB} = Q_B + Q_{SCB} + Q_{SB}. \tag{1b}$$

Following the fill and spill phases, Gauss' Law applied to each MOS capacitor yields

$$Q'_A + Q_{OXA} + Q_{DA} = 0 \tag{2a}$$

and

$$Q'_B + Q_{OXB} + Q_{DB} + Q_0 = 0 \tag{2b}$$

where Q_{DA} and Q_{DB} are the depletion layer charges under the A and B electrodes respectively, and Q_0 is the charge trapped under electrode B. Also, since the surface potentials under each electrode have been equalized by means of the fill and spill process, equal depletion layer charge areal densities are implied by the equal doping profiles, provided that the voltage drop across the captured minority carrier charge packet Q_0 is negligible. Thus

$$Q_{DA}/A_A = Q_{DB}/A_B \tag{3}$$

where A_A and A_B are the areas of electrodes A and B.

Substituting (1) into (2) and using (3) yields

$$Q_0 = \alpha Q_{SA} - Q_{SB} - \Delta Q_0 \tag{4}$$

where

$$\Delta Q_0 = \alpha(Q'_{SCA} - Q_{SCA}) - (Q'_{SCB} - Q_{SCB})$$

and

$$\alpha = A_B/A_A$$

where it has been assumed that $Q_{OXA}/A_A = Q_{OXB}/A_B$ and that during the precharge phase both potential wells under the primary electrodes are equally deep depleted so that $Q_A/A_A = Q_B/A_B$.

The change in stray capacitance charge can be related to the change in effective differencer electrode voltage through the differential stray capacitances C_{SCA} and C_{SCB} such that

$$Q'_{SCA} - Q_{SCA} = C_{SCA}(V'_A - V_A) \tag{5a}$$

and

$$Q'_{SCB} - Q_{SCB} = C_{SCB}(V'_B - V_B). \tag{5b}$$

In the special case that α is unity and the differential stray capacitances are equal

$$\Delta Q_0 = C_{SC}(V'_A - V'_B). \tag{6}$$

Finally, recognizing that

$$Q_0 = C_{ox}(V'_A - V'_B)$$

where

$$C_{ox} = A_B \epsilon_o \epsilon_{ox}/d_{ox} \tag{7}$$

such that ϵ_o is the permittivity of free space, ϵ_{ox} is the relative dielectric constant of the oxide, and d_{ox} is the oxide thickness, (4) becomes

$$Q_0 = \alpha_{SC}(Q_{SA} - Q_{SB}) \tag{8}$$

where α_{SC} is the stray capacitance attenuation factor of a unity gain differencer equal to $(1 + C_{SC}/C_{ox})^{-1}$. The effect of stray capacitance is to attenuate the output charge packet. To minimize this effect, the stray capacitance should be smaller than the oxide capacitance of the primary electrodes. Note that if Q_{SA} is less than Q_{SB}, there is no output charge packet captured.

In the absence of appreciable stray capacitance, the differencer may be configured with a fixed non-unity gain as described by (4) with $\Delta Q_0 = 0$. For example, with the A to B electrode area ratio set to 2, and no charge subtracted from the B electrode, the output of the circuit is a charge packet equal to half the value of the input charge packet.

It is interesting to note that leakage of charge from the primary electrodes has little effect on the transfer characteristic of a unity-gain configured differencer if the leakage rate from each electrode is equal. This is due to the output charge packet being related to the difference in charge subtracted from each electrode. In most operations though, the B electrode will be at a higher effective potential than the A electrode, so that the charge subtracted from the B electrode due to leakage will be larger and the output charge packet will be attenuated accordingly.

The maximum charge packet which can be handled by this circuit depends on the precharge bias, the device area, the breakdown strength of the oxide, and the breakdown strength of the silicon. It is generally undesirable to have breakdown in the silicon, so that for moderate doping levels, the silicon breakdown strength determines the maximum precharge bias. For lower doping levels, charge transport through the oxide for full buckets becomes the dominant issue. The maximum charge which can be subtracted from the A electrode is approximately equal to the total deep depletion charge under the electrode following the precharge phase. For charge packets exceeding this level, the subsequent fill and spill phases are hampered by the lack of a channel under the A electrode. This maximum input charge in turn determines the maximum output charge according to the relationship expressed by (4), assuming no gate charge subtraction on the B electrode.

III. Prototype Device Fabrication

In order to demonstrate the operation of the charge packet differencer circuit described above, a prototype device was fabricated in the modest Yale semiconductor processing facility. The devices were fabricated on 2-$\Omega \cdot$ cm n-type wafers. Diode and channel stop diffusions were performed using a spin-on dopant source. All wet oxidations were carried out at 900°C to reduce oxidation induced silicon defects and suppress bucket dark current [2]. The gate oxide was grown at 1000°C in dry oxygen. Single level aluminum electrodes separated by submicrometer gaps (typically 0.5 μm) were formed using a shadow evaporation process [3]. Completed devices were scribed and bonded into chip carriers. All device characterization was carried out with the packaged device in a light tight shielded test box.

The gate oxide was determined to be 550 Å thick using high-frequency capacitance measurements. The interface trap density near midgap was determined to be approximately 2-3 $\times$ $10^{10}/\text{cm}^2 \cdot \text{eV}$ using a high-low-frequency capacitance technique [4]. The surface doping concentration was $1.0 \times 10^{16}/\text{cm}^3$. Using a pulsed capacitance transient method [5], the dark current was measured to be in the 10 nA/cm^2 range. No fabrication techniques other than wet oxidation temperature reduction and phosphorous doped channel stop gettering [6] were employed to reduce the dark current. The surface hole

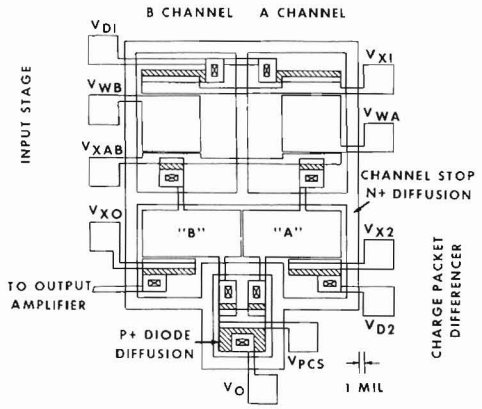

Fig. 2. Layout of prototype device for demonstrating circuit operation. A 1-mil (or 25.4 μm) design rule was utilized. Interelectrode gap size exaggerated.

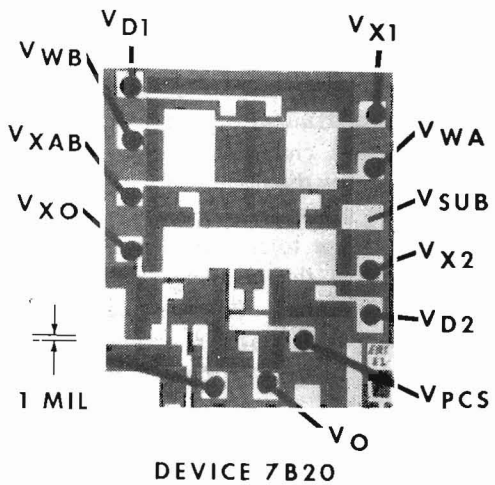

Fig. 3. Photograph of bonded prototype device. 1 mil = 25.4 μm.

mobility for the devices was 146 $cm^2/V \cdot s$ determined from MOSFET test sites. A charge transfer efficiency test site was not included in the chip layout since the large geometries required by the Yale design rules were a priori acknowledged to yield less than optimal performance and multiple lateral charge transfers are not employed in the differencer circuit. Though not relevant to this study, high quality 33-Å-gate oxide MOSFET's and capacitors were successfully fabricated as part of the process used to make the prototype differencer devices as has been reported previously [7]-[9].

A layout of the prototype device is shown in Fig. 2, and a photograph of the fabricated device is shown in Fig. 3. Note that a 1-mil (25.4 μm) design rule was employed (with the exception of the submicrometer inter-electrode gap). The layout consists of three stages, a dual input stage, the actual differencer circuit stage, and an output amplifier stage (not shown in the figures). The input stage consists of two metering wells, each 254 μm by 254 μm in size, for generating the input charge packets using the surface potential equilibration technique. The differencer primary electrodes A and B were laid out as symmetrically as possible to achieve balanced operation with unity gain. In retrospect, the differencer electrode geometry should have been made narrower but longer

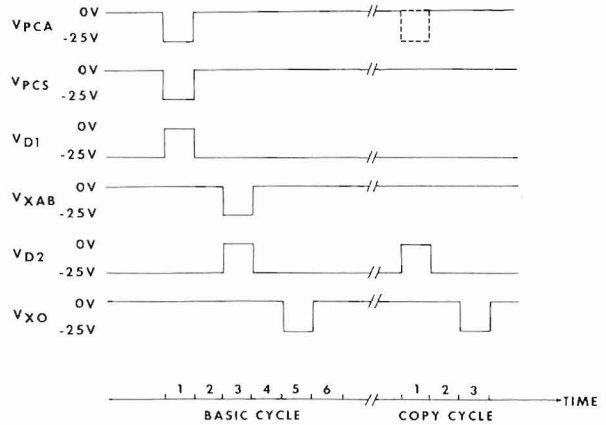

Fig. 4. Timing diagram for clocked biases used in characterizing the prototype device. V_{PCA} refers to the output amplifier precharge or reset MOSFET. Typical pulse width used was 50 μs.

to improve operating speed, though speed was not an initial issue. Also, more care should have been taken to reduce stray capacitance attenuation effects in the prototype layout. For example, the underlap capacitance of the floating collector diffusion and input stage output transfer gate contributes a significant stray capacitance. The output amplifier stage used for reading out the differencer output charge packet is a source-follower configured MOSFET [10] with a large value of W/L and an external load resistor.

IV. Device Characterization

A timing diagram illustrating the clocked biases applied to the prototype device is shown in Fig. 4. Due to the large geometries employed in the device layout, the fundamental clock period was kept at 50 μs to accomodate the diffusion limited charge transfer [11]. Note that the gate charge subtraction phase is coincident with the fill phase. Although it is conceptually more difficult to visualize the dynamics of this operation, the total differencing time is reduced by such timing without significantly affecting the output charge packet. In order to separate the linearity distortion and gain of the input stage and output stage combination, a separate test site on the chip was employed. By measuring the dc input current to the separate input stage and the corresponding response of the output amplifier, it was found that the output amplifier delivered a linear 1-V response per 37.7 pC of input charge for an external source-follower load resistance R_L of 500 kΩ.

Using this calibration factor and stray capacitances computed from the layout, an ideal transfer characteristic for the charge packet differencer prototype circuit may be constructed as shown in Fig. 5. The ideal performance shows output voltage as a function of input stage A and B channel voltages for V_{X1} set equal to -4.0 V. For increasing A channel input voltage and fixed B channel voltage, the output should rise linearly. For some fixed A channel input voltage and increasing B channel input voltage, the output voltage should drop linearly. The output signal should be clipped at zero since for Q_{SA} smaller than Q_{SB} no output charge packet should be captured.

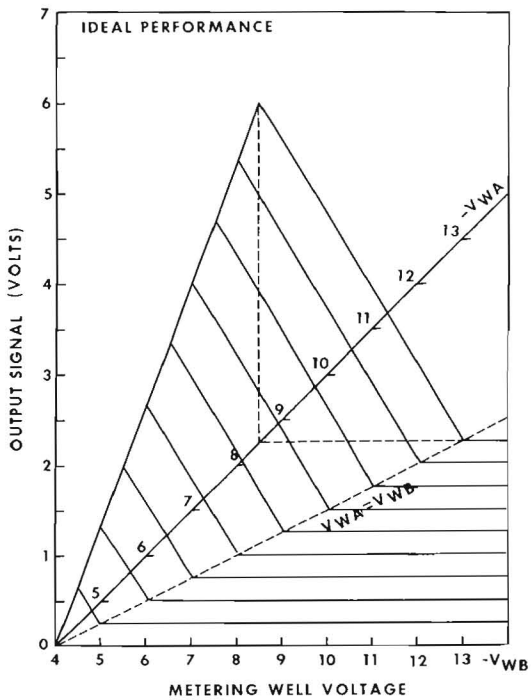

Fig. 5. Ideal transfer characteristic for the differencer circuit using layout geometry and measured values for doping concentration oxide thickness, and output amplifier calibration, assuming V_{X1} set at -4.0 V.

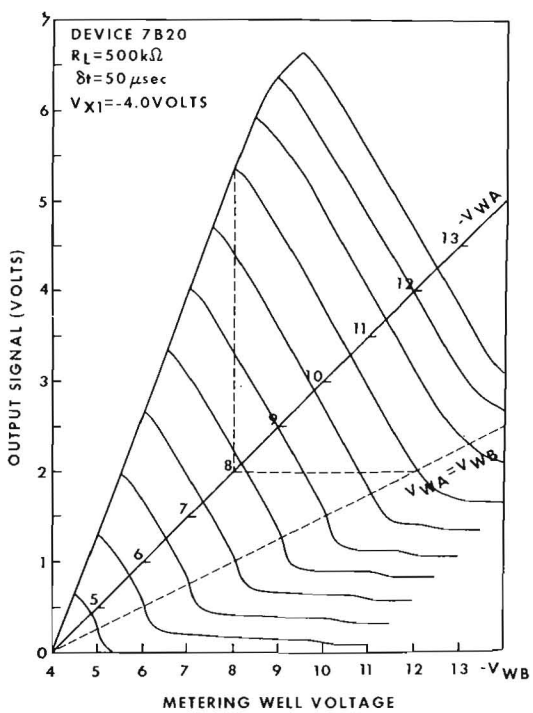

Fig. 6. Measured transfer characteristic of prototype device.

This ideal performance surface may be compared to the experimentally measured performance surface shown in Fig. 6. The prototype device performs well despite its large geometry. The device begins to exhibit input saturation behavior for input charge packets exceeding a 5.0-V input bucket, which is in quantitative agreement with a saturation level calculated using a precharge voltage of - 20 V on the A electrode. The output signal voltage (defined as the change in source-follower output voltage relative to some reset level) appears to drop below zero for large values of V_{WB} because a dark current generated signal, which depends somewhat on the B electrode charge state, has been already subtracted in Fig. 6. The linearity is quite good except near the extremes of the transfer characteristic. This rounding effect is due to charge transfer inefficiency during the fill and spill process and is expected to be eliminated in smaller geometry devices.

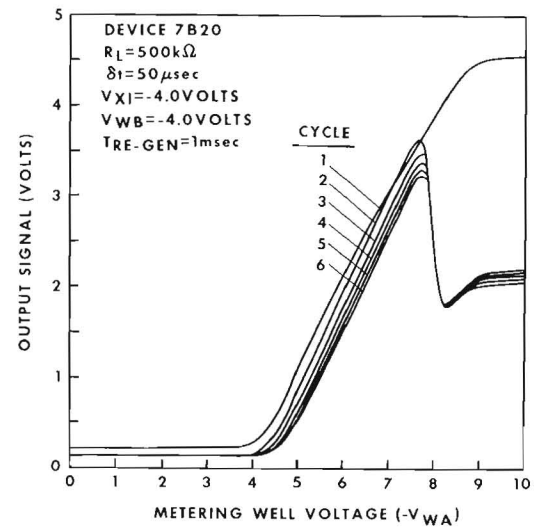

Fig. 7. Transfer characteristic for A channel of differencer for multiple output charge packet regeneration cycles performed at 1-ms intervals.

The linearity of the prototype device in the central part of the transfer characteristic is better than -40 dB measured using the technique of Espley [12], over a dynamic range (defined for a signal to noise ratio of unity) which exceeds 70 dB. The dynamic range measurement was limited by test station noise whose magnitude was estimated from an oscilloscope trace. The equal primary electrode areas yields excellent balance between the A and B channels with an A channel gain ($\Delta V_{OUT}/\Delta V_{WA}$) of 0.89 and a B channel gain ($\Delta V_{OUT}/\Delta V_{WB}$) of 0.86, depending slightly on the bias conditions. The overall gain of the differencer is 0.82, in good agreement with the evaluated stray capacitance attenuation factor α_{SC} using the layout of the prototype device.

The device was also tested in a multiple cycle operation mode, in which the primary electrodes were not recharged between successive output charge packet regeneration cycles. Output signal as a function of A channel metering well voltage is shown in Fig. 7 for 5 regeneration cycles, 1 m s apart. The change in transfer characteristic with regeneration cycle is due to the leakage of charge from the primary electrodes through the reverse biased p-n junctions. Such leakage effects are diminished at higher operating speeds or shorter regeneration cycle times. The change in transfer characteristic at V_{WA} equal to - 8 V is due to the hampering of the fill and spill cycles caused by the saturation effect discussed above. This characteristic demonstrates the feasibility of building a charge packet "copying machine."

V. Conclusions

A quasi-three-dimensionally charge-coupled circuit for performing a charge packet differencing operation has been analyzed and demonstrated in a prototype circuit. This circuit shows promise for delivering high accuracy in a compact low power way. It was developed as part of a research program to investigate image preprocessing on or just behind the focal plane of an image sensor. In such a system, the charge packet differencer circuit realized in several configurations would form the core of a very compact simple charge-coupled computer arranged in an array format for spatially parallel processing. From this perspective, the results obtained with the prototype device are encouraging. However, it is anticipated that the basic circuit may be useful in other applications where compaction, accuracy, and simplicity are desired.

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