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A CCD-BASED WAVEFORM GENERATOR FOR DRIVING CCD CIRCUITS

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ABSTRACT

A low-power method for on-chip generation of complex timing waveforms for charge-coupled device (CCD) circuits is described. The method utilizes four parallel-in, serial-out CCD shift registers whose outputs are interleaved and amplified to produce the desired waveform. The shift registers are periodically loaded in parallel with the waveform using a hard-wired template, which may be programmed using laser ablation of wire links. The output of the shift registers is preamplified and multiplexed to achieve the highest possible waveform bandwidth. The approach addresses a long-standing problem in CCD circuits of generating complex waveforms on-chip with minimum power and maximum flexibility.

INTRODUCTION

Charge-coupled device (CCD) circuits, while widely used commercially as image sensors, are also well-suited for analog signal processing. Demonstrated applications include correlators, filters, and signal transforms [refs] with performance (e.g. speed, power, and real estate) often surpassing that of digital signal processing circuits. However, a long-standing problem inhibiting the general acceptance of CCD-based analog signal processing is the requirement of many complex timing waveforms as control inputs. These waveforms are often voltage patterns which switch between two reference voltage levels, as illustrated in Fig. 1. For bench-top testing, multi-channel digital pattern generators are used to generate the timing, and the digital signals are amplified and level-shifted before being delivered to the circuit under test. Such an approach yields flexibility at the price of severe hardware and power cost.

In real applications, the pattern generation can be done with a high-speed PROM and an appropriate amplifier circuit. However, the power and circuit board space to generate the appropriate timing offsets the real-estate and power advantages of the intrinsic CCD circuit. Thus, systems designers are often inhibited from choosing CCD circuits.

This paper presents a method using CCDs for the on-chip, low-power generation of the complex timing waveforms suitable for driving CCD-based analog signal processing circuits.

CCD WAVEFORM GENERATION CIRCUIT

The CCD waveform generation circuit consists of a parallel-in, serial-out shift register and an output amplifier. The digital data in the shift register causes the output amplifier to swing between one of two DC voltages (V_H or V_L) which are supplied externally. Although there are several ways to implement the shift register and output amplifier, the method used in a prototype version of the generator currently being fabricated is described. In this case, each shift register is implemented as an NMOS surface-channel four-phase CCD.[ref] To maximize the waveform bandwidth attainable by this method, four shift registers are used and their output multiplexed following a preamplifier stage.

The shift registers are periodically loaded in parallel using the input structure illustrated in Fig. 2, with timing illustrated in Fig. 3. Phases P_1, P_2, P_3, P_4 and I_2 are supplied externally, and phases O_1, O_2, O_3, and O_4, which drive the four-phase shift register, are easily generated on-chip. Each input diode is connected either to clock line I_1 or I_2. Clock lines I_1 and I_2 are held at a high voltage but clock line I_2 is periodically set to ground (substrate) potential, thus loading input wells under phases O_1 and O_2 with charge. The electrical connection from the input diode to either clock line I_1 or I_2 can be made with the last level of metal. Alternatively, links can be made to both and one later selectively ablated with a laser pulse[ref], thus providing programmability. In other implementations, direct laser writing of the wiring connection[ref] or more conventional programmable read-only memory programming techniques to achieve a programmable connection could be used.

Another interesting possibility is to load the CCD shift register optically by periodically illuminating the linear array.

Shifting of the charge proceeds in the usual four-phase fashion, with the input structure arrangement preventing accidental back flow of the signal charge into the reverse-biased input diode. The charge packet is collected by the reset floating diode output structure and preamplifier shown in Fig. 4. The preamplifier is designed to use minimal power and is configured in a manner similar to precharged NMOS ~~domino~~ logic inverters. Input transistor M_I is reset (precharged) during phase P_4 and the CCD output bucket is loaded onto the gate during phase P_1. If there is signal charge, transistor M_I's gate is discharged. Also during phase P_1, the preamplifier inverters are precharged. During phase P_2, transistors M_D, M_2, and M_3 are discharged if signal charge was not present in the output bucket, and transistors M_1 and M_4 are not discharged through transistor M_D during phase P_3. However, with signal charge, transistor M_I is turned off thus preventing the discharge of transistors M_D, M_2, and M_3 during phase P_2, and enabling the discharge of transistors M_1 and M_4 during phase P_4.

In the present implementation, there are four shift registers, four preamplifiers, and a drive amplifier. The actual voltages which drive the preamplifiers are shifted by one phase from preamplifier to preamplifier and each successive register is longer by one electrode. Since each preamplifier output is enabled by only one phase (P_4 in Fig. 4), multiplexing of the outputs to the drive amplifier is readily achieved. Thus, during phase P_4, either transistor M_H or M_L is enabled with the other disabled, depending

the presence of signal charge in the output bucket. Since the voltages P_1, P_2, P_3, and P_4 are larger than V_H or V_L, V_H appears at the output during phase P_4 if no signal charge was in the output bucket and V_L otherwise.

The sizes of the drive amplifier transistors are chosen according to the capacitance they drive and the desired transition time. Several transistors can be tied in parallel and electively disconnected by laser ablation to slow transition times in a programmable fashion. Similar programmability for transition time can be achieved by electively disconnecting parallel capacitance, but using capacitance to slow transition times requires extra power. The geometries of transistors used in the preamplifier and in the drive amplifier (configured for driving x pF) are shown in Table 1.

The preamplifier and drive amplifier performance has been simulated using SPICE modelling. The response of the drive amplifier output to an alternating pattern of zero's and one's is shown in Fig. 5.

DISCUSSION

The power requirements of the configuration have been reduced by using dynamic circuits and for the shift register are estimated to be xx mW per 128-bit long waveform with 20 nsec clock widths. This requirement scales linearly with the bit length of the waveform and the frequency of operation. The shift register, while easily implemented in dynamic NMOS logic, would consume at least as much power at the highest clock rates as the CCD approach, would consume

more power at lower clock rates, and would consume approximately four times the real-estate.[CAZ]

Charge in digital CCD shift registers is usually detected using active comparator circuits[ref]. The power requirement of a comparator can be reduced by timing[ref us] but remains relatively large and undesirable. Since the number of cells in each register is not expected to exceed 32 (for a pattern length of 128 bits), charge transfer inefficiency is not anticipated to significantly degrade the integrity of each bit. The thresholding function served by a comparator is performed in this circuit by the discharge of the input transistor M_I gate. A small charge packet will partially discharge this gate, but transistor M_I will remain able to discharge the gates of transistors M_D, M_2 and M_3 during phase P2. The complete discharge of the M_I gate by a large charge packet can be guaranteed if its capacitance is lower than that of the input well. Excess minority carrier charge from the output bucket not accomodated by the low capacitance output node will diffuse through the reset transistor M_R and be collected by its reverse-biased drain. Thus the noise margin afforded by this approach is large enough to compensate for threshold voltage non-uniformities and an active comparator circuit appears unnecessary.

SUMMARY

A low-power CCD-based waveform generator for driving CCD circuits has been described. The on-chip generator addresses the long standing problem with CCD circuits of complex timing waveforms required for analog signal processing.

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FIGURE CAPTIONS

Fig. 1. An example of four waveforms necesary to drive CCD analog signal processing circuits. The individual waveforms are 16 bits in length.

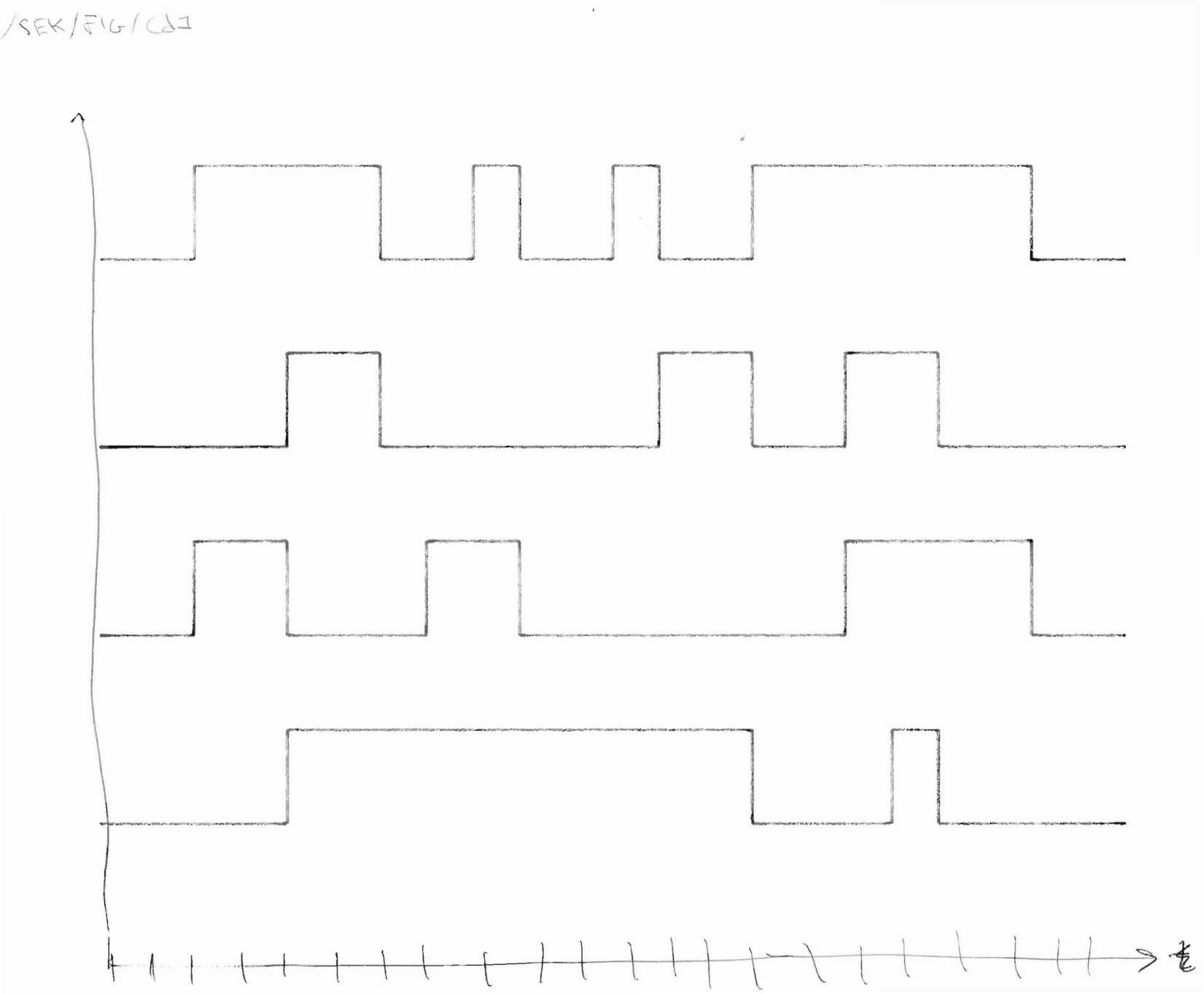
Fig. 2. Layout of prototype waveform generator shift register.

Fig. 3. Timing requirements of CCD waveform generator. Note that phases O_1, O_2, O_3, and O_4 can be readily generated on-chip from phases P1, P2, P3, and P4.

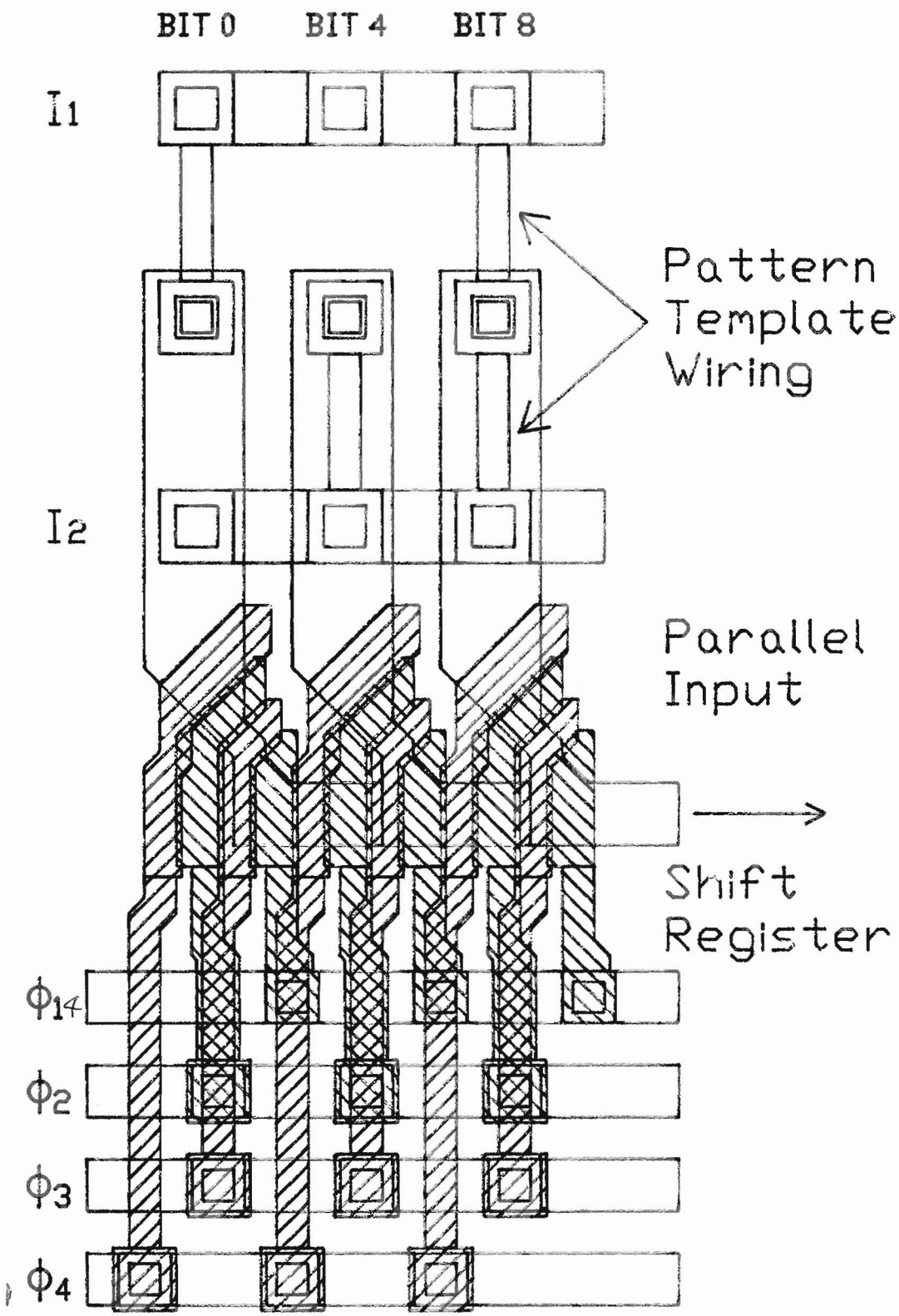
Fig. 4. Circuit schematic of output portion of the waveform generator. Transistor geometry (W/L) is shown next to each transistor. Note that only one of four shift registers and preamplifiers is shown.

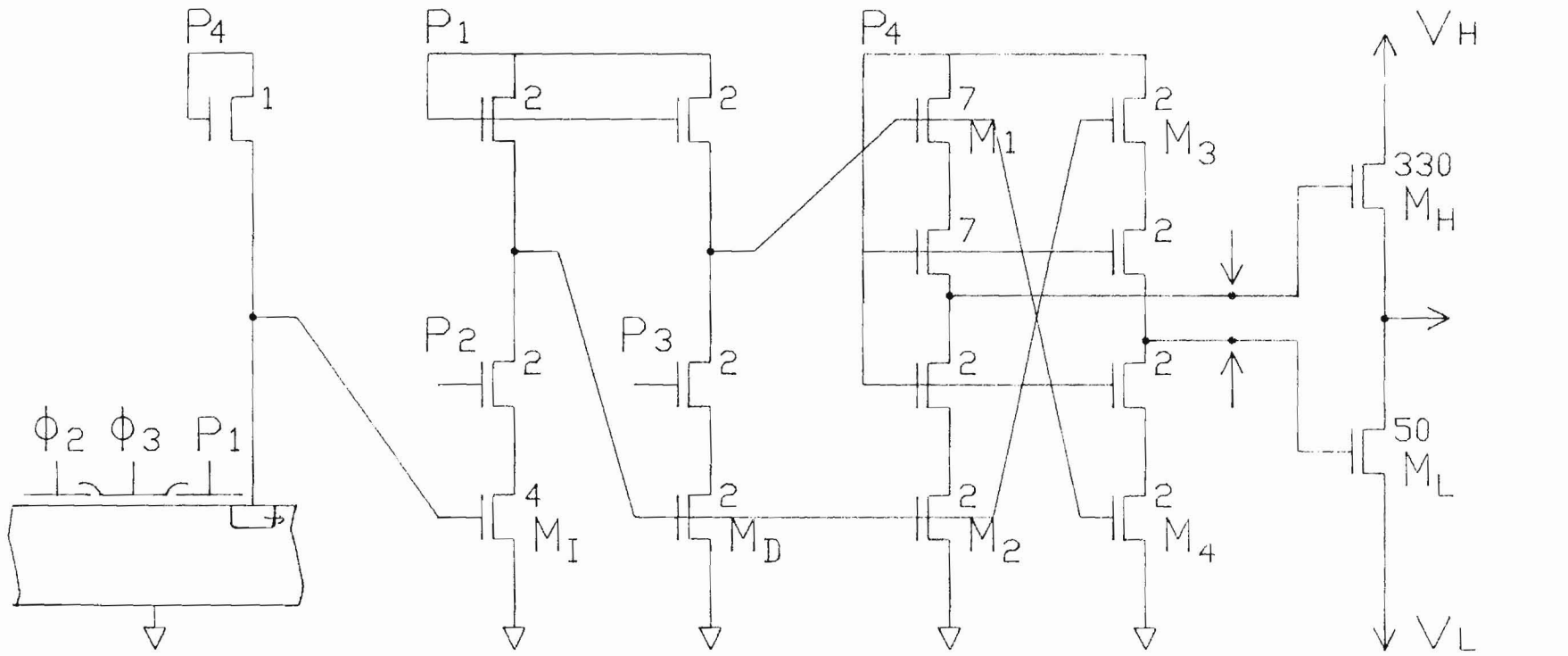
Fig. 5. SPICE simulation of drive amplifier output response driving 22 pF load.

/SEK/FIG/CD1



/Fig/CD2


BIT 0
BIT 4
BIT 8
I1
I2
Pattern
Template
Wiring
Parallel
Input
Shift
Register
ϕ_{14}
ϕ_2
ϕ_3
ϕ_4


P4
1
P1
2
2
P4
7
M1
2
M3
7
2
330
MH
VH
P2
2
P3
2
2
2
ϕ2 ϕ3 P1
4
MI
2
MD
2
M2
2
M4
50
ML
VL
SHIFT
REGISTER
PREAMPLIFIER
DRIVE
AMPLIFIER

/Fig/CD3