A 76 x 77mm^2, 16.85 Million Pixel CMOS APS Image Sensor

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Abstract

A 16.85 million pixel (4,096 x 4,114), single die (76mmx77mm) CMOS active pixel sensor (APS) image sensor with 1.35Me- pixel well-depth was designed, fabricated, and tested in a 0.5µm CMOS process with a stitching option. A hybrid photodiode-photogate (HPDPG) APS pixel technology was developed. Pixel pitch was 18µm. The developed image sensor was the world's largest single-die CMOS image sensor fabricated on a 6-inch silicon wafer.

Keywords: CMOS Image Sensor, APS pixel, stitching.

Introduction

Conventional charge-coupled devices (CCDs) have been fabricated with very large array formats [1]. However, these devices are extremely expensive and difficult to produce with the low defect rates needed for quality imaging. As well depth increases, the necessary increase in pixel and sensor size makes the production of such a device prohibitively expensive. A specially designed CMOS active pixel sensor (APS) device could have a large array format with large full-well capacity (FWC) without the need for designing a fabrication process. The power consumption of CMOS APS devices is small, and it is easy to integrate digital controlers along with analog signal processing circuits.

Achieving large-pixel FWC (>1 million electron) and large-array format (>16 megapixels) were two of the main goals of this work [2]. Large pixel FWC was achieved by using an APS pixel called hybrid photodiode-photogate (HPDPG) [2]. Also extra effort was taken to improve the short-wavelength collection efficiency of the pixel. Pixel pitch was determined to be 18µm by 18µm that could hold more than 1Me-.

Stitched Imager Design: Architecture

Imager die area with 18µm pixels was 80mm on a side. This certainly exceeded the typical reticle size of 20mm. In order to fabricate such a large sensor, a "stitching" process was used. Stitching allows up to nine different pieces of a chip to be repeated across the surface of a wafer. The considerable regularity of CMOS image sensors allows this very useful procedure to be used. High-resolution CMOS image sensors readily lend themselves to this process [3], with the pixel array forming the central repeated piece and the assorted circuits and pads forming the external pieces. The imager comprises nine stitchable blocks (A, B, C, D, E, F, G, H, I) as shown in Fig.1. Block E was the main block forming the pixel array. It contained 512 by 512 pixels that were stitchable on four sides. It was repeated 64 times (8 x 8) to form a 4,096 by 4,096 pixel array. Extra rows and columns of open and covered pixels were

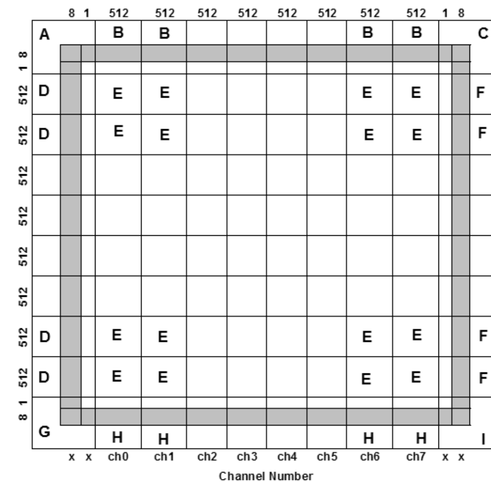

Fig. 1. Imager array and stitchable block map.

placed on the surrounding blocks to form a stitchable design. Each surrounding block had eight closed (dark) and one open pixel row or column. There were 4,112 by 4,114 pixels placed in the pixel array. 4,096 by 4,114 of them could be read. The rest were used as barrier pixels and kept in reset. Effective imaging pixels totaled 16.85 million. Die size was 76.08mm x 77.55mm. Block D contained 512 row decoders and row drivers, 8 by 512 dark and 1 by 512 imaging pixels. Block G contained row and column decoder controllers and digital and analog buffers. Charge-mode readout circuitry, controllers, column decoders, and analog signal processors were placed in block H. The imager has eight differential analog outputs working in parallel. Blocks A, B, C, F, and I were mostly composed of power and signal routings and pads. The imager chip after fabrication on a 6-inch wafer is shown in Fig. 2.

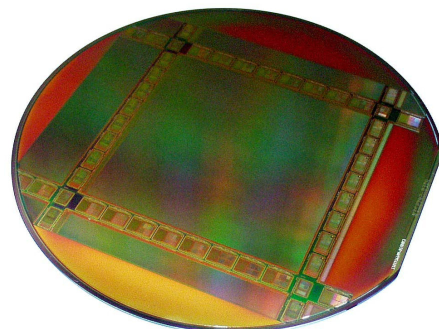

Fig. 2. 6-inch wafer photo of 4Kx4K CMOS APS imager.

Stitched Imager Design: Pixel

HPDPG-type APS pixel layout is shown in Fig.4. It comprises a parallel connected photodiode and photogate imaging elements [2]. HPDPG pixel has a nonlinear light response set

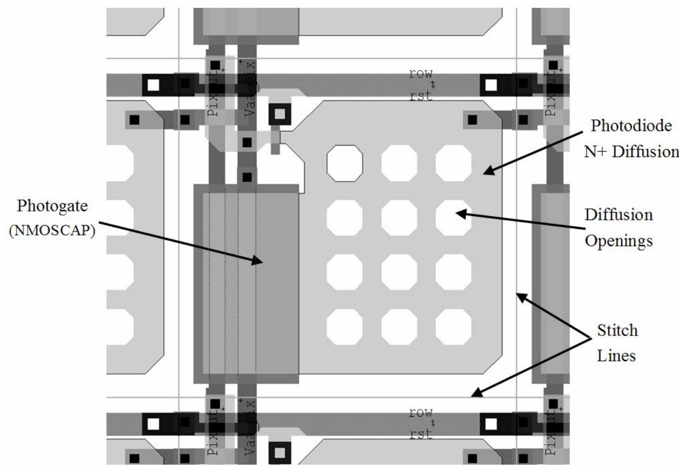

Fig.4. 4-way stitchable HPDPG APS pixel layout.

by the photogate bias voltage. A number of diffusion openings were placed on the photodiode to improve lateral collection and to increase the junction capacitance. The pixel is designed in such a way that it is stitchable on all four sides.

Stitched Imager Design: System Integration and Testing

A full custom printed circuit board (PCB) base packaging solution was developed. The packaging PCB has two headers bringing control and other necessary signals to a controller board. The controller board contains FPGAs, DACs, ADCs, USB controllers, and memory. Packaging PCB comprises a large sit plane and 156 bonding pads. A fully populated PCB package and mounted imager is shown in the Fig. 5.

Conclusion

A raw, reproduced image taken by the 4Kx4K imager is shown in Figure 6. Measured characteristics of the imager are given in Table.1. Total pixel count was 16.85 million (4,096 by 4,114) with a single 76.08mm by 77.55mm die. Full well depth of the imaging HPDPG APS pixel was 1.35Me-. The dynamic range of the imager was 75dB due to the higher readout noise at 240e-. The imager consumes 500mW on single 5V power supply while running at 1.25 fps.

The CMOS APS image sensor chip presented was the world's largest single-die CMOS image sensor fabricated on a 6-inch silicon wafer to date. In addition, developed CMOS HPDPG APS pixel technology achieves a unit-area pixel well-depth of 12.345 Ke-/μm^2.

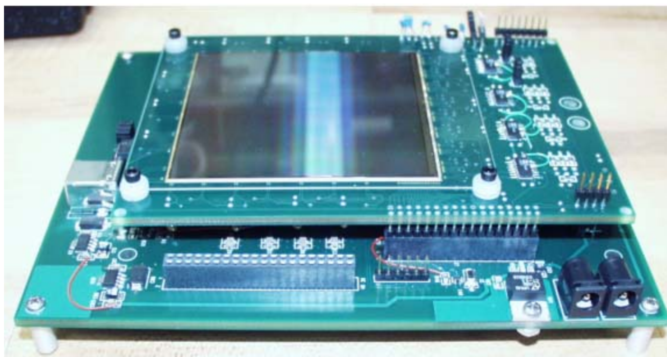

Fig. 5. Controller and packaging PCB of 4Kx4K APS imager.

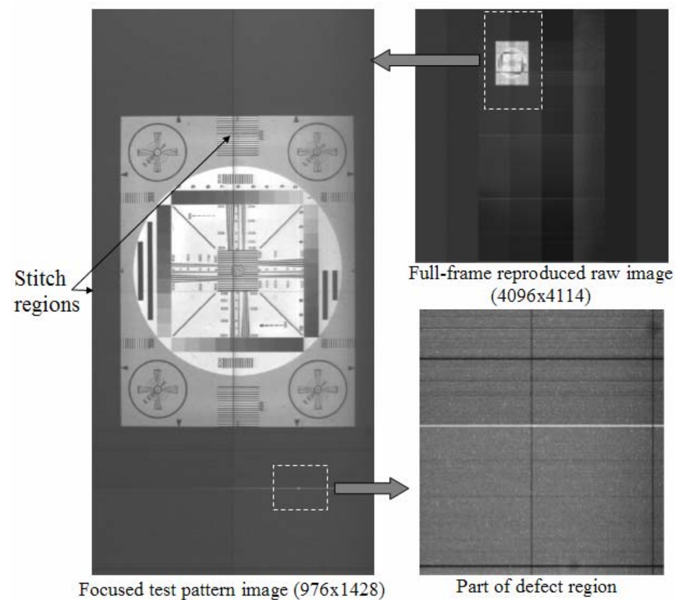

Fig.6. Reproduced raw image taken by the 4Kx4K imager.

Acknowledgment

This work was supported by U.S. NASA under an SBIR Phase-II contract. The authors would like to thank Leon Luo and Sandor Barna of Micron Technology, Inc. for their support of this work and Dr. Michael Lesser and his ITL team of the University of Arizona for packaging the device.

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Table 1. Measured characteristics of the 4Kx4K APS imager.

Process	0.5µm, 2P3M CMOS*	
Pixel Size	18µm x 18µm	
Pixel Type	3T, Hybrid PDPG APS	
Total Pixel	16,916,768 (4112x4114)	
Effective Pixels	16,850,944 (4096x4114)	
Pixel Array Dimensions	73.73 x 74.05	mm^2
Chip Die Dimensions	76.05 x 77.55	mm^2
Frame Rate	1.25	FPS
Conversion Gain	2.27 / 0.23	µV/e-
Pixel well-depth	1.35	Me-
Sensitivity	1.45 / 0.37	Volt/Lux-sec.
Quantum Efficieny	24**	% @ 390nm
	46**	% @ 550nm
Dark Current	57.4	mVolt/sec.
	25.3	e-/sec.
SNR (max)	61.3	dB
Read Noise	240	e-
Dynamic Range	75.0	dB
Supply Voltage	5.0	Volt
Power Consumption	550	mWatts

*:with stitching option, **:extrapolated