A 256 X 256 CMOS Active Pixel Image Sensor

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Abstract

A 256 X 256 CMOS photo-gate active pixel image sensor is presented. The image sensor uses four MOS transistors within each pixel to buffer the photo-signal, enhance sensitivity, and suppress noise. The pixel size is 20 μm X 20 μm and was implemented in a standard digital 0.9 μm single-polysilicon, double-metal, n-well CMOS process; leading to 25% fill-factor. Row and column decoders and counters are monolithically integrated as well as per column analog signal correlated double-sampling (CDS) processors, yielding a total chip size of approximately 4.5 mm X 5.0 mm. The image sensor features random accessibility and can be employed for electronic panning applications. It is powered from a single 5.0 V source.

At 5.0 V power supply, the video signal saturation level is approximately 1,200 mV with rms read-out noise level of approximately 300 μV, yielding a dynamic range of 72 dB (12 bits). The read-out sensitivity is approximately 6.75 μV per electron, indicating a read-out node capacitance of approximately 24 fF which is consistent with the extracted value. The measured dark current (at room temperature) is approximately 160 mV/s, equivalent to 3.3 nA/cm^2. The raw fixed pattern noise (exhibited as column-wise streaks) is approximately 20 mV (peak-to-peak) or approximately 1.67% of saturation level. At 15 frames per second, the power dissipation is approximately 75 mW.

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Introduction

The 256 X 256 CMOS active pixel image sensor has three main sections as shown in Fig. 1. The heart of the image sensor is a 256 X 256 array of picture elements (pixels). Within each pixel there are a photo-sensitive area and four active transistors to buffer the photo-signal, enhance sensitivity, and suppress noise.

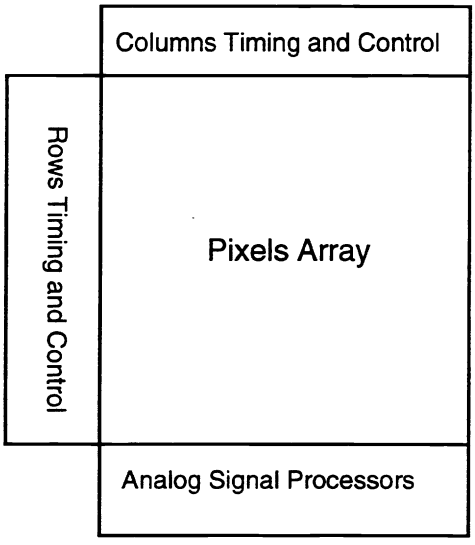

Fig. 1 Architecture of the 256 X 256 CMOS Active Pixel Image Sensor.

The 256 X 256 CMOS active pixel array is randomly accessible in a similar manner to that of a random-access memory (RAM). The accessibility of the pixel array is achieved via two decoders: a row (horizontal) decoder and a column (vertical) decoder. The row decoder is to address one row at a time while the column decoder is to address one column at a time. The column decoder sequentially addresses all the columns during the period their row is being addressed by the row decoder. The two decoders represent the

minimum required on-chip control and timing circuitry. Two on-chip counters are employed to interface the two decoders.

The photo-signal is processed by an on-chip analog signal chain of circuits. There is an analog signal processor for each column. The primary function of the on-chip analog circuitry is to perform correlated double-sampling (CDS), thus eliminating reset noise and suppressing 1/f noise. The output of the analog circuitry is a pair of analog signals. The first analog signal represents the photo-signal level while the second one represents the dark signal level. The analog video signal is the difference between these two signals.

Pixel Design and Operation

The 256 X 256 CMOS active pixel image sensor employs a single-polysilicon CMOS active pixel, thus allowing its implementation in a standard digital single-polysilicon CMOS process. The following two subsections details the design and operation of both the double-polysilicon and single-polysilicon CMOS active pixels.

Double-Polysilicon CMOS Active Pixel:

The double-polysilicon CMOS active pixel design is shown in Fig. 2 [1]. The double-polysilicon structure is to provide the fundamentally required electrical coupling between the semiconductor substrate surface regions under the photo-gate (PG) and the transfer gate (TG). The substrate surface potential under PG is controlled by the voltage applied to PG itself. Likewise, the substrate surface potential under TG is controlled by the voltage applied to TG itself. If the gap between PG and TG is not narrow enough, the substrate surface potential under this gap will constitute a barrier (electrical potential barrier) for the transfer of the charge signal from under PG to under TG, resulting in the failure of the signal read-out. The double-polysilicon structure permits the overlapping of PG and TG as each is on a different polysilicon level. Consequently, the gap between PG and TG is as narrow as the thickness of the silicon

dioxide layer between them, which is in the order of few tens nanometers. This very narrow gap and the coupling capacitance due to overlapping provide the required electrical coupling.

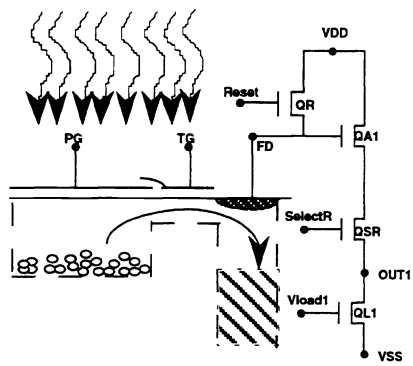

Fig. 2 Double-Polysilicon Active Pixel.

The operation of the double-polysilicon pixel has two phases. In the first phase, integration, the generated photo-charge carriers are collected under the photo-gate (PG) for a predetermined period (integration time). This is done by clocking PG to a high voltage level (approximately VDD). In this phase, the transfer gate, TG, is turned off.

In the second phase of operation, read-out, QR is pulsed on and off. This causes the potential of FD to float at a level approximately equal to VDD less the threshold voltage. Then, the bias of PG is changed to approximately VSS, causing the transfer of the charge signal into FD. This charge signal transfer causes the potential of FD to deviate from its approximately VDD value (reset level) to another value (signal level). This potential deviation (the difference between the reset and signal levels) is proportional to the incident light intensity and constitutes the video signal. A source-follower consisting of an active transistor (QA1) and a load transistor (QL1) is used to buffer the pixel FD node from the output node (OUT1) which is common (along with QL1) to a column of pixels within the image sensor pixel array. A select transistor (QSR) is used to select

the pixel (along with its common row of pixels) for read-out. In this phase, the transfer gate, TG, is turned on to allow the transfer of the signal charge from under PG into FD. However, it is turned off right after the completion of this transfer and before PG is clocked high for the following integration time, ensuring that none of the signal charge will transfer back to under PG causing image lag.

The transfer gate, TG, should be clocked on and off as described above for the optimum operation of the pixel. However, if TG is dc biased such that it is slightly conducting, the pixel operates satisfactorily. DC biasing the transfer gate makes the operation simpler by eliminating the need for one control clock and the associated driving circuitry, but it may cause some of the signal charge to transfer back to under PG, resulting in image lag. This effect is more pronounced at high signal levels.

It should be noted that active pixels can be either n-channel devices with electrons as the generated photo-charge carriers (charge signal) or p-channel devices with holes as the generated photo-charge carriers.

Single-Polysilicon CMOS Active Pixel:

If the above structure were to be fabricated using only one level of polysilicon, the gap between PG and TG would be in the order of a micron, too wide to provide the required electrical coupling. An active pixel design which employs only one level of polysilicon and provides the required electrical coupling is shown in Fig. 3. In this design, a transfer transistor (QT) replaces the transfer gate (TG). This is equivalent to introducing a diffusion region (called coupling diffusion) between PG and TG of the structure outlined in the previous section. This diffusion region functions as a conducting channel between the substrate surface under PG and the channel of the transfer transistor QT, thus providing the required electrical coupling.

The introduction of the coupling diffusion has the effect of increasing the kTC noise of the pixel. This effect can be minimized

by making the coupling diffusion capacitance as low as possible. This coupling diffusion capacitance can be made as low as few to several femto-Farads. This is equivalent to kTC noise in the order of few tens of electrons.

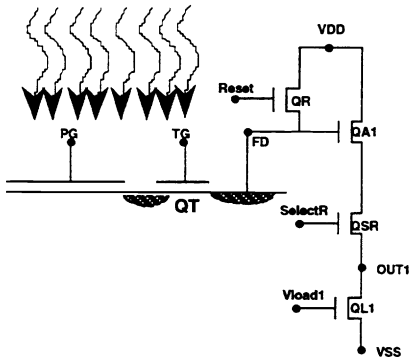

Fig. 3 Single-Polysilicon Active Pixel.

The single-polysilicon CMOS active pixel can be operated in a fashion similar to that of its double-polysilicon counterpart. For example, the transfer transistor, QT, can be turned on and off in a similar manner to that of the transfer gate, TG, for the optimum operation of the pixel. On the other hand, the transfer transistor can be dc biased such that it is slightly conducting, resulting in the trade-off between operation simplicity and image lag effect as described above.

On-Chip Timing and Control Circuitry

The 256 X 256 CMOS active pixel image sensor array is randomly accessible in a similar fashion to that of a random-access memory (RAM). The accessibility of the pixel array is achieved via two decoders; a row (horizontal) decoder and a column (vertical) decoder. The slow scan row decoder is to address one row at a time while the fast scan column decoder is to address one column at a time. The

column decoder sequentially addresses all the columns during the period their row is being addressed by the row decoder. Two on-chip counters are employed to interface the two decoders. Counters with load and clear control signals add the very significant functionality of random accessibility. In this mode of operation, instead of reading-out the whole image frame, a random window (sub-frame) can be read-out. The starting horizontal and vertical addresses of the window can be loaded into the counters in conjunction with the two load control signals. On the other hand, the horizontal and vertical dimensions of the window can be determined via the timing of the two clear control signals.

On-Chip Analog Signal Circuitry

The photo-signal is processed by an on-chip analog signal chain of circuits shown in Fig. 4 [2]. There is an analog signal processor for each column. The primary function of the on-chip analog circuitry is to buffer the pixel read-out node (FD) and perform correlated double-sampling (CDS). The first stage of this analog signal processor is the in-pixel source-follower. The in-pixel source-follower, which consists of an active transistor (QA1) and a load transistor (QL1), is used to buffer the pixel read-out node (FD) from the output node (OUT1) which is common (along with QL1) to a column of pixels within the image sensor pixel array. A select transistor (QSR) is used to select the pixel (along with its common row of pixels) for read-out. Thus, the pixel read-out node is local to its pixel and buffered from any other read-out nodes within the image sensor pixel array. Consequently, the capacitance of the read-out node is significantly reduced, resulting in significant improvements of read-out sensitivity and noise. For a 256 X 256 image sensor pixel array, the reduction in the capacitance of the read-out node is more than four orders of magnitude compared to that of a design where the read-out node is common for all pixels within the image sensor array, and more than two orders of magnitude compared to that of a design where the read-out node is common for all pixels within a row or a column of the image sensor

array [3]. A reduction of the read-out node capacitance results in an increase of the read-out sensitivity by the same amount and a reduction of the read-out kTC noise by the square root of this amount.

The second stage of the analog signal processor is a parallel pair of sample-and-hold circuits. The first sample-and-hold circuit handles the reset voltage level and consists of a sampling switch (QRS) and a holding capacitor (CRH). Similarly, the second sample-and-hold circuit handles the signal voltage level and consists of a sampling switch (QSS) and a holding capacitor (CSH). The third and final stage of the analog signal processor is a parallel pair of source-followers, each drives an output pad. The first source-follower handles the reset voltage level and consists of an active transistor (QA2) and a load transistor (QL2). Similarly, the second source-follower handles the signal voltage level and consists of an active transistor (QA3) and a load transistor (QL3). Two select transistors (QSCR and QSCS) are used to select the pixel, along with its common column of pixels.

The output of the analog circuitry is a pair of analog signals. The first analog signal (OUTR) represents the dark signal level while the second one (OUTS) represents the photo-signal level. The analog video signal is the difference between these two signals. This difference operation (OUTR-OUTS) is done off-chip. This approach eliminates kTC noise through CDS, as well as fixed pattern noise (FPN) due to pixel transistor offsets, and suppresses 1/f noise. However, it introduces additional kTC noise due to the two hold capacitors and FPN due to unmatched column source-follower transistors. This FPN can be suppressed via additional on-chip analog circuitry or off-chip signal subtraction techniques.

It should be noted that the physical layout of the analog signal processor shown in Fig. 4 is at the bottom of each of the columns of the pixel array. The only exception is the in-pixel active transistor (QA1), the row select transistor (QSR), and the reset transistor (QR). Each pixel in the array has its local active transistor (QA1), row select transistor (QSR), and reset transistor (QR).

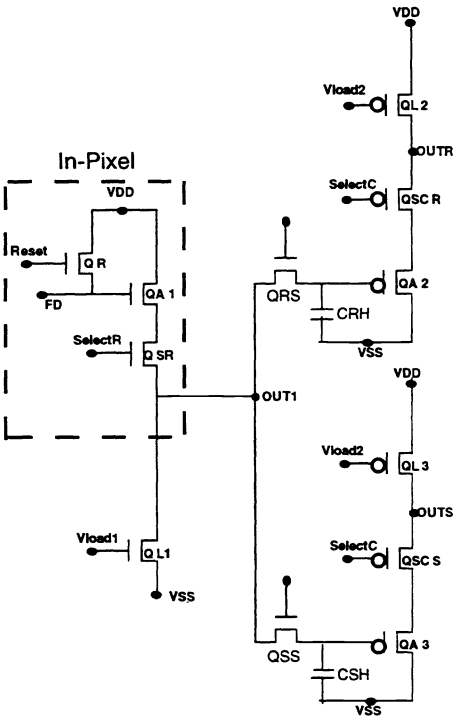

Fig. 4 On-Chip Analog Signal Processor.

Experimental Results

We have designed, fabricated, and tested the 256 X 256 CMOS active pixel image sensor. The pixel size is 20 μm X 20 μm. The chip was fabricated in a 0.9 μm, twin-tub (p-substrate), single-polysilicon, double-metal CMOS process. The resultant pixel fill-factor is approximately 25%. Two 8-input NAND decoders, with a 20 μm pitch, were used for row and column selection. Two monolithically integrated counters with load and clear control signals were employed to interface the two decoders. The analog signal processor, which was laid out at the bottom of the pixel array, has a 20 μm pitch as well. The output of the chip is a pair of analog

signals. The first analog signal represents the photo-signal level while the second one represents the dark signal level. The analog video signal is the difference between these two signals. This difference operation was done off-chip. The total size of the 44-I/O pad chip is approximately 4.5 mm X 5.0 mm.

The CMOS active pixel image sensor was successfully demonstrated. At 5.0 V power source, the image sensor exhibited a video signal saturation level of approximately 1,200 mV. The conversion gain (read-out sensitivity) was measured to be approximately 6.75 μV per electron. This corresponds to a read-out node capacitance of approximately 24 fF, which is in a very good agreement with the value extracted from physical design. The measured voltage signal saturation level and conversion gain yields a charge signal saturation level of approximately 215 thousand electrons per pixel. However, the pixel charge capacity is approximately 6 million electrons. This means that the signal saturation level is limited by the output source-follower(s) rather than by the pixel charge capacity. The measured rms read-out noise is approximately 300 μV (equivalent to approximately 44 electrons), which is in a very good agreement with the extracted value of the read-out node capacitance. The dynamic range, which is defined as the ratio of signal saturation level to rms read-out noise level, is approximately 72 dB. This is equivalent to 12 bits. The peak-to-peak fixed pattern noise was measured to be approximately 20 mV, or approximately 1.67% of saturation level. The dark signal (thermally generated signal) was measured to be approximately 160 mV per second at room temperature. At a pixel rate of approximately one million pixels per second (15 frames per second), the measured power dissipated in the chip is approximately 75 mW.

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