A 1.5-V 550-μW 176×144 Autonomous CMOS Active Pixel Image Sensor

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***Abstract*—This paper addresses the development of a micropower 176×144 CMOS active pixel image sensor that dissipates one to two orders of magnitude less power than current state-of-the-art CMOS image sensors. The chip operates from a 1.5-V voltage source and the power consumption measured for the chip running from an internal 25.2-MHz clock yielding 30 frames per second is about 550 μW. This amount enables the sensor to run from a watch battery. In order to achieve design goals, a low-power sensor design methodology is applied throughout the design process from system-level to process-level, while realizing the performance to satisfy the design specification. As an autonomous sensor, it can be operated with only three pads [GND, VDD (1.2–1.7 V), DATAOUT]. The die occupies 4 mm^2 of silicon.**

***Index Terms*—Active pixel image sensor, autonomous sensor, battery-operated devices, CMOS image sensors, image sensor, low-power, low-voltage, micropower, on-chip clock, system-on-a-chip.**

I. Introduction

LOW-POWER consumption is a fundamental demand for battery-operated devices [1]–[3], such as cellular phones, portable digital assistants (PDAs), and wireless security systems. Cellular videophones that emerge on the market will utilize state-of-the-art CMOS image sensors consuming 5–30 mW of power. The requirements of the next generation of portable devices to components are expected to be more stringent in terms of power and size.

This paper presents an image sensor which is a prototype of a future generation of micropower image sensors that consume less than 1 mW of power. This value is one to two orders of magnitude less than the power in current state-of-the-art CMOS image sensors. The chip is designed for 1.2–1.7-V operation, supposedly from one battery, and dissipates 550 μW.

This paper is organized as follows. Section II describes the image sensor architecture and analog and digital building blocks in this micropower CMOS active pixel image sensor. Section III summarizes a low-power sensor design methodology in this research. Section IV addresses the results of the sensor characterization and internal on-chip clock generation issues. Finally, the conclusions are presented in Section V.

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II. Sensor Chip Architecture

The image sensor's block diagram is shown in Fig. 1. The core pixel array consists of 176 (H) $\times$ 144 (V) photodiode active pixels [quarter common intermediate format (QCIF)] with a 5-μm pitch. The array of pixels is accessed in the row-wise fashion using a shift register and row driver with a reset bootstrapping circuit. All pixels in the row are read out into column analog readout circuits in parallel. Each of the 176 column-parallel readout circuits performs both sample-and-hold (S/H) and delta double sampling (DDS) functions [4], eliminating pixel offset variations and pixel source-follower $1/f$ noise. The signal is stored in the charge domain. The global charge-sensitive amplifier at the front end of the analog-to-digital converter (ADC) provides a fixed gain for the column charges being read using the column select logic. The amplifier reset and the amplifier signal values are sent to the 8-b self-calibrating successive approximation ADC. The ADC generates the 8-b digital output. The digital timing and control logic block generates the proper sequencing of the row address, column address, ADC timing, as well as generates the synchronization pulses for the pixel data going off-chip. The on-chip clock generator generates an internal clock with on-chip bandgap reference circuitry and power-on-reset circuit for the timing and control logic.

A. Signal Path From Pixel to ADC

A signal path from the pixel to the ADC is shown in Fig. 2.

A photodiode pixel is the sensing structure used for this micropower image sensor. Increasing the amplitude of the *rst* signal as $Vdd +$ threshold voltage using the bootstrap switch circuit adopted from [5] should increase the pixel reset voltage in order to extend the pixel dynamic range.

Our biasing Vln for each column's source-follower is 1.25 μA, permitting charging of the sampling capacitors in the allotted time. The source-followers can then be turned off by Vln_en. Once *row* and *sample_in* switches are selected, the photogenerated pixel signal value is stored in the column capacitors $C2$ clamped to an operational transconductance amplifier input voltage $V\mathrm{ref}$. After resetting the pixel, the pixel reset value is stored in the capacitor $C1$, and the difference between pixel reset and signal is stored in the capacitor $C2$. The overall input capacitance is $C_{\mathrm{in}} = C1C2/(C1 + C2)$. The charge difference between the pixel reset and signal is transferred to the operational amplifier by turning on the *col* switch.

Fig. 3 shows the relative timing for row and column operation of the sensor. At 30 frames/s, the sensor is clocked from

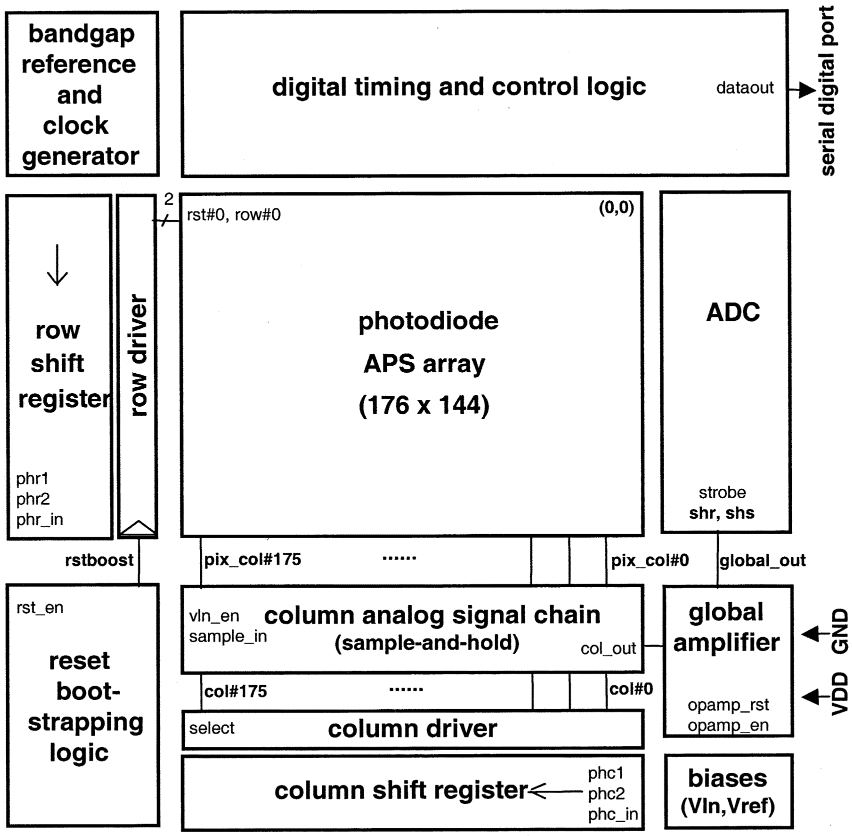

Fig. 1. Sensor's block diagram.

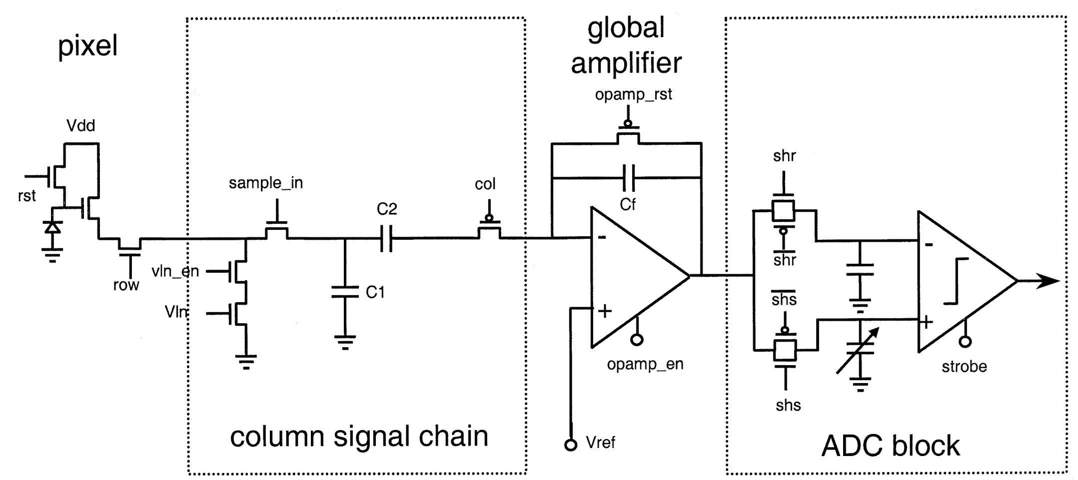

Fig. 2. Pixel to ADC signal path.

a 25.2-MHz source. The total row time at this frame rate is 231.1 μs [$(192 + 176 \times 32)$ clocks]. This period is divided between the time required for column analog operations (192 clocks) and the ADC conversion time (32 clocks). The analog readout sequence starts with the selection of a pixel row, whose output is sampled onto the column S/H capacitor in parallel. Each ADC processing time is the global S/H (16 clocks) and the ADC conversion (16 clocks). At the full 30-Hz frame rate, the ADC used in this sensor needs to operate at 0.75 Msamples/s.

B. Operational Transconductance Amplifier

The major problem in the realization of micropower operational amplifiers is obtaining a reasonable speed and an acceptable dynamic range. A key factor for power reduction is the avoidance of any compensation capacitor other than the load itself, which is only possible if the major part of the voltage gain is achieved at the output node, that is, by using a single-stage operational transconductance amplifier (OTA) [6]. The

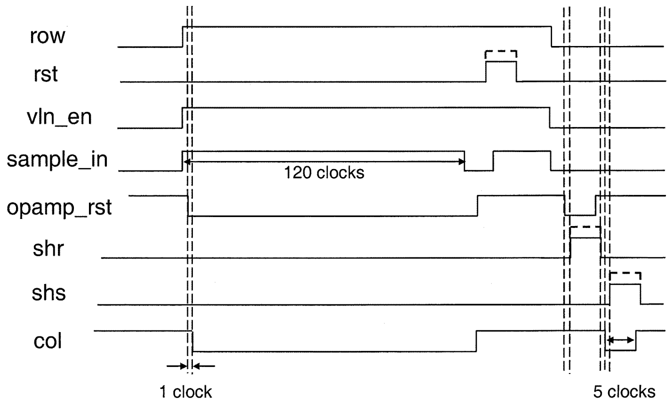

Fig. 3. Relative row and column timing.

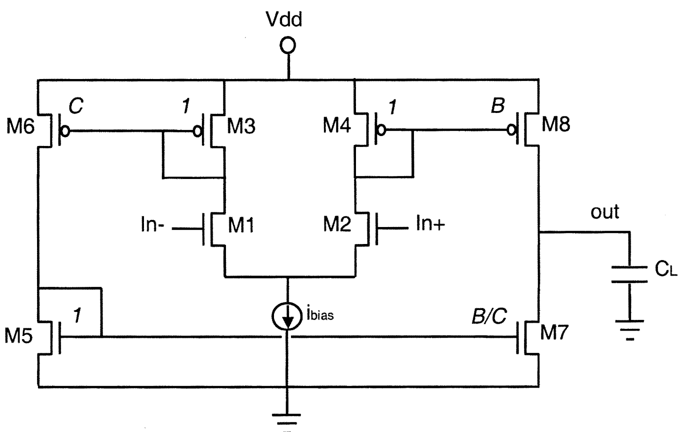

Fig. 4. Low-voltage operational transconductance amplifier.

OTA used is shown in Fig. 4. Assuming a ratio B of the mirror $M4$–$M8$, the overall transconductance of the amplifier is

$$g_m = Bg_{m1(2)}. \tag{1}$$

The circuit, loaded by C_L, behaves essentially as an integrator with a time constant

$$\tau_u = \frac{C_L}{g_m} \tag{2}$$

which is the inverse of the unity gain frequency f_u.

The very low frequency $1/\tau_d$ of the dominant pole depends directly on the dc gain A_{dc}. Also, the slew rate is Bi_{bias}/C_L. The key performance parameters of the opamp with a load C_L of 4.3 pF are summarized in Table I.

C. The 8-B Successive Approximation ADC

The low-power 8-b successive approximation ADC [7] is shown in Fig. 5. The ADC consists of a capacitor bank, a comparator, decision latches, and correction latches.

The calibration portion of the ADC serves to eliminate the dynamic comparator offset, which is typically 30 mV, by sampling the same amplifier reset voltage $V\text{ref}$ on both input capacitors of the comparator. It has one sign capacitor bit (2^4C) and five binary-scaled capacitor bit cells. This ADC is calibrated at the beginning of the very first frame for compensating the dc offset at the input of the comparator.

TABLE I
SIMULATED PERFORMANCE OF THE LOW-VOLTAGE OTA

A_{dc}	> 40 dB
PM	80°
GBW	10 MHz
Slew Rate	5.7 V/μs

The main ADC conversion uses eight binary-scaled capacitors to sample the amplifier signal and reset capacitor to store the amplifier reset voltage. These capacitor networks are connected to the input of the comparator. After saving these signal and reset voltages on the top plate of the capacitors, the bottom plates are successively connected to V_{dd}.

The comparator output determines whether or not the signal side maintains the updated signal in the top plate. During the convergence process, the variable signal is matched to a fixed amplifier reset voltage $V\text{ref}$. Not only does this allow the use of a limited input swing comparator, but it causes the comparison to happen at the same level each time, eliminating the potential comparator offset versus signal dependence.

In the current implementation, the power supply voltage V_{dd} as the ADC reference voltage $V\text{ref}_{\text{adc}}$ and PMOS switches to connect this voltage are used. Generally ADC reference voltage is provided from off-chip through pad or on-chip reference circuit. Because of the 3-pin configuration, on-chip ADC reference voltage generation is required; however, $V\text{ref}_{\text{adc}}$ generation takes the big portion of total power consumption. Because of that, power supply Vdd is used to create $V\text{ref}_{\text{adc}}$ using the additional capacitor (2^7C). In Fig. 4, LSB (least significant bit) voltage V_{LSB} and the ADC reference voltage $Vref_{\text{adc}}$ can be expressed by

$$V_{\text{LSB}} = Vdd\left(\frac{C}{C_{\text{tot}}}\right) = \frac{1.5}{430} = 3.5 \text{ mV} \tag{3}$$

$$V\text{ref}_{\text{adc}} = Vdd\left(\frac{C_{\text{conv}}}{C_{\text{tot}}}\right) = 1.5\left(\frac{255}{430}\right) = 0.89 \text{ V} \tag{4}$$

where $C_{\text{tot}} = (2^N - 1 + 2^{N-4} + 2^{N-3} - 1 + 2^{N-1})C$, $C_{\text{conv}} = (2^N - 1)C$, $N = 8$, and $Vdd = 1.5$ V, respectively.

D. On-Chip Clock Generator

The three-stage ring oscillator as an on-chip clock generator is used as shown in Fig. 6(a). The stable clock power *Vclock* is required to stabilize the clock frequency over process, voltage, and temperature variations. The bandgap reference is one of the most popular reference voltage generators that achieve the requirement [8]. In Fig. 6(a), the clock power *Vclock* comes from on-chip bandgap reference circuitry. The output voltage $V\text{ref}_{\text{conv}}$ of the conventional bandgap reference is 1.25 V. This fixed output voltage of 1.25 V limits the low-voltage operation. In [9], a bandgap reference that can successfully operate with a sub-1-V supply is presented. Fig. 6(b) shows the low-voltage bandgap reference circuit with the decoupling capacitors $C1$ and $C2$. The output voltage of this low-voltage bandgap reference circuit becomes

$$V\text{ref}_{\text{low\_voltage}} = \text{R4}\left(\frac{\text{Vf1}}{\text{R2}} + \frac{\text{dVf}}{\text{R3}}\right) = \frac{\text{R4}}{\text{R2}}\text{Vref}_{\text{conv}} \tag{5}$$

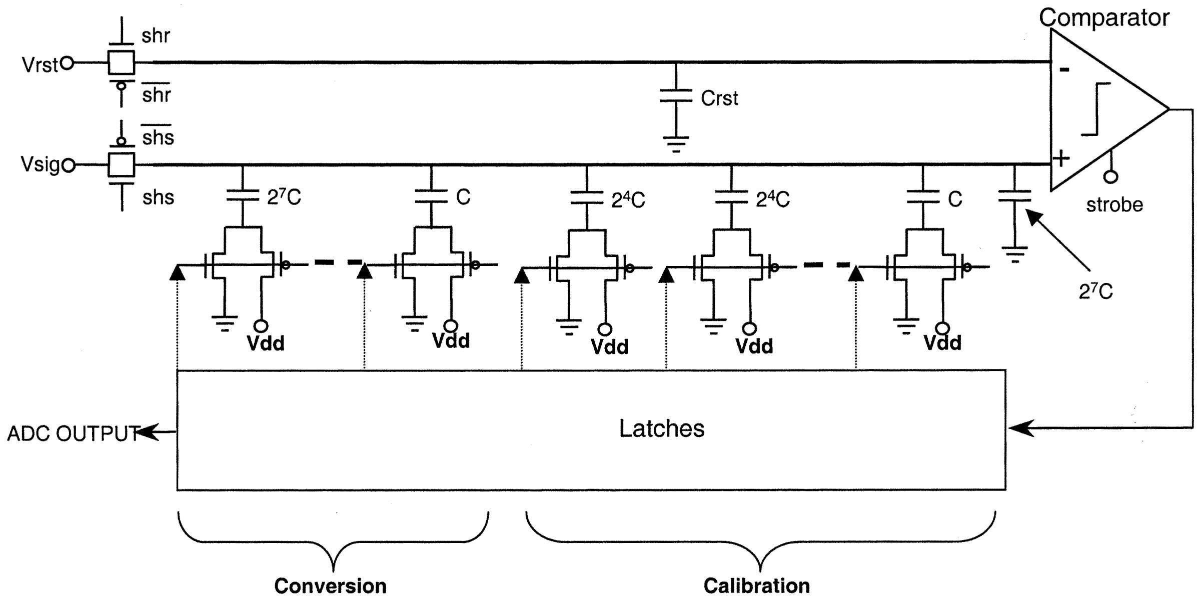

Fig. 5. Low-power 8-b successive approximation ADC.

where $Vf1$ is the built-in voltage of the diode and dVf is the forward voltage difference between on diode $D1$ and N diodes $D2$ with proportional to the thermal voltage, respectively.

Therefore, $V\mathrm{ref}_{\mathrm{low\_voltage}}$ as *Vclock* can be freely changed from $V\mathrm{ref}_{\mathrm{conv}}$ and Vdd can be lowered below 1 V if the amplifier is properly working. Unlike using the native NMOS transistors [9], the simple differential amplifier is used, therefore the minimum supply voltage value is imposed by the differential pair of the input stage, and is equal to a threshold voltage plus two overdrive voltages (V_{ds}). For the 0.35-μm CMOS process used, this value turns out to be around 1 V.

The signals *rst* and *rstb* are generated by the power-on-reset circuit as shown in Fig. 6(c). A power-on-reset circuit provides the stable generation of a reset signal without being affected by the rising characteristic of a power-supply voltage. This power-on-reset circuit includes two MOSFETs ($M1$ and $M2$), a capacitance (C), and two inverters. In the power-on-reset circuit, $M1$ is acted as the resistance R with a large threshold voltage and $M2$ is a pull-down switch, and the reset signal is determined by the difference of threshold voltages between $M1$ and $M4$ in the first inverter and the *RC* constant of $M1$ and C.

III. Low-Power Sensor Design Methodology

Low-power sensor design methodology is considered at all levels—technology, circuit and logic, architecture, algorithm, and system integration. Fig. 7 summarizes low-power design steps from process technology to system integration in this research.

For power reduction through process technology, generally digital circuitry can benefit most from the next-generation technology such as area, speed, and power performance [1], [10]. From the scaling laws, the most advanced technology is good for low-power consumption. However, CMOS image sensors are more performance sensitive than digital circuitry, thus they require a stable, well-characterized technology. From this point of view, a 0.35-μm CMOS technology as the preferred design technology for this research is chosen.

For power reduction through circuit/logic design, the reduction of the power supply voltage can be a key element in low-power CMOS image sensors. However, the design of a low voltage CMOS sensor involves several well-known challenges such as: 1) the reduced dynamic range of pixel; 2) the low-voltage MOS switch problem; 3) low-voltage opamp and ADC design; and 4) low-power internal bias generation. The challenges discussed above are addressed in the following way.

1) The pixel voltage dynamic range is increased by using a bootstrapped reset pulse.
2) The column analog readout circuit is designed so that only unipolar MOS switches are required. For instance, the S/H switch is of an n-type and is good for sampling pixel signals that are always "low." While the column select switch is of a p-type, which is good at connecting high level signals, such as for the reference voltage, etc.
3) The charge mode readout fixes the readout bus voltage so that the requirements on the amplifier input voltage swing are relaxed. On the other hand, an inverting current-mirror OTA used in this design yields almost rail-to-rail output and a capacitive ADC is selected to avoid some low-voltage design problems that would be faced with different types of ADC such as flash, pipelining, or folding converter.
4) Column readout circuits receive the reference voltage from the readout opamp, eliminating the need for a power consuming reference voltage generator. In this case, the reference voltage is loaded only onto the high impedance opamp input, so the $Vref$ voltage source can be implemented as a high-resistance one.

In addition, the following measures have been undertaken to reduce the sensor power. First, unused blocks such as the pixel

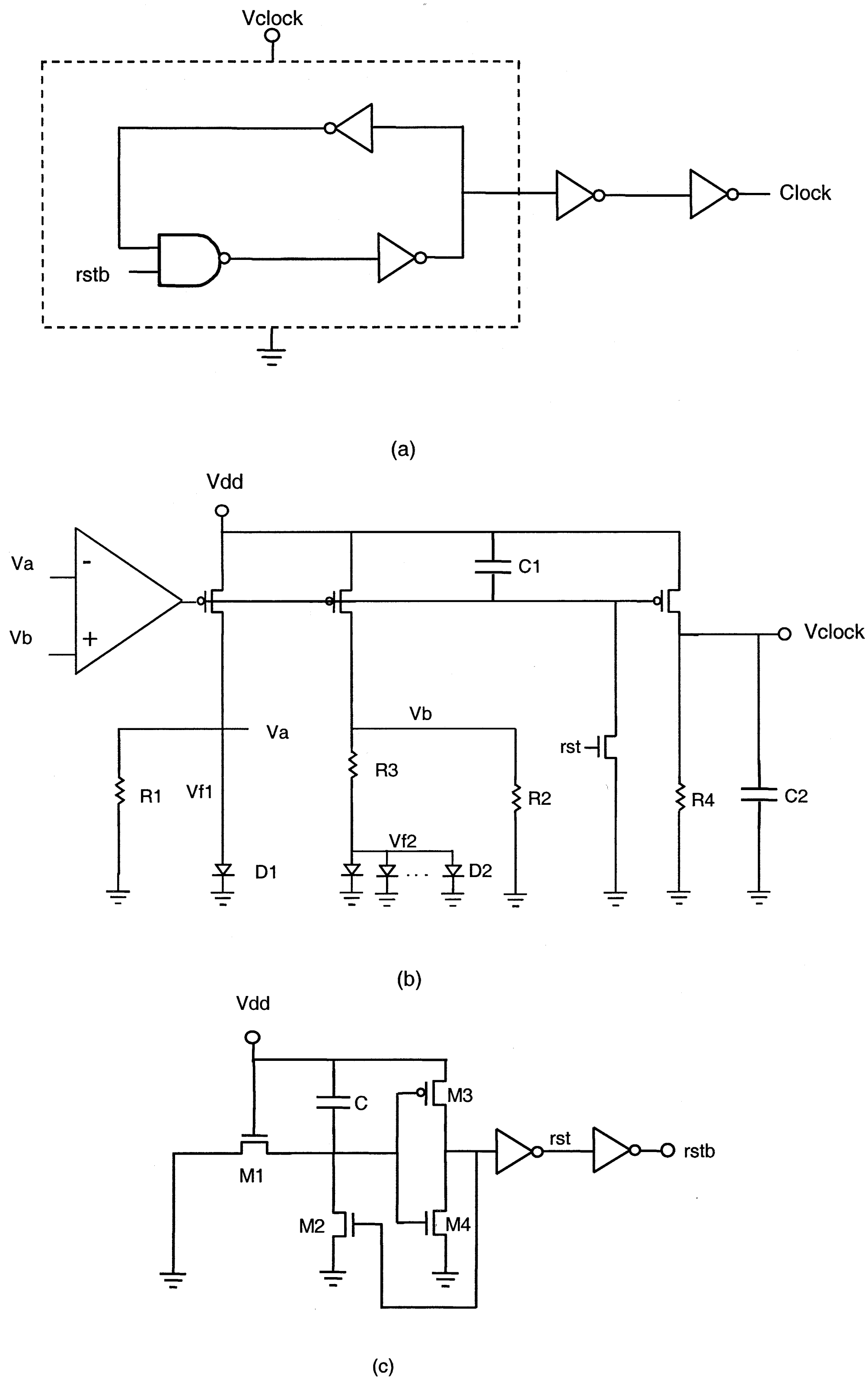

Fig. 6. On-chip clock generator. (a) Three-stage ring oscillator. (b) Low-voltage on-chip bandgap reference circuitry. (c) Power-on-reset circuit.

current load Vln in the column circuit, the opamp in the analog signal chain, and the comparator in the ADC have been cut from power for the time they do not operate. Second, the column S/H circuit does not have an active buffer. It was replaced with a passive capacitor storage.

For power reduction through architectural design, the power consumption can be further reduced by minimizing the chip function and the number of blocks. Also, we divide the chip architecture partition with selectively enabled blocks. For reducing the operation for decoding and execution, the shift

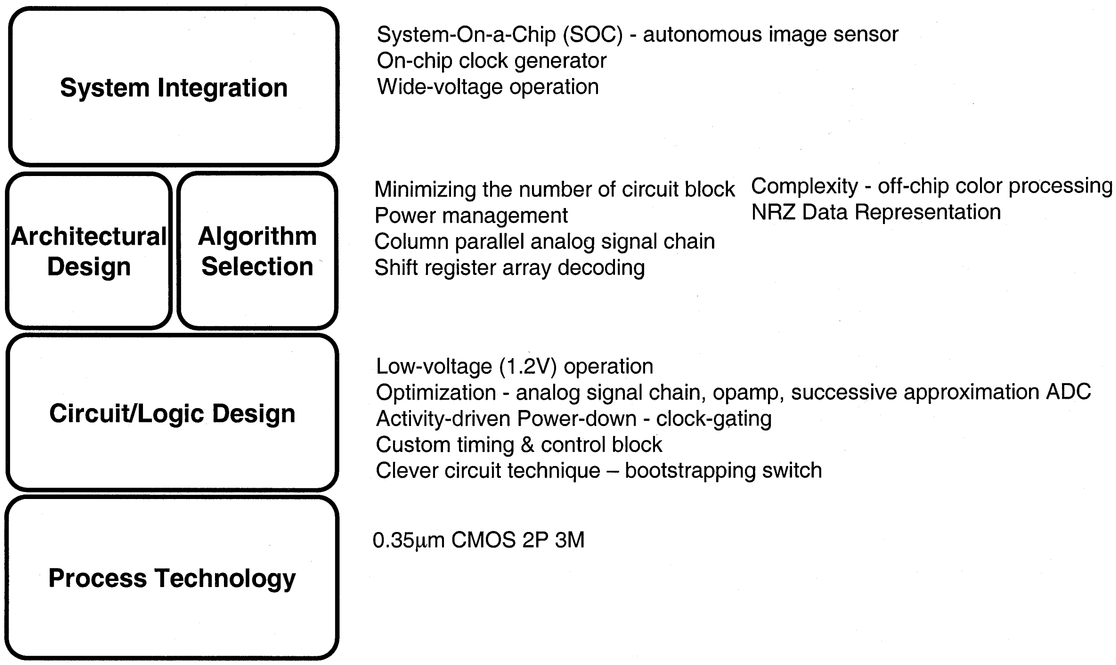

Fig. 7. Low-power sensor design steps in this research.

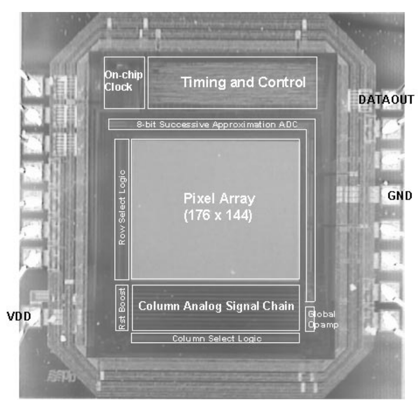

Fig. 8. Image sensor chip microphotograph.

register array type is chosen. Although window and random access functions are sacrificed, which are not necessary in a small-format image sensor, shift register array type reduces the number of global buses.

For power reduction through algorithm selection, the operation and the number of hardware resources can be minimized [11]. On-chip color processing can not be considered, which tends to be very compute-intensive and power-hungry. The nonreturn-to-zero (NRZ) representations [12] that reduce the bandwidth needed to send the pulse-code modulation (PCM) code is chosen.

For power reduction through system integration, the overall system pin requirements by combining functionality into system-on-a-chip (SOC) can be reduced [13]. By integrating the master clock generator and other ICs such as digital and analog peripherals, the image sensor can be operated with only three pads which are GND, VDD, and DATAOUT. At the system level, off-chip buses have capacitance C that is orders

TABLE II
SPECIFICATION AND MEASURED SENSOR PERFORMANCE AT A 1.5-V AND 5 FRAMES/S

Technology	0.35 µm, 2 P, 3 M CMOS
Pixel array size	176(H) x 144(V) (QCIF)
Pixel size and type	5 µm x 5 µm Photodiode APS
Pixel fill factor	30 %
Chip size	2 mm x 2 mm
Sensor output	8-bit serial digital
On-chip ADC	8-bit single successive approximation
ADC DNL/INL	1 LSB / 2 LSB
Conversion gain (pixel PD-referred)	34 µV/e-
ADC conversion gain	3.5 mV/LSB
Dark signal	6.97 LSB/sec or 24.4 mV/sec or 718 e-/sec
Saturation (pixel PD-referred)	253.2 LSB or 886.2 mV or 26,065 e-
Noise	0.85 LSB or 3.0 mV or 88 e- r.m.s.
Operating voltage	1.2 – 3.6 V
Maximum frame rate	40 fps
Maximum pixel readout rate	1 Mpix/sec
Power consumption	550 µW at 1.5 V, 30 fps

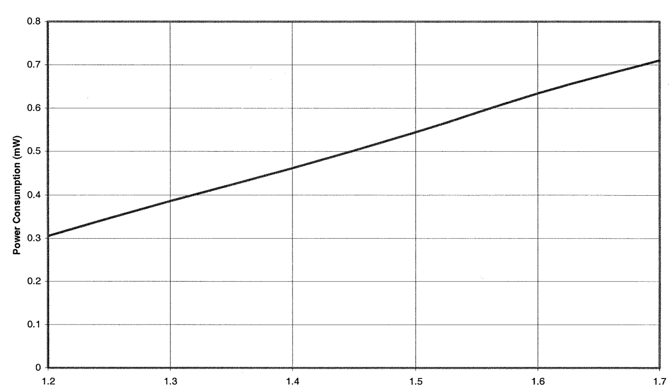

Fig. 9. Measured power consumption at 30 frames/s from 1.2 to 1.7 V with a 25.2-MHz on-chip clock.

TABLE III
ESTIMATED CHIP POWER PORTFOLIO WITH 30 FRAMES/S AT A 1.5-V POWER SUPPLY

Main components	Current (μA)	Quantity	Average current (μA)	Peak current (μA)
Column analog signal chain (vln)	1.25	176 x (1/50)^	4.4	220
Global opamp	30	1 x (1/2)^	15	30
ADC (comparator)	16	1 x (1/4)^	4	16
Biases (Vln + Vref)	16	1	16	16
Peripheral (row & col logic + rst bootstrapping circuit + drivers)	20	1	20	300
Clock generator	75	1	75	200
Timing and control	170	1	170	6200
Dataout	60	1	60	3200
Total Average Current (μA)		364.4		
Total Peak Current (μA)		10182		
Total Average Power (V x I) (μW)		1.5 x 364.4 = 546.6		
^ duty cycle factor				

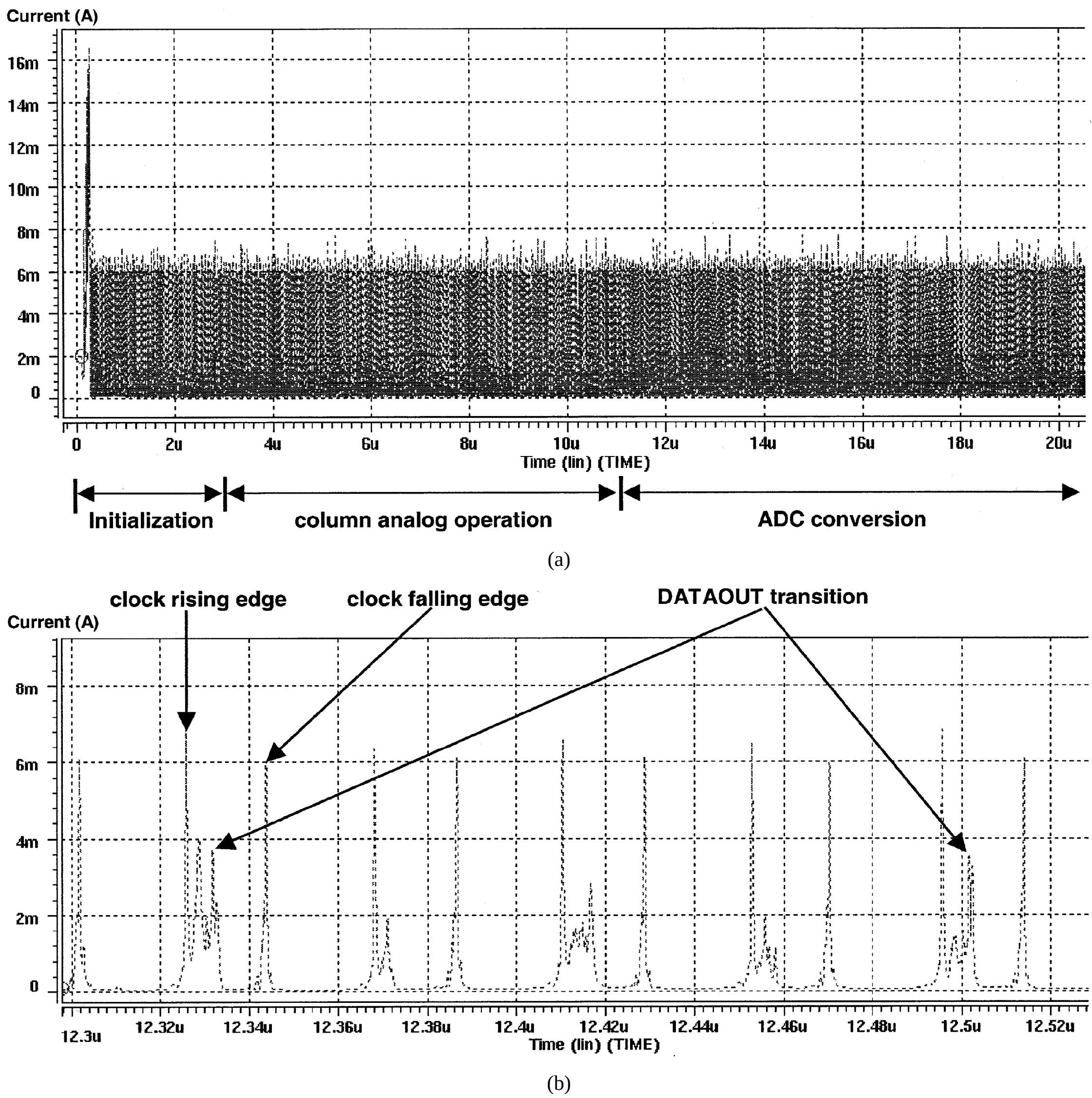

Fig. 10. Peak current from the chip-level HSPICE simulation at 1.5 V and 30 frames/s with on-chip 25.2-MHz clock. (a) Peak current profile. (b) Zoom in on ADC conversion.

of magnitude greater than those found on signal lines internal to a chip. Therefore, transitions on these buses result in considerable system power dissipation. Also, the system can be operated without a voltage regulator, there will be greater savings, but then a more variable supply voltage must be tolerated. This sensor can be operated in a wide voltage range (1.2–3.6 V).

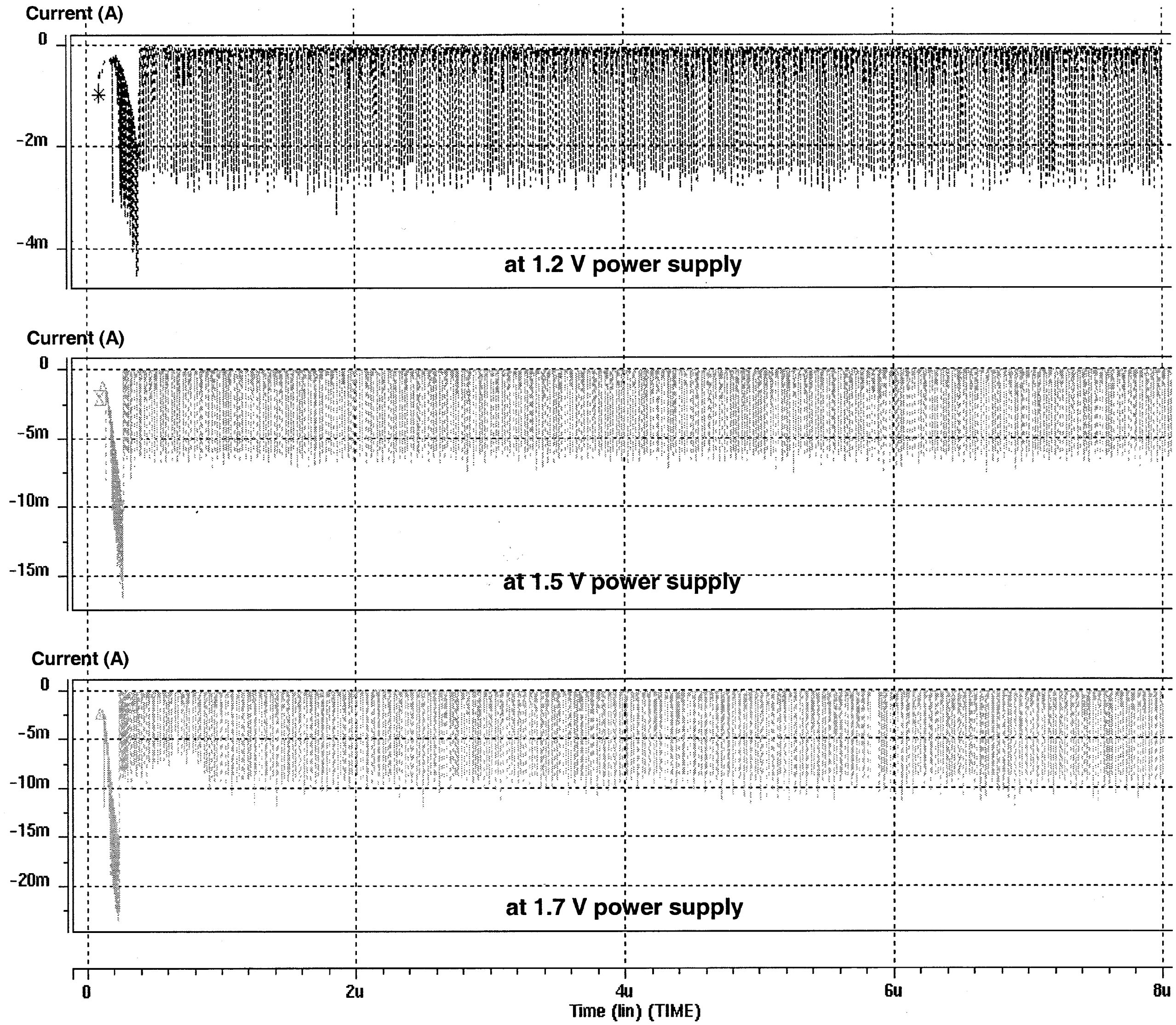

Fig. 11. Peak current at different power supplies of 1.2, 1.5, and 1.7 V.

IV. Test Results

The sensor is implemented in a 0.35-μm, 2P, 3M 3.3-V CMOS process with $Vtn = 0.65$ V and $Vtp = -0.85$ V. The micrograph of the image sensor is shown in Fig. 8. The size of the chip is about 2 mm $\times$ 2 mm, which includes the pixel array, row/column logic, analog readout, ADC, biases, on-chip clock generator, timing and control block, and 16 pads including test pins. This chip is packaged by 28-pin ceramic leadless chip carrier (CLCC).

The chip can be operated autonomously with only three pads [GND, VDD (1.2–1.7 V), DATAOUT]. Also, with an external master clock, the chip can be operated on a 1.2–3.6-V power supply. Table II summarizes the sensor chip characteristics at 5 frames/s and 1.5-V power supply with the external 4.125-MHz clock.

A. Power Consumption

The measured power consumption of the overall chip, which includes the pixel array, row/column logic, analog readout, ADC, biases, timing and control block, on-chip clock generator, and pads, is shown in Fig. 9 with the internal 25.2-MHz on-chip clock (30 frames/s) from a 1.2-1.7-V power supply. At 1.5 V, the measured average power consumption is about 550 μW.

The estimated overall chip power consumption is 546.6 μW at 1.5 V and 30 frames/s with the internal 25.2-MHz clock as shown in Table III. Note that, first, the timing and control block consumes about 1/2 of total average current and 3/5 of total peak current. Second, the serial digital output port DATAOUT consumes about 1/3 of total peak current.

Fig. 10 shows less than 8 mA of peak current from the chip-level HSPICE simulation at 1.5 V and 30 frames/s with the internal 25.2-MHz clock. To reduce the peak current, DATAOUT transition is designed to happen in about 1/4 clock period after the rising edge of the master clock of the timing and control block as shown in Fig. 10(b). Also, Fig. 11 shows the peak current at different power supply voltages. At a 1.2-V power supply, the peak current can be about 3 mA according to the HSPICE simulation result. As expected, the peak current is proportional to Vdd^2.

The measured power consumption of the overall chip is shown in Fig. 12 with the external 16.5-MHz clock (20

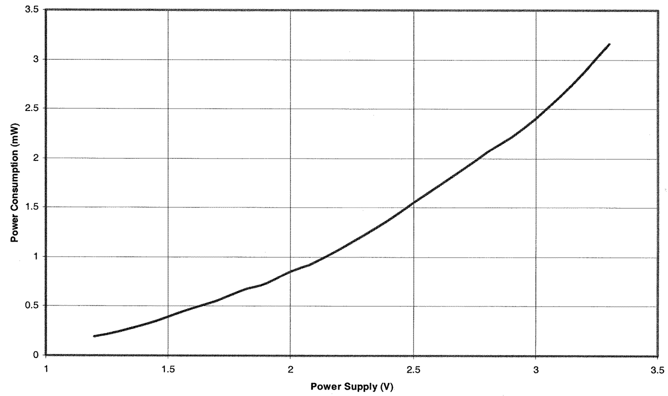

Fig. 12. Measured power consumption with the external 16.5-MHz clock (20 frames/s) from a 1.2–3.3-V power supply.

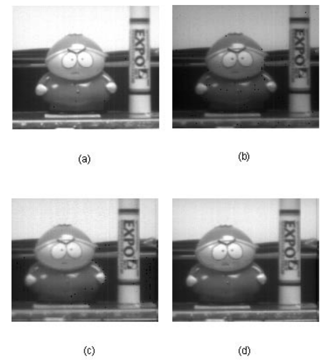

Fig. 14. Test images. (a) Twenty frames/s at 1.5 V with the external 16.5-MHz external clock. (b) Forty frames/s at 1.5 V with the external 33-MHz clock. (c) Thirty frames/s at 1.5 V with the internal 25.2 MHz clock. (d) Thirty frames/s at 1.7 V with the internal 25.2-MHz clock.

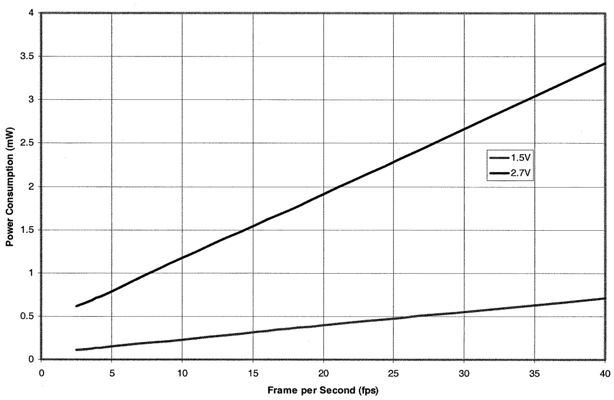

Fig. 13. Measured power consumption at 1.5-V and 2.7-V power supplies for different frame rates.

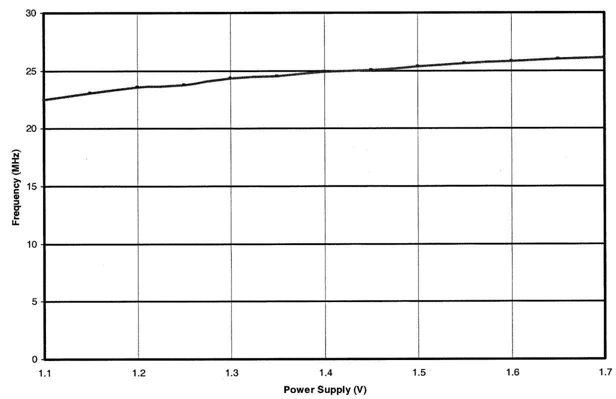

Fig. 15. Measured frequency response of on-chip clock generator.

frames/s) from a 1.2–3.3-V power supply. As expected, the power consumption is proportional to Vdd^2.

Fig. 13 shows the measured power consumption of the overall chip at 1.5-V and 2.7-V power supplies for different frame rates. As expected, the power consumption is proportional to the frame rate.

B. Test Images

Images taken with the sensor at 20 and 40 frames/s with a 1.5-V power supply and the external clock are shown in Fig. 14(a) and (b). Also, images taken with the sensor at 30 frames/s (25.2 MHz on-chip block) with 1.5-V and 1.7–V power supplies are shown in Fig. 14(c) and (d).

C. Clock Stability

The measurement result of the three-stage ring oscillator with clock power *Vclock* from the on-chip low-voltage bandgap reference circuitry is shown in Fig. 15. The on-chip low-voltage bandgap reference circuitry generates 0.9 V as *Vclock* from a 1.1–1.7-V power supply. The measured clock frequency shows from 22.5 MHz to 26 MHz with respect from 1.1 to 1.7 V, which corresponds to a less than 15% variation. This means that the bandgap reference circuitry generates less than a 5-mV variation from 0.9 V, which is less than 1% variation.

V. Conclusion

An active pixel image sensor designed for 1.2–1.7-V operation with an on-chip clock generator and 1.2–3.6-V operation with an external clock to provide 176 (H) $\times$ 144 (V) QCIF 8-b monochrome video is presented. As an autonomous sensor, it can be operated with only three pads [GND, VDD (1.2–1.7 V), DATAOUT]. The measured power consumption of the overall chip with the internal 25.2-MHz on-chip clock (30 frames/s) at a 1.5– V power supply is about 550 μW. Low-power, low-voltage image sensor techniques have been successfully tried and the possibility has been shown of wide voltage-range operation (1.2–3.6 V).

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