MP 6.7 A 1.2V Micropower CMOS Active Pixel Image Sensor for Portable Applications

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Low-power image sensors are desirable for portable applications, including cellular phones, portable digital assistants (PDAs), and wireless security systems. Scaled CMOS technology has bright prospects for both high performance and low power image sensor systems [1]. This image sensor for 1.2V operation dissipates one-to-two orders of magnitude less power than the current state of the art CMOS active pixel sensors.

The sensor block diagram is shown in Figure 6.7.1. The core pixel array consists of 176(H)x144(V) (QCIF) photodiode active pixels with a 5μm pitch. The array of pixels is accessed in the standard row-wise fashion using a shift register and row driver with a reset bootstrapping circuit, so that all pixels in the row are read out into column analog readout circuits in parallel. Each of the 176 column-parallel readout circuits performs both sample-and-hold (S/H) and delta double sampling (DDS) functions, eliminating pixel offset variations and pixel source-follower 1/f noise. The signal is stored in the charge domain. The global charge-sensitive amplifier at the front end of the ADC provides fixed gain for the column charges being read using the column select logic. The amplifier reset and the amplifier signal values are sent to the 8b self-calibrating successive approximation ADC.

A simplified signal path from pixel to ADC is shown in Figure 6.7.2. The design of a low voltage CMOS sensor involves several challenges such as a) reduced circuit dynamic range, b) the low voltage MOS switch problem, c) low-voltage opamp and ADC design, and d) low-power internal bias generation. The challenges discussed above are addressed in the following way: a) the pixel voltage dynamic range is increased by using a bootstrapped reset pulse; b) the column analog readout circuit requires only unipolar MOS switches. For instance, the S/H switch is of an n-type and is good for sampling pixel signals that are always "low". While the column select switch is of a p-type, which is good at connecting high-level signals, such as for the reference voltage, etc.; c) the charge mode readout fixes the readout bus voltage so that the requirements on the amplifier input voltage swing are relaxed. On the other hand, a current-mirror OTA used in this design yields almost rail-to-rail output; and d) a capacitive ADC avoids low-voltage design problems that would be faced with different types of ADC such as flash, pipelining, or folding converter.

The low-power 8b successive approximation ADC shown in Figure 6.7.3 consists of a capacitor bank, a comparator, decision latches, and correction latches. In this implementation rail supply Vdd is used as the ADC reference voltage and pMOS switches to connect this voltage. The calibration portion of the ADC eliminates dynamic comparator offset, which is typically 30mV. It has 5 capacitor bit cells. The main ADC conversion uses 8 binary-scaled capacitors to sample the amplifier signal and reset capacitor to store the amplifier reset voltage. These capacitor networks are connected to the input of the comparator. After saving these signal and reset voltages on the top plate of the capacitors, the bottom plates are successively connected to Vdd. The comparator output determines whether or not the signal side maintains the updated signal in the top plate. For low voltage operation of this kind of ADC, it is usually essential to have a wide input voltage swing comparator. This approach eliminates the need for such a comparator. During the convergence process, the variable signal is matched to a fixed amplifier reset voltage. This not only allows use of a limited input swing comparator, but also causes comparison to occur at the same level each time, eliminating potential comparator offset vs. signal dependence.

In addition, the following measures reduce sensor power. First, unused blocks such as the pixel current load in the column circuit, and the comparator and opamp in the ADC are cut from power when not operating. Second, column readout circuits receive the reference voltage from the readout opamp, eliminating a power-consuming reference voltage generator. In this case, the reference voltage is loaded only onto the high-impedance opamp input, so the Vref voltage source can be implemented as a high-resistance one. Third, the column S/H circuit does not have an active buffer. It is replaced by passive capacitor storage.

Figure 6.7.4 shows relative timing for row and column operation. At 20frames/s, the sensor is clocked from a 16.5MHz source. Total row time at this frame rate is 352.96μs ((192 + 176 x 32) clocks). This period is divided between time required for column analog operations (192 clocks) and ADC conversion (32 clocks). The analog sequence starts with selection of a pixel row, whose output is sampled onto the column S/H capacitor in parallel. Each ADC processing time is the global S/H (16 clocks) and ADC conversion (16 clocks). At full 20Hz frame rate, the ADC used in this sensor operates at 500kSample/s. The ADC is calibrated at the beginning of the first frame to compensate the comparator input.

The sensor is implemented in a 0.35μm, 2P, 3M 3.3V CMOS with Vtn=0.65V and Vtp =-0.85V. Figure 6.7.5 summarizes sensor chip characteristics at 6.5frames/s and 1.2V supply. Measured ADC differential nonlinearity (DNL) is 1LSB and integral nonlinearity (INL) is 2LSB. The sensor core, which includes the pixel array, row/column logic, analog readout, ADC, and biases, dissipates 48μW at 20 frames/s. Although the goal is an autonomous sensor with 3 pads (GND, VDD (1.0-1.7V), DOUT), the current sensor implementation includes some externally controlled input pins such as a master clock and ADC controls. To simplify communication with the sensor, I/O pads perform 3.3V -> 1.2V and 1.2V -> 3.3V conversion. Because of driving external loads at 3.3V, the overall power consumption is approximately 1mW. Images taken with the sensor at different power supply voltages are shown in Figure 6.7.6. A micrograph of the image sensor core is shown in Figure 6.7.7.

Reference:

[1] Fossum, E. R., "CMOS Image sensors: Electronic Camera on a Chip," *IEDM Tech. Dig*, pp. 17-25, Dec. 1995.

Technology	0.35μm, 2P, 3M CMOS
Pixel array size	176(H) x 144(V) (QCIF)
Scanning	Progressive
Pixel size	5 μm x 5 μm
Pixel type	Photodiode APS
Pixel fill factor	30 %
Sensor core size	1.2 mm x 1.2 mm
On-chip ADC	8-bit single successive approximation
ADC DNL/INL	1 LSB / 2 LSB
Frame rate	20 fps
Pixel readout rate	0.5 Mpix/sec
Conversion gain (pixel PD-referred)	20 μV/e-
ADC conversion gain	2.8 mV/LSB
Dark signal	4.64 LSB/sec or 13 mV/sec or 650 e-/sec
Saturation (pixel PD-referred)	214.3 LSB or 600 mV or 30,000 e-
Noise	0.43 LSB or 1.2 mV or 60 e- r.m.s.
Operating voltage	1.0 – 3.6 V
Sensor output	8-bit parallel digital
Power consumption	48 μW at 1.2 V, 20 frames/sec w/o pad power

Figure 6.7.5: Measured sensor performance.

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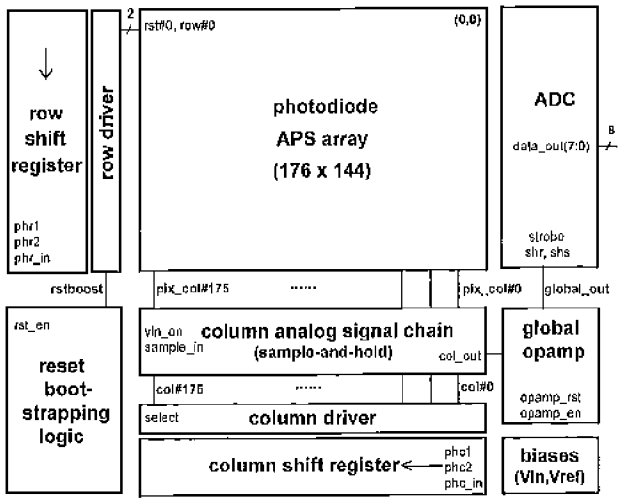

Figure 6.7.1: CMOS image sensor block diagram.

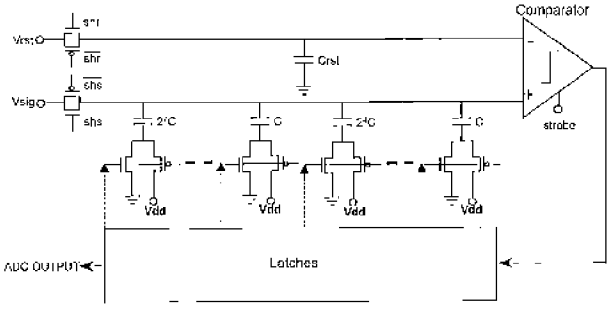

Figure 6.7.3: 8b successive approximation ADC architecture.

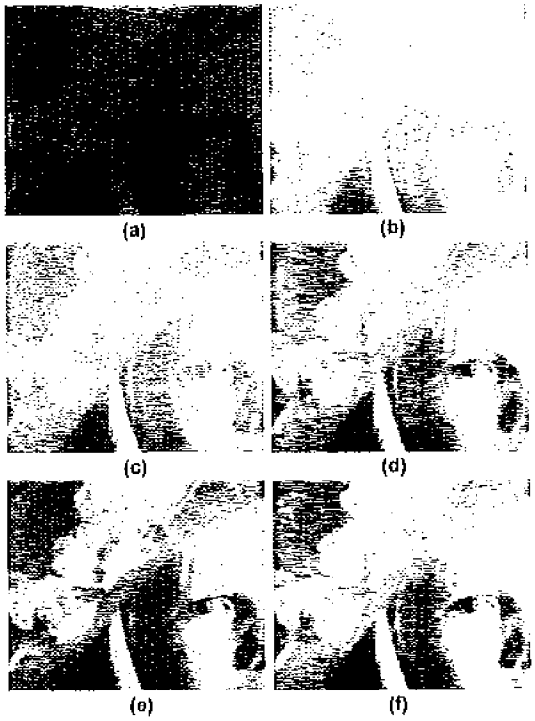

Figure 6.7.6: Images at different power supply voltages. (a) 1.0V (b) 1.2V (c) 1.5V (d) 2.0V (e) 2.5V (f) 3.3V.

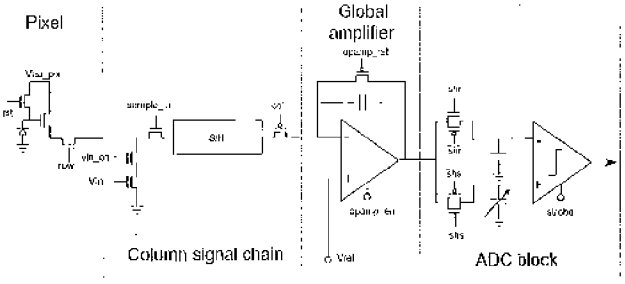

Figure 6.7.2: Simplified signal path from pixel to ADC.

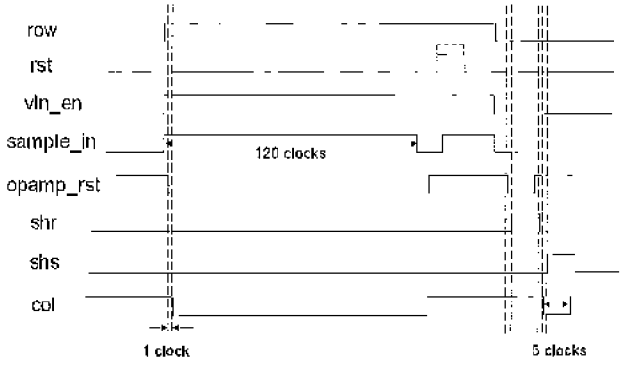

Figure 6.7.4: Relative timing for row and column operation.

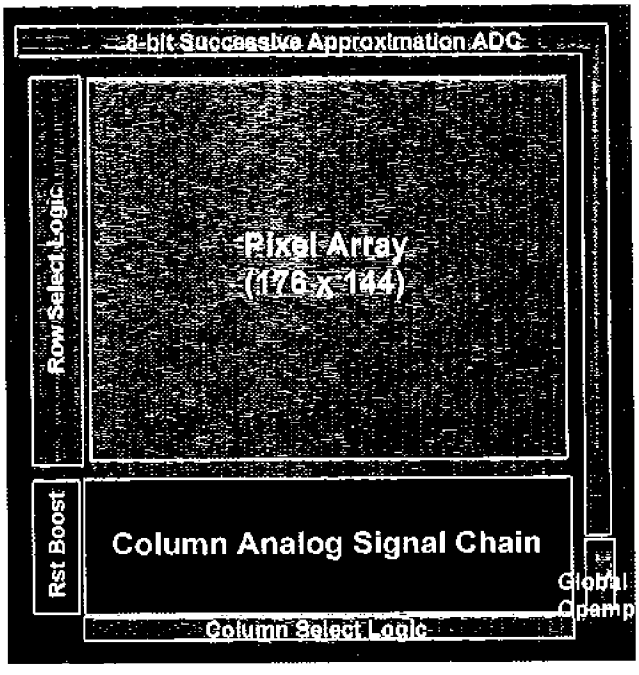

Figure 6.7.7: Sensor core micrograph.