1989
INTERNATIONAL SYMPOSIUM ON VLSI TECHNOLOGY, SYSTEMS AND APPLICATIONS

PROCEEDINGS OF TECHNICAL PAPERS

MAY 17-19, 1989/TAIPEI, TAIWAN, R.O.C.

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Library of Congress Number 88-83530
IEEE Catalog Number 89CH2631-0

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A 1 GHZ GaAs CCD WITH CAPACITIVE GATES AND HIGH TRANSFER EFFICIENCY

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ABSTRACT

A high performance GaAs charge-coupled device (CCD) structure is reported which has charge transfer efficiency (CTE) greater than 0.999 at 1 GHz. This device is the highest performance capacitive gate GaAs CCD yet reported. A new method of improving CTE in capacitive-gate CCD's by recessing the gap regions is described and preliminary experimental results presented. In addition, use of an AlGaAs cap layer resulting in a four order of magnitude reduction in Schottky gate leakage current is described.

INTRODUCTION

GaAs CCD's are important in many demanding signal processing applications because of their high speed, low noise capability coupled with the electro-optic properties of GaAs and other III-V compounds. These attributes are a consequence of the high electron mobility and wide direct bandgap in this material system. Applications range from imaging to addressing schemes for bandgap engineered electro-optic devices.

The primary obstacle to implementation of GaAs CCD's is achieving the necessary charge transfer efficiency (CTE) for the application. At low frequencies, as might be found in imaging applications, the Schottky gates used in GaAs CCD's present a significant dark current problem. During high frequency operation, limits on CTE depend on the device implementation.

Two CCD device structures based on Schottky barriers, rather than insulated gates, have found application in GaAs: capacitive-gate CCD's (CGCCD's) and resistive-gate CCD's (RGCCD's). CGCCD's shown in Fig. 1a, have the advantage of being well understood and using relatively low power. However, because of Fermi-level pinning at the GaAs surface, coupling of adjacent wells in CGCCD's relies on the proximity of adjacent electrodes. If the interelectrode gap spacing is excessive for the doping and thickness of the CCD channel layer, large potential troughs develop in the gap region. Of equal importance in CGCCD's is that the gate length be small enough that the charge move rapidly under the influence of the large fringing fields. If gate length is excessive, the charge transfer time will be limited by diffusion, reducing the maximum clock frequency.

RGCCD's eliminate the inter-electrode gap and ensure that the charge packets are transferred under the influence of electric field. In

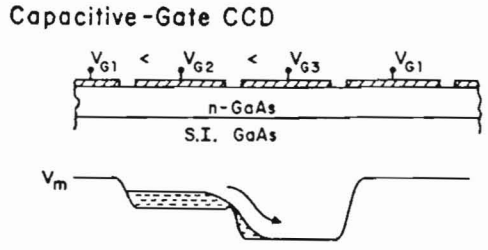

Fig. 1a Charge Transfer in a CGCCD

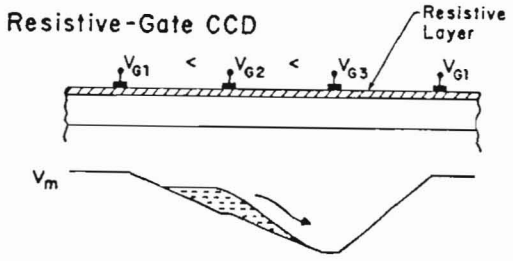

Fig. 1b Charge Transfer in a RGCCD

RGCCD's, shown in Fig. 1b, a layer of resistive material forms a Schottky barrier to the GaAs and is used as a continuous voltage divider between two or more finger contacts. The channel potential follows the linear resistive-gate voltage drop between finger electrodes and hence the carriers move under the influence of an electric field. Furthermore, since the thickness and doping of the active layer need not be parameters in the CCD device design, the active layer can be chosen for optimum MESFET performance. Compatibility with typical MESFET active layers is desirable in order to facilitate integration of the CCD's with high-performance on-chip amplifiers and digital logic for clock generation. Although the interelectrode gap is largely eliminated with RGCCD's, the gap is useful for clock feedthrough isolation, particularly for parallel-to-serial structures. The disadvantage of RGCCD's is that the gates dissipate dc power.

This paper describes the optimization of a CGCCD for high transfer efficiency at GHz frequencies. In addition, a new method of reducing the potential trough in the interelectrode gap region is proposed and preliminary experimental results discussed. Finally, to enhance GaAs CCD performance at low frequencies, a novel low dark current device structure is also presented.

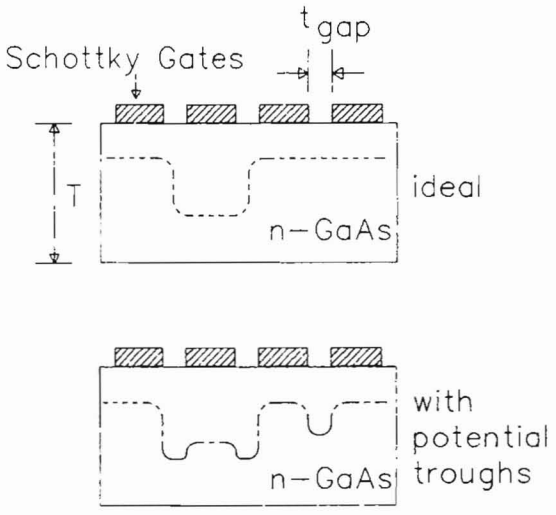

Fig 2. Channel potential for CGCCD

HIGH CTE CAPACITIVE-GATE CCD

In order to optimize CGCCD's, the interelectrode potential trough must be minimized. The gap potential trough problem is illustrated in Fig. 2. A 1-dimensional solution to Poisson's equation in the gap region indicates that for an empty potential well the channel potential is more positive than the gate by the pinch-off voltage of the active layer. If the same analysis is applied along the surface in the interelectrode gap, ignoring surface charge, the center of the gap is found to be more positive than the gates by an amount proportional to doping and gap size. As shown in Fig. 3, this implies that the channel under the gap is also more positive than the channel under the gates. (Note that this superposition of two 1-D solutions is qualitatively correct, but ignores 2-D effects and surface pinning.) Thus a decrease in doping or gap size results in a reduction of the trough depth. However, the dynamic range of the device is directly proportional to the product of doping and active

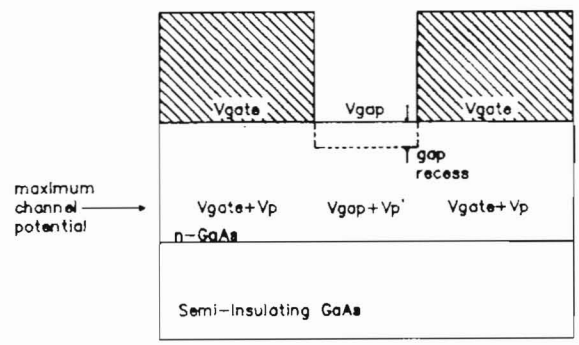

Fig. 3 1-D potential trough analysis

layer thickness. Since, the gap size is usually constrained by photolithography or process complexity, high CTE CGCCD's typically use low doped relatively thick active layers. Similarly, the device gate length determines the dynamic range of the device, but as discussed, short gate length is desirable for field assisted charge transfer. Further consideration must be given to the Schottky diode reverse breakdown and channel pinch-off voltages. In order for the output amplifier to be viable, the pinch-off voltage should be kept lower than the breakdown voltage. Schottky breakdown voltage increases

with increasing doping and channel thickness.

The high CTE device developed in this effort consisted of a 0.9 um thick n-type GaAs epitaxial channel layer doped at $7x10^{15}/cm^3$ on a Cr-doped semi-insulating substrate. Mesa isolation is used with Au-Ge alloyed ohmic contacts. Schottky gate metal is Cr-Au defined by lift-off. The threshold voltage for the

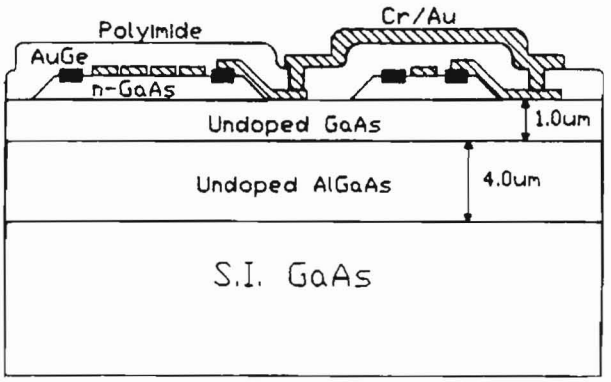

Fig. 4 CGCCD cross-section

channel is 3.0 volts, while the reverse bias breakdown voltage exceeded 15 volts. A photo-lithographically patternable polyimide is used for the interlayer dielectric. This polyimide requires only a UV cure. A second level of metal (Cr-Au) is used for interconnects. A device cross-section is shown in Fig. 4. Devices are wire bonded in high speed leadless chip carriers and press-fitmated to a microstripline test fixture. Fig. 5 is a schematic diagram of the high speed test setup.

The CCD is organized as a 4-phase, 50-stage (200 electrode) delay line. The transfer gates are 100 um wide by 2 um long, separated by 1 um gaps. The 2 um gate length is considerably shorter than that used in previous work.[1] The output stage is a MESFET source-follower with an active load and dual-gate reset . FET gate lengths are 1 um.

At the maximum test frequency of 1 GHz, the input-to-output delay is 50 nsec with a CTE exceeding 0.999, as shown in Fig. 6. CTE is determined by the summation of leading-edge loss, as proposed by Brodersen et al.[2] A two-dimensional solution to Poisson's equation in the gap region, accounting for surface pinning, finds the potential trough depth to be 120 mV. There is no isolation electrode at the end of the delay line, which accounts for the significant amount of clock feedthrough at the output. The clock swing is 0 to 5 volts.

RECESSED-GAP STRUCTURE

To achieve greater compatibility with high transconductance MESFET's, which require thin, highly doped active layers, previous effort has

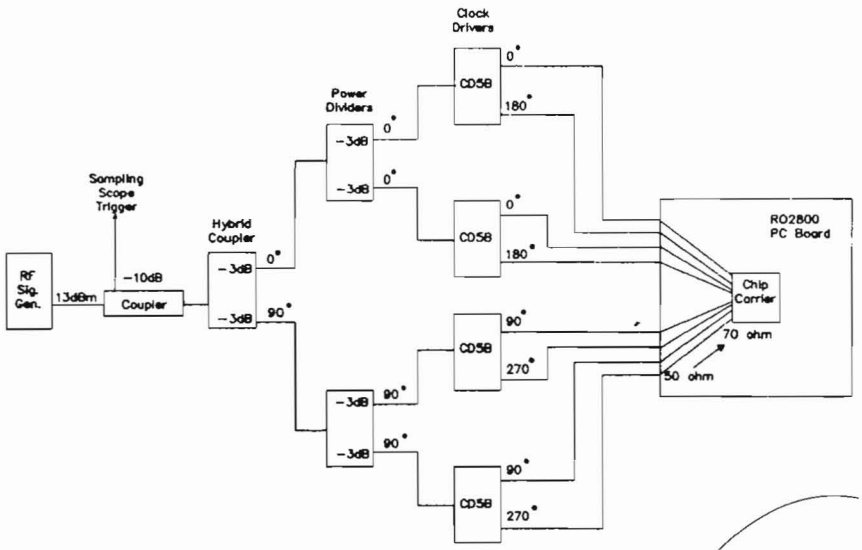

Fig. 5 High Speed Test Station

concentrated on reducing the size of the interelectrode gap.[3,4,5] Referring to Fig. 3, the objective is to reduce the potential at the surface in the center of the gaps, V_{gap}. The detrimental effect of these ultra-small gaps is a decrease in the gate-channel-gate breakdown voltage and an increase in the gate-to-gate capacitance.

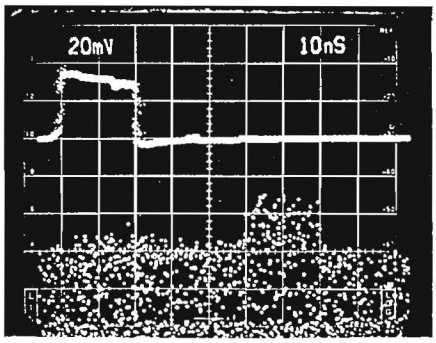

Fig. 6a A 50 nsec delay

A new method of improving CTE, while avoiding the problems associated with ultra-small gaps, is to recess the active channel in the interelectrode gap region. Again referring to Fig. 3, rather than reducing V_{gap}, the pinch-off voltage

Table 1 Simulation of gap region

Gap Size (um)	Channel Thick-ness (um)	Doping (/cm^3)	Gap Recess Depth (A)	Channel Potential Under Gate (volts)	Channel Potential Under Gap (volts)	Potential Trough (volts)
2.0	0.2	1x10^{17}	0	2.36	7.55	5.19
1.5	0.2	1x10^{17}	0	2.36	5.91	3.55
1.0	0.2	1x10^{17}	0	2.36	4.31	1.95
0.75	0.2	1x10^{17}	0	2.36	3.59	1.23
0.5	0.2	1x10^{17}	0	2.36	2.92	0.56
0.25	0.2	1x10^{17}	0	2.36	2.44	0.08
1.0	0.2	1x10^{17}	0	2.36	4.31	1.95
1.0	0.2	1x10^{17}	100	2.36	3.91	1.55
1.0	0.2	1x10^{17}	200	2.36	3.61	1.25
1.0	0.2	1x10^{17}	300	2.36	3.28	0.92
1.0	0.2	1x10^{17}	400	2.36	2.95	0.59
1.0	0.2	1x10^{17}	500	2.36	2.60	0.24
1.0	0.2	1x10^{17}	600	2.36	2.23	−0.13
1.0	0.2	1x10^{17}	700	2.36	1.84	−0.52

in the gap region is reduced. In this process, the relatively large gap of 1 um is recessed by post-gate-definition etching. Table 1 shows the results of a 2-D electrostatic modelling, which includes Fermi-level pinning and surface charge. As expected reduction of the gap size reduces the potential trough depth. In addition, the simulation shows

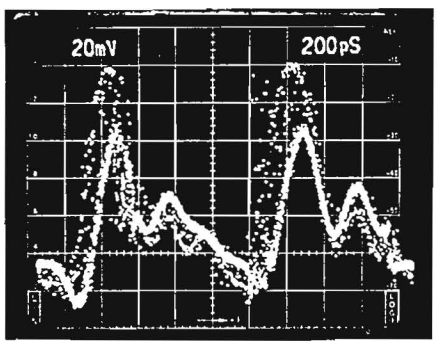

Fig. 6b Output amplifier signal

that recessing the interelectrode gap results in a corresponding decrease in trough depth. The results also suggests that the recess depth should be fairly well controlled to avoid the formation of potential barriers.

Preliminary results have been obtained by recessing the above CCD structure with a weak 1:1:2000, $NH_4OH:H_2O_2:H_2O$ solution. The etch rate is approximately 100 A/min and etch depth is monitored using an Alpha Step surface profiler. The active layer used is 1350 A thick with n-type doping of 2.1x10^{17}/cm^3 and threshold voltage of 1.9 volts. For no recess and a 300 A recess, with corresponding trough depths of 4 volts and 2 volts, no output from a 150 ns input pulse is discernable. For a 500 A recess, potential trough depth of 0.2 volts, an output is obtained with a 50 nsec delay and an apparent CTE of 0.82 at 800 MHz. Further work is in progress to confirm the result and correlate the recess depth measurement with post-recess electrical measurements in order to monitor both recess depth and uniformity. In the present experiment, the input and output impedance of the delay line is increased due to the recessing etch, making systematic assessment difficult.

REDUCTION OF GATE LEAKAGE CURRENT

Excessive gate leakage current degrades CTE and dynamic range by adding charge to the signal packet during each transfer. This becomes particularly problematic in imaging applications at low clock rates, where the non-uniformity in leakage from pixel to pixel gives rise to fixed pattern noise.

Previous III-V imagers[6] sought to take advantage of the low bulk generation rate in wider-bandgap AlGaAs by using this material as the channel layer. Observation of bulk-generation-dominated dark current in these devices was possible because the Schottky barrier heights on AlGaAs are higher than on GaAs. Unfortunately, the relatively low electron mobility of AlGaAs prohibits the realization of high transconductance FET's and high frequency operation.

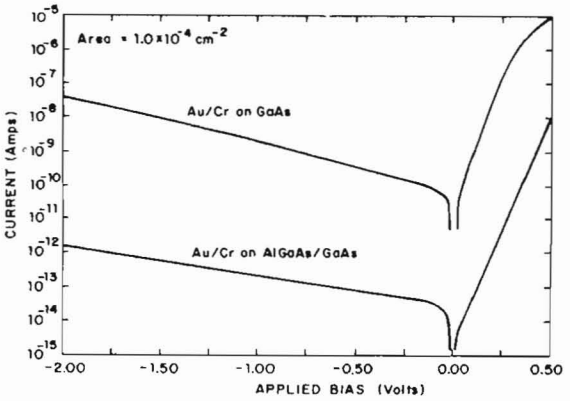

Fig. 7 Comparison of Schottky I-V with AlGaAs cap and without

An alternative approach has been investigated in which a 500 A cap layer of AlGaAs is used to increase the Schottky barrier height, while retaining the GaAs active layer. No major process modification is needed to accommodate the thin AlGaAs top layer. Fig. 7 shows the results for diodes fabricated on top of the AlGaAs and on the GaAs after a recessing etch through the AlGaAs. A four order of magnitude reduction in leakage current is achieved, which makes the leakage current of the CCD gates comparable to the bulk generation rate for GaAs. To date, CGCCD's with an AlGaAs cap layer have been fabricated and demonstrated.

CONCLUSION

With the emerging maturity of III-V bandgap engineered detector structures, GaAs CCD's are increasing in importance as addressing and readout structures. In an effort to improve fundamental performance criteria over a large bandwidth, a number of investigations have been conducted to optimize CTE in the GHz range as well as extend the useful low frequency range of the device.

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ACKNOWLEDGMENTS

The authors would like to thank the following for valuable discussion and assistance: J.Woodall, M. Tischler, and P. Kirchner at IBM T.J. Watson Research Center; R. Sahai at Rockwell International; S. Othmer at Hughes MSG;and R. Ade at Columbia University. Support for this work has been provided, in part, by the NSF Center for Telecommunications Research, the ONR URI Program, an NSF Presidential Young Investigator Award, the International Test Foundation, Rockwell International, and Hughes Aircraft Company.