Received 9 August 2016; revised 5 October 2016; accepted 13 October 2016. Date of publication 19 October 2016;
date of current version 20 December 2016. The review of this paper was arranged by Editor A. G. Unil Perera.

Digital Object Identifier 10.1109/JEDS.2016.2618721

Analytical Modeling and TCAD Simulation of a Quanta Image Sensor Jot Device With a JFET Source-Follower for Deep Sub-Electron Read Noise

JIAJU MA (Student Member, IEEE), AND ERIC R. FOSSUM (Fellow, IEEE)

Thayer School of Engineering, Dartmouth College, Hanover, NH 03755, USA

CORRESPONDING AUTHOR: E. R. FOSSUM (e-mail: eric.r.fossum@dartmouth.edu)

This work was supported by Rambus.

ABSTRACT A novel quanta image sensor (QIS) jot device with a CMOS compatible junction-field effect transistor (JFET) source follower (SF) is introduced. The device is proposed to further reduce the read noise of QIS jots and ultimately realize a read noise of 0.15e-r.m.s. for accurate photoelectron counting. We take advantage of the small gate capacitance in a p-channel JFET SF to reduce the total capacitance of the floating diffusion, which yields a greatly improved conversion gain of 1.38 mV/e- in TCAD simulation compared to MOSFET SF with the same pitch size. Lower 1/*f* noise is also anticipated yielding a low input-referred read noise. The device is designed in a 45 nm CMOS image sensor process. The fundamental working principles of this device are discussed, and important functionalities are analyzed with simulation and theory.

INDEX TERMS CMOS image sensor, quanta image sensor, jot device, low noise imaging, TCAD simulation.

I. INTRODUCTION

The quanta Image Sensor (QIS) was first proposed in 2004 as a "digital film camera" [1], [2] outlining a different way to utilize sub-diffraction-limit (SDL) pixels. In the concept, a QIS might consist of one billion specialized sub-micrometer-pitch pixels, which are called "jots". The large array of jots work at a high frame rate (e.g., 1000fps) and with extremely low power consumption [3]. The small area size per jot and high frame rate ensures that the photon exposure on each jot per frame is limited to several photons. Jots detect the number of incident photons, and then output single-bit or multi-bit digital data corresponding to this number [4]. The final image is created by integrating the digital data both spatially over multiple jots and temporally over multiple frames [5] with image processing. If jots can count photoelectrons in each frame so accurately that counting error is negligible, noise-free jot data binning is achievable. QIS can enable many applications, such as high-dynamic-range imaging in consumer photography [6], scientific imaging, security [7], and encryption [8].

In a photoelectron counting image sensor, the counting accuracy or counting error rate is impacted by many characteristics, and the noise floor of the signal readout chain is the dominant factor [9]. Deep sub-electron read noise (DSERN) (read noise lower than 0.5e- r.m.s.) is a prerequisite for photoelectron counting capability, and read noise of 0.15e- r.m.s. or lower is necessary for ultimately accurate photoelectron counting (0.04% counting error rate). The counting error rate is so sensitive that a mild increase of read noise, e.g., 0.25e-r.m.s., will increase the error rate to 1%.

The photoelectron signal is converted to a voltage signal by the floating diffusion (FD) node capacitance. The voltage signal is sensed by an in-pixel SF and subsequently amplified and digitized. In low-noise image sensors, the in-pixel SF is generally the most significant contributor to the total read noise (commonly 100-200 μV r.m.s.). It is a result of higher 1/*f* noise caused by shrinking SF area size and lack of

amplification of signal before the SF. Two major noise types in a SF are 1/*f* noise and random telegraph signal (RTS). The origin of RTS is known to be related to the random capture and emission of channel carriers by Si-SiO_2 interface traps [10]. There is still debate on the origin of 1/*f* noise, but the most widely accepted explanation is the fluctuation of conduction carrier population due to interface traps and the fluctuation of carrier mobility due to phonon scattering [11].

Many experiments have been done to reduce SF noise. Replacing the surface-channel SF with a buried-channel SF has been used historically in CCDs [12] and CMOS image sensors [13]. In-pixel buried-channel SF and correlated multiple sampling (CMS) can be used together for improved noise reduction [14], [15]. Improvement in noise in minimum geometry buried-channel SF transistors in advanced technology nodes may be less [16], perhaps due to STI sidewall effects. In addition, three-fold SF noise reduction was recently demonstrated by tuning the bandwidth of correlated double sampling (CDS) circuitry [17].

To reduce input-referred read noise, another approach is to increase the signal using avalanche multiplication. This approach has been applied to CCDs [18], single-photon avalanche detectors (SPADs) [19], and CMOS image sensors [20]. However, use of avalanche multiplication has a number of drawbacks including high electric fields and operating voltages, that lead to large pixel size, high dark count rate, manufacturing challenges and reliability issues.

Another approach is to increase the conversion gain by reducing the capacitance of the floating diffusion node. The pump-gate (PG) jot device developed by our group improved CG to 410 μV/e- by reducing the FD parasitic capacitance induced by transfer gate (TG) and reset gate (RG) [21]–[23], and a best-case 0.22e- r.m.s. read noise was demonstrated. For the first time the PG jot enabled DSERN and photoelectron counting without electron multiplication, which was a major step forward in our efforts to realize highly accurate photoelectron counting for QIS applications. However, more progress needs to be made to further reduce read noise to 0.15e- r.m.s. or lower. In general, QIS jot devices have good compatibility with most of the existing read noise reduction techniques, but CMS requires relatively long processing time and low temperature which may not be compatible with the high frame rate used with QIS. In a PG jot device, the SF gate oxide capacitance is the dominant contributor to the total FD capacitance, so the reduction of SF size is inevitable for future improvements in CG. As is well-known and re-verified in our PG jot devices, the reduction of SF size leads to higher 1/*f* noise [22], [23], so the improvement in CG from smaller SF will be negated by higher 1/f noise, and input-referred read noise will hardly be improved. From this dilemma arises the motivation for the present approach.

In this paper, a jot device with a junction-field effect transistor (JFET) SF is proposed. The JFET SF is a good alternative because of its potential for low-noise and scalability [24], [25], which may be a solution for the SF-size-shrinking tradeoff with 1/*f* noise allowing for higher CG and lower SF noise simultaneously compared to a PG jot with MOSFET SF. The device is designed with TCAD simulation tools in a 45nm backside illumination (BSI) process and will be fabricated in the coming year. In the following sections, the fundamental working principles of this device will be discussed, and important functionalities are analyzed with simulation and theory.

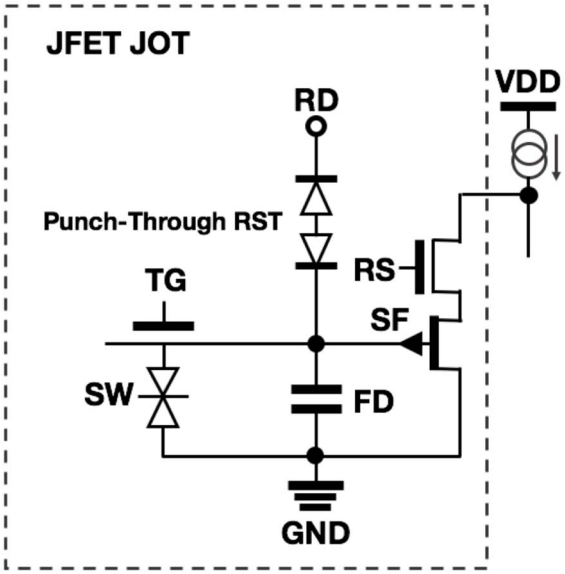


FIGURE 1. Schematic of a jot device with a JFET SF and punch-through reset.

II. DEVICE DESCRIPTION

The schematic of the jot device is shown in Fig. 1. The jot consists of a pump-gate TG, a reset transistor, a JFET SF and a row-select transistor. The reset transistor can also be replaced with a punch-through reset diode for further improvement in CG, and more details will be discussed in Section IV. The JFET SF has a p-type channel and n-type gate. The source (SRC) of SF is biased by a current source, and its drain (DRN) is biased to ground (GND). The pump-gate TG and photoelectron storage well (SW) have a similar design to the previously fabricated PG jots. The 3D doping profile of this device with a punch-through reset diode obtained from TCAD simulation is depicted in Fig. 2. As shown, FD also functions as the gate of the SF, located underneath a shallow p-type channel. During the readout, photoelectrons transferred from SW to FD cause a potential change in the integrated gate of the JFET, or FD. This in turn modulates the JFET current. If the JFET is used as a SF and operates in the saturation region, the voltage on the source will follow the FD potential. Because the JFET is built on a p-type substrate, the p-type source has to be isolated from the substrate to avoid a short-circuit current from the source to the bulk. The isolation is achieved by extending the FD n-well under the source and surrounding the source with STI. Using a similar concept, a buried-channel version of

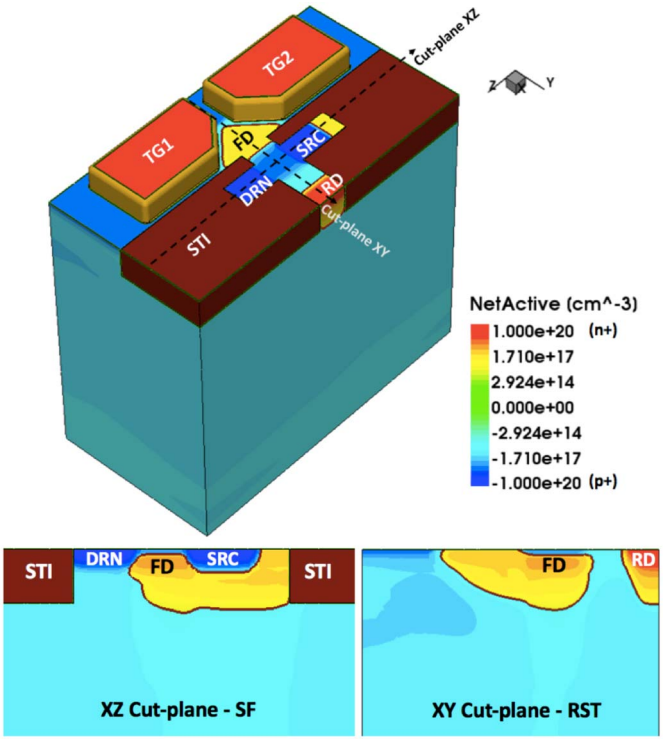


FIGURE 2. Doping profiles from 3D modeling in TCAD. Row Selector (RS) is not included. 3D doping profile of a 2x1 shared jot with a JFET SF (Top). Cut-planes doping profile of SF region (XZ) and punch-through reset (RST) region (XY).

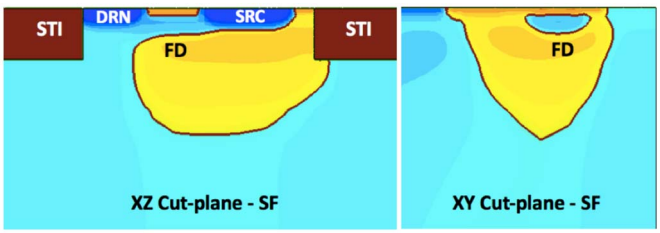


FIGURE 3. Doping profiles from 3D TCAD simulation. Cut-planes doping profile of buried-channel JFET SF region on XZ plane (left) and XY plane (right).

this device is also designed as shown in Fig. 3 to potentially further reduce 1/*f* noise from surface effects.

This device enables the reduction of many FD capacitance components. First, in a pixel with a MOSFET SF, the FD node is connected to the gate of SF through a metal wire. In order to have an ohmic contact, the FD node needs to be heavily doped, which increases the FD-sub junction capacitance. In the proposed device, since the FD is integrated in the SF, a metal connection is not necessary, therefore the doping of the FD can be reduced, which yields a smaller junction capacitance. Second, the large gate-oxide capacitance in small-scale a MOSFET SF, resulting from extremely thin oxide, is replaced by a relatively small junction capacitance between the gate and channel. A comparison of parasitic capacitance components is depicted in Fig. 4, in which the capacitance data of MOSFET SF device is extracted from

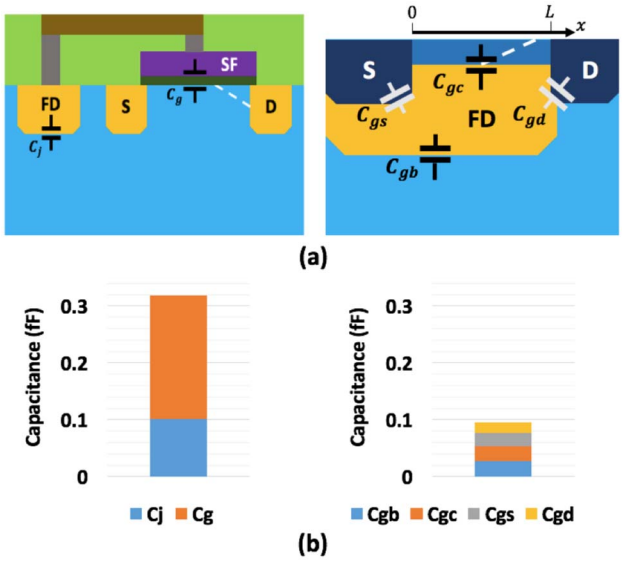


FIGURE 4. (a) Capacitance components in a TPG Jot with MOSFET SF [18] (left) and a JFET Jot (right). (b) Comparison of calculated capacitance components in the two types of jots.

the TPG jot device published in [21] and the capacitance of this JFET SF is obtained from analytic calculation and simulation. The result clearly shows the total FD capacitance can be greatly reduced with a JFET SF approach.

In a MOSFET SF, the interface traps on the surface and STI side-wall interact with conduction carriers in the channel, and noise is introduced by the resulting carrier population fluctuation and threshold fluctuation. In this JFET SF, since the gate is located underneath the channel and the channel is surrounded by FD instead of STI, the interface traps have less impact on the conduction carriers and threshold. Lower 1/*f* noise can be expected because the amount of traps in the silicon bulk is much less than the amount of interface traps.

III. THEORETICAL DEVICE ANALYSIS

Many theoretical studies of JFET devices have been presented in [26]–[28]. Compared to conventional JFET devices in [27], the device in this paper has a relatively short channel length, so the short channel effects become more important when modeling the device characteristics. Compared to typical short-channel JFETs, the gate in this JFET is relatively lightly doped, and due to its asymmetric structure, the conventional short-channel JFETs model cannot match the device performance properly. We felt some additional theoretical analysis is necessary for a better understanding of this device, but as the major design work still relies on TCAD simulation, a simplified 1D analytic model was developed to be used for verification and estimation.

A. PINCH-OFF EFFECT AND EFFECTIVE CHANNEL DEPTH

In the JFET, the channel and gate form a PN junction, and the effective channel depth is equal to the physical channel

depth minus the depth of the depletion region induced by the gate potential. The abrupt junction assumption is used to get the channel depletion region depth:

$$D(x) = \left\{ \frac{2\varepsilon_s \beta}{q} \left[V_{bi_{gc}} + V_g - V_c(x) \right] \right\}^{\frac{1}{2}} \quad (1)$$

where q is the elementary charge of holes, ε_s is the permittivity of silicon, $V_{bi_{gc}}$ is the gate-channel built-in voltage, V_g is the gate bias voltage, and $V_c(x)$ is the potential in the channel at location x. β is a doping ratio coefficient defined as:

$$\beta = \frac{N_d}{N_a} \frac{1}{N_a + N_d} \quad (2)$$

where N_a and N_d are the doping concentration of the channel and the gate respectively. The coordinate system that will be used in the following discussions is defined in Fig. 4(a): $x = 0$ is the origin of the channel at the source-end; and $x = L$ is the endpoint of the channel at the drain-end, with L being the physical channel length.

The channel potential is determined by the bias voltages applied to the source V_S, and the drain V_D. When the JFET is setup as a SF, the drain is biased to ground and the source has a positive output voltage, so the situation when $V_{SD} > 0$ is of most interest. Under this condition, $V_c(x)$ decreases gradually from the V_S (at $x = 0$) to V_D (at $x = L$).

When the depletion region depth is equal to or greater than the physical channel depth, pinch-off occurs. From Eq.1, it can be anticipated that pinch-off will happen at the drain-end first as V_g increases. The pinch-off voltage is defined in [26] as:

$$V_p = V_{bi_{gc}} + V_{GS} - V_{SD_{sat}} = \frac{qh^2}{2\varepsilon_s \beta} \quad (3)$$

where h is the physical channel depth, and $V_{SD_{sat}}$ is the minimum source-drain voltage to trigger pinch-off under a given gate bias V_{GS}. As V_{GS} increases, pinch-off will expand towards the source, and the whole channel will be cut-off when pinch-off reaches the source-end. The cut-off voltage is then given by:

$$V_{GS_{cutoff}} = V_p - V_{bi_{gc}} \quad (4)$$

Pinch-off and cut-off effects can be observed in TCAD simulation and examples are shown in Fig. 5.

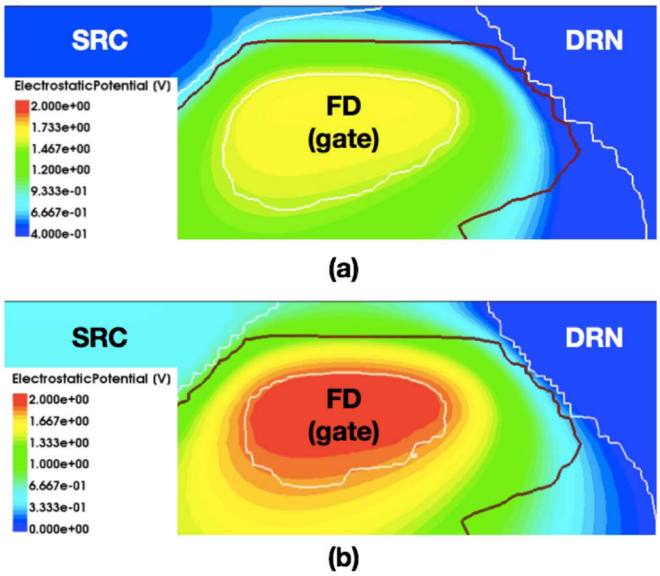


FIGURE 5. Illustrations of pinch-off and cut-off effects from TCAD simulation. Electrostatic potential profile is shown in color. The boundary of depletion region is shown in white lines. (a) Pinch-off effect, where $V_{GS} = 0.1V$ and $V_{SD} = 0.4V$. (b) Cut-off effect, where $V_{GS} = 0.3V$ and $V_{SD} = 0.4V$.

B. DRAIN CURRENT BEFORE SATURATION

A longitudinal electric field is created in the channel by V_{SD}, resulting in a hole current from source to drain. The current flowing through the cross-section of channel at location of x is given by,

$$I_D(x) = W\left[h - D(x)\right] N_a q \mu_{HF}(x) \frac{dV_c}{dx} \quad (5)$$

where W is the channel width, and $\mu_{HF}(x)$ is the mobility of holes. In a short-channel device, the carrier mobility reduces significantly with relatively high electric field, and the dependence can be described by an empirical model given in [26]:

$$\mu_{HF} = \frac{\mu_p}{1 + \left(\frac{\mu_p \mathcal{E}(x)}{v_s} \right)} \quad (6)$$

where $\mathcal{E}(x)$ is the electric field, μ_p is the low-field hole mobility that is also doping dependent, and v_s is the hole saturation velocity in silicon. By integrating Eq. 5, the average drain current can be obtained. The detailed calculation of this step can be found in [26]. The result is given as:

$$I_D = -\frac{g_0 V_p}{1 + \left(\frac{\mu_p V_{SD}}{v_s L} \right)} \left\{ \left(u_D^2 - u_S^2 \right) - \frac{2}{3} \left(u_D^3 - u_S^3 \right) \right\} \quad (7)$$

$$g_0 = \frac{Wh}{L} N_a \mu_p q \quad (8)$$

where g_0 is the unit transconductance, and u_S, u_D are the normalized depletion depth at the source-end and drain-end of the channel:

$$u_S = \frac{D(0)}{h} = \left\{ \frac{2\varepsilon_s \beta}{q} \left[V_{bi_{gc}} + V_{GS} \right] \right\}^{\frac{1}{2}} / h \quad (9)$$

$$u_D = \frac{D(L)}{h} = \left\{ \frac{2\varepsilon_s \beta}{q} \left[V_{bi_{gc}} + V_{GS} + V_{SD} \right] \right\}^{\frac{1}{2}} / h. \quad (10)$$

C. SHORT-CHANNEL EFFECTS

In this JFET device, several short-channel effects arise as non-negligible factors affecting device current-voltage characteristics. One of the several phenomena, carrier mobility reduction due to high electric field, is already discussed in the previous discussion. Another important effect, channel length

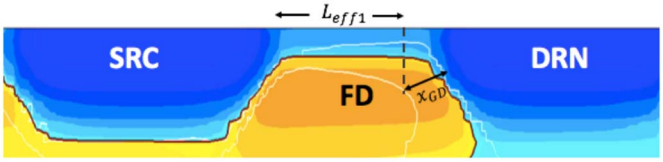


FIGURE 6. Illustration of drain-induced gate depletion in TCAD simulation when $V_{GS} = -0.5V$ and $V_{SD} = 1V$. The white lines are boundaries of depletion region. L_{eff1} is the effective channel length.

modulation (CLM), is the shortening of the effective channel length with increased drain bias, which is seen as an increase in current and reduction of output resistance with increased drain bias. CLM caused by drain-induced gate depletion as well as pinch-off are considered in this model.

C.1. CLM BY DRAIN-INDUCED GATE DEPLETION

According to Eq. 1, the amount of carriers in the channel is controlled by V_{GS} and is ideally independent of V_{SD}. However, because the drain has much higher doping than the gate, the gate is partially depleted by the drain, as shown in Fig. 6. In the depletion region, as a result of charge conservation the drain supplies carriers to the channel, and hence leads to a reduction in the output resistance and an increase in current. Because the depletion region width x_{GD} is of the same order of magnitude as the channel length, the resulting CLM effect has a strong influence on the I-V characteristics. One may expect the same effect at the source-end, but since V_{GS} is always lower than V_{GD}, the gate depletion is much weaker at the source-end. Assuming a continuous current flowing from the source to the drain, the current in the gate depletion region is equal to the current flowing in the effective channel region, therefore the drain current I_D can be calculated by the current flowing in the effective channel region. The effective channel length is given by,

$$L_{eff1} = L - x_{GD} \tag{11}$$

$$x_{GD} = \sqrt{\frac{2\varepsilon_s}{q}\frac{N_{aD}}{N_d}\frac{1}{N_{aD}+N_d}\left(V_{bi_{gd}} + V_{GS} + V_{SD}\right)} \tag{12}$$

where N_{aD} is the drain doping concentration and $V_{bi_{gd}}$ is the gate-drain built-in voltage.

C.2. CLM BY PINCH-OFF

After pinch-off occurs near the drain, the JFET operates in saturation mode. The pinch-off region will expand towards the source with further increased V_{SD}. The channel cannot get any narrower once pinch-off is reached at the drain-end, however higher V_{SD} will increase the electric field prior to the pinch-off point, and hence leads to an increase in the current. Similar to CLM caused by the drain-induced gate depletion, to maintain a continuous current in the whole channel, the current flowing in the pinch-off region must be equal to the current in the previous region, and I_D can be calculated by the current-flow prior to the pinch-off point. To locate the the pinch-off point, the channel potential as a function of x needs to be identified according to Eq. 1. In TCAD, the channel potential profile is a numerical solution of a 3D charge conservation equation given by Gauss' law. The same scenario cannot be applied to a 1D model, and approximation is necessary to get an analytical answer. Based on the TCAD results and following the well-demonstrated approach used in [29], an approximation is made that the hole velocity in the channel is a linear function of x, and the channel potential profile can be obtained using this approximation. The analytical potential profile was re-verified with a 3D TCAD simulation and showed good agreement. It is worth noting that this assumption is valid when the maximum hole velocity is lower than its saturation velocity, which is suitable for the condition in which this JFET is operating. In other cases, the velocity saturation model in [26] can be applied instead.

The expression of hole velocity is derived from Eq. 6:

$$v(x) = \mu_{HF}\mathcal{E}(x) = \frac{\mu_p\mathcal{E}(x)}{1+\left(\frac{\mu_p\mathcal{E}(x)}{v_s}\right)} = C_v x \tag{13}$$

where C_v is a linear coefficient. From Eq. 13, the expression of electric field is given,

$$\mathcal{E}(x) = \frac{C_v x}{\mu_p\left(1-\frac{C_v x}{v_s}\right)} \tag{14}$$

and the channel potential expression can be obtained by integrating Eq. 14:

$$\begin{aligned} V_c(x) &= -\int_0^x \mathcal{E}(t)\,dt \\ &= -\frac{v_s}{\mu_p}x - \frac{v_s^2}{\mu_p C_v} ln\left(1-\frac{C_v x}{v_s}\right) \end{aligned} \tag{15}$$

With a given bias V_{SD} and channel length L. The coefficient C_v can be solved with:

$$-\frac{v_s}{\mu_p}L - \frac{v_s^2}{\mu_p C_v} ln\left(1-\frac{C_v L}{v_s}\right) = V_{SD} \tag{16}$$

Then the effective channel length L_{eff2} can be obtained by solving:

$$-\frac{v_s}{\mu_p}L_{eff2} - \frac{v_s^2}{\mu_p C_v} ln\left(1-\frac{C_v L_{eff2}}{v_s}\right) = V_{SD_{sat}}. \tag{17}$$

C.3. DRAIN CURRENT WITH SHORT CHANNEL EFFECTS

The expression of drain current in Eq. 7 can be updated to include the modulation of effective channel length as:

$$I_D = -g_0 g_{sc} V_P\left\{\left(u_\theta^2 - u_S^2\right) - \frac{2}{3}\left(u_\theta^3 - u_S^3\right)\right\} \tag{18}$$

where g_{sc} is the short-channel transconductance coefficient:

$$g_{sc} = \frac{1}{\frac{L_{eff}}{L} + \frac{\mu_p V_\theta}{v_s L}} \tag{19}$$

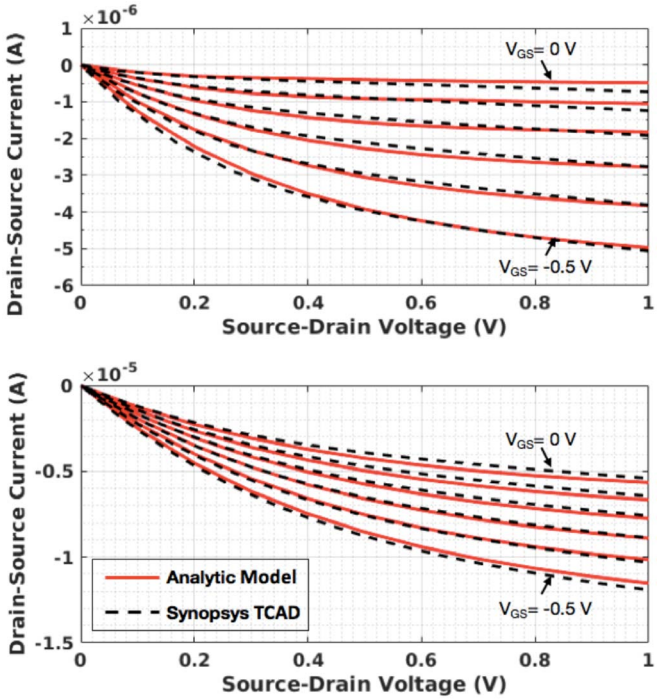


FIGURE 7. I-V curves of Device 1 (Top) and Device 2 (Bottom). Curve with V_{GS} from −0.5V to 0V are presented. The red solid lines are data from analytic model, and the black dashed lines are simulation results from Synopsys TCAD tools.

and L_{eff} is the effective channel length considering modulations from DIBL and pinch-off effects.

$$L_{eff} = \begin{cases} L_{eff1} & V_{SD} \le V_{SD_{sat}} \\ \min\left(L_{eff1}, L_{eff2}\right) & V_{SD} > V_{SD_{sat}} \end{cases} \tag{20}$$

In Eq. 19, $V_\theta = V_c(L_{eff})$ is the potential at the endpoint of the effective channel, and u_θ is the normalized depletion depth at the endpoint of the effective channel.

$$V_\theta = -\frac{v_s}{\mu_p} L_{eff} - \frac{v_s^2}{\mu_p C_v} ln\left(1 - \frac{C_v L_{eff}}{v_s}\right) \tag{21}$$

$$u_\theta = \left\{\frac{2\varepsilon_s \beta}{q}\left[V_{bi} + V_{GS} + V_\theta\right]\right\}^{\frac{1}{2}} / h. \tag{22}$$

D. CURRENT-VOLTAGE CHARACTERISTICS

Given the device parameters, the I-V curves can be plotted with Eq. 18. This model was compared to the TCAD results. The parameters of the devices being used for verification are listed in Table 1. Device 1 has actual parameters for a jot device, and device 2 has some intentional doping variations from device 1 to test the robustness of this model. The I-V curves with different V_{GS} are depicted in Fig. 7. The results from both devices showed a good alignment with the TCAD simulation.

When the JFET is used as a SF, transconductance g_m is important in terms of gain and load driving capability, and higher g_m is desired for low-noise and high-speed readout.

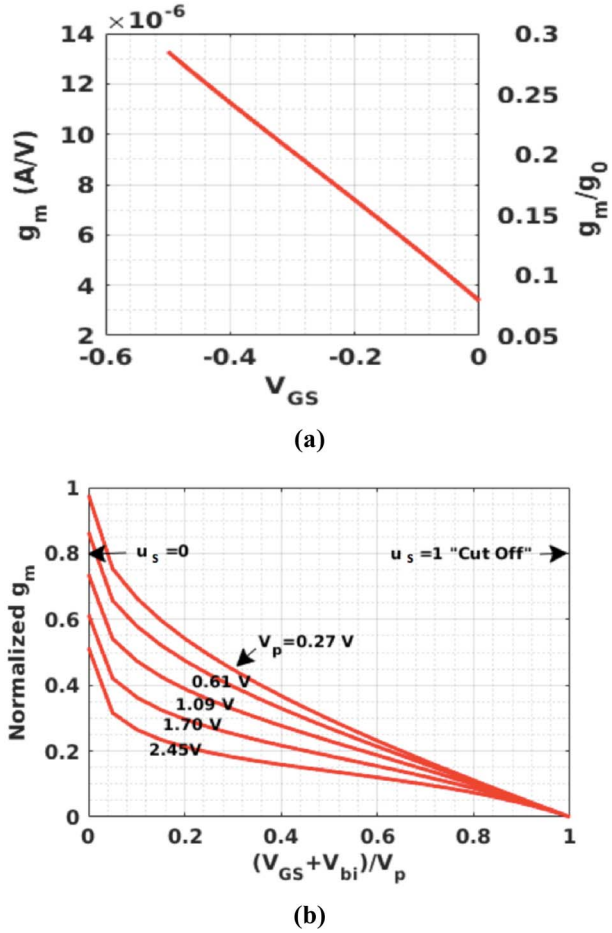


FIGURE 8. Analytic results of transconductance. (a) g_m and normalized g_m of device 1 as a function of V_{GS}. (b) normalized g_m of device 1 as a function of bias condition and pinch-off voltage.

Transconductance g_m can be derived at $V_{SD} = V_{SD_{sat}}$:

$$g_m = \frac{\partial I_{Dsat}}{\partial V_{GS}} \tag{23}$$

Substituting Eq. 18 in Eq. 23, the expression of g_m can be obtained. It is worth noting that under this condition L_{eff} is not a function of V_{GS} according to Eq. 3 and Eq. 12, and thus we have:

$$g_m = \left\{-I_{Dsat}\frac{g_{sc}\mu_p v_s}{L_{eff}}\frac{\partial V_\theta}{\partial V_{GS}}\right\} + \left\{g_0 g_{sc}\left\{u_\theta\left(1 + \frac{\partial V_\theta}{\partial V_{GS}}\right) - \frac{\partial V_\theta}{\partial V_{GS}} - u_s\right\}\right\} \tag{24}$$

Because the first term is much smaller than the second term, Eq.24 can be simplified to:

$$g_m = g_0 g_{sc}\left\{u_m - u_S\right\} \tag{25}$$

where, u_m is a short-channel coefficient:

$$u_m = u_\theta\left(1 + \frac{\partial V_\theta}{\partial V_{GS}}\right) - \frac{\partial V_\theta}{\partial V_{GS}} \tag{26}$$

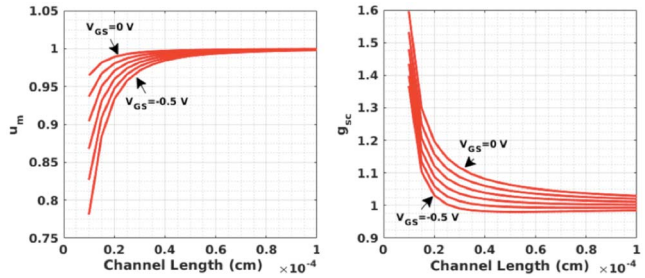


FIGURE 9. Short channel factors u_m and g_{sc} with different channel length L and V_{GS}.

the term $\frac{\partial V_\theta}{\partial V_{GS}}$ can be solved from Eq. 21:

$$\frac{\partial V_\theta}{\partial V_{GS}} = -\frac{\ln\left(1-\frac{C_v L_{eff}}{v_s}\right)+\frac{C_v L_{eff}}{v_s - C_v L_{eff}}}{\ln\left(1-\frac{C_v L}{v_s}\right)+\frac{C_v L}{v_s - C_v L}} \tag{27}$$

and C_v can be obtained from Eq. 16 with $V_{SD} = V_{SDsat}$. The normalized g_m is given by,

$$\frac{gm}{g_0} = g_{sc}\{u_m - u_S\} \tag{28}$$

As depicted in Fig. 8(a), the normalized g_m has a value from 0 to 1 and is dependent on V_{GS}. It suggests that g_m is mainly determined by g_0, and g_0 is affected by the device dimensional ratio $\frac{Wh}{L}$ and the channel doping concentration N_a. With given device parameters, lower V_{GS} is preferred for higher g_m. Short-channel factors u_m and g_{sc} both tend to 1 as channel length increases, as shown in Fig. 9. In long-channel JFETs, Eq. 28 can be simplified to:

$$g_m = g_0(1-u_S) = g_0\left[1-\left(\frac{V_{bi_{gc}}+V_{GS}}{V_p}\right)^{\frac{1}{2}}\right] \tag{29}$$

which exactly matches the result in [26]. The unit transconductance g_0 of device 1 is $51.1\mu A/V$, which is very close to the unit transconductance of a PMOS SF ($\sim 54\mu A/V$) with the same dimensions and under the same process, but lower than a NMOS SF with the same dimensions ($\sim 179\mu A/V$) mostly due to the lower mobility of holes compared to electrons. However, the current driving capability of device 1 as a SF is already high enough to meet the high-speed operation requirements in QIS application based on our empirical data, so higher g_m may not be needed.

According to Eq. 3, a larger channel depth h or higher doping factor β leads to higher pinch-off voltage V_p, which weakens the control of the gate on the channel current. It is presented as a lower normalized g_m as depicted in Fig. 8(b).

E. DEVICE DESIGN DISCUSSION

This JFET device works as a SF, so the parameters must be well engineered to meet requirements from other components in the jot device. For instance, the bias voltages range is determined by,

$$\begin{cases} V_g = V_{FD} \\ V_S = V_{out} \\ V_D = 0 \end{cases} \tag{30}$$

where the FD potential V_{FD} is determined by,

$$V_{RST} - (CG \times FWC) \le V_{FD} \le V_{RST} \tag{31}$$

and V_{RST} is the FD potential after reset. As presented in Eq. 3, to make the JFET SF work in saturation mode, the following condition must be satisfied,

$$V_{RST} - (CG \times FWC) \ge V_p - V_{bi} \tag{32}$$

In a jot device with a conventional reset transistor, V_{RST} is flexible and can be adjusted according to the working range of the JFET SF. In a device with punch-through reset, V_{rst} is normally confined to a certain range, and the design of the JFET needs to accommodate these constraints, whereby V_p and V_{bi} have to be engineered accordingly to have enough FWC. The maximum FWC is given by:

$$FWC_{max} = \frac{V_{RST} - V_p + V_{bi}}{CG} \tag{33}$$

The source follows the FD potential, and the output range is determined by the bias current and the I-V characteristics of the JFET.

IV. PUNCH-THROUGH RESET

The punch-through reset technique was proposed to improve reset speed [30], and used in [15] to reduce the parasitic capacitance from the reset gate. In [15], for example, the punch-through reset voltage was over 20V. One of the goals in our design was to reduce the voltage required for reset.

The punch-through reset process relies on the fringing effect induced by a strong lateral electric field in a NPN junction. As shown in Fig. 2, FD and RD are separated by a p-type region, which creates a potential barrier between the two n-type regions. During the reset state, RD is biased to a higher level V_{RDHI}, e.g., V_{DD}. In this case, the p-type region is fully depleted by RD, and the strong lateral electric field between FD and RD forces the potential in the p-region to increase. As shown in Fig. 10(a), the potential barrier between FD and RD is reduced with increased V_{RD}. Electrons start to flow from FD to RD once the potential barrier has been lowered, as depicted in Fig. 11(a). Meanwhile, FD is discharged and V_{FD} increases until the RD-FD electric field is too weak to maintain punch-through. The FD voltage after the reset V_{RST} depends on the bias V_{RDHI} during the reset and the reset pulse duration. After the reset, bias V_{RD} is reduced to V_{RDLO} and the potential barrier V_B is restored to stop electron current, as shown in Fig. 10(b). During the "off" state, in order to have a solid barrier on both FD and RD ends, V_{RD} needs to be equal to, or near V_{RST}, as shown by the green curve in Fig. 10(b). The maximum potential barrier height depends on the doping in the p-type region and its width. It is a tradeoff that a higher potential barrier

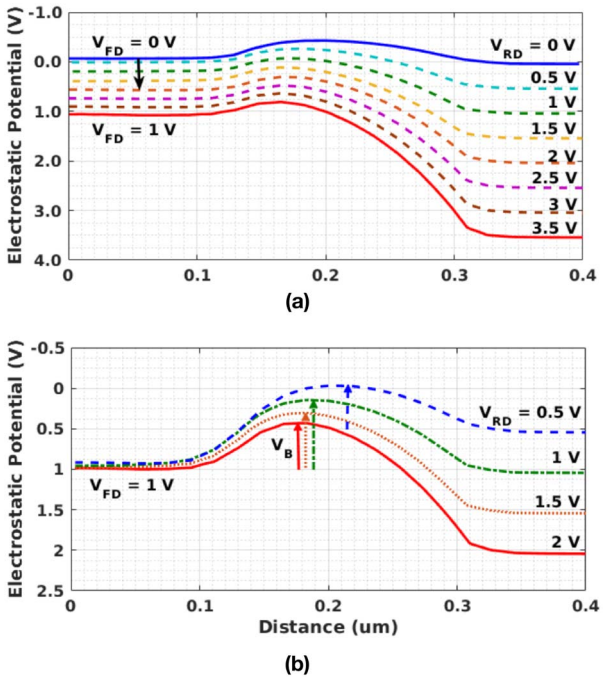


FIGURE 10. **FD (left) to RD (right) electrostatic potential profile from TCAD simulation. Cutline is illustrated in Fig. 11. (a) Potential profile during punch-through reset with different V_{RD}. V_{FD} after reset changes accordingly. (b) Potential profile after reset, with $V_{FD} = 1V$. The height of potential barrier changes with different V_{RD}.**

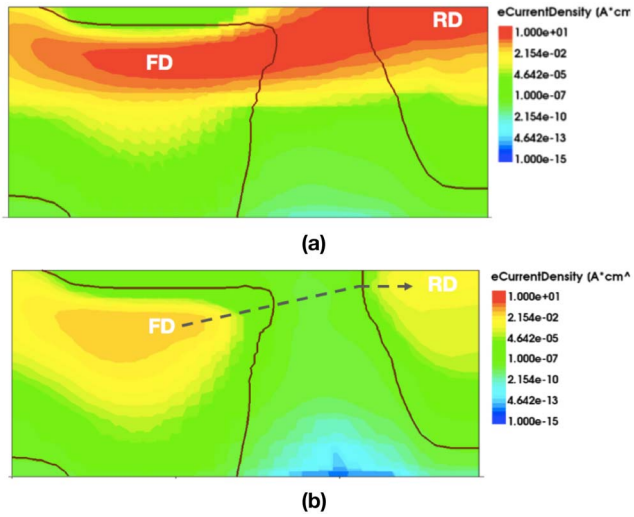


FIGURE 11. **FD (left) to RD (right) electron current density profile from TCAD simulation. (a) Electron current density during punch-through reset with $V_{RD} = 2.5V$. (b) Electron current density after reset, with $V_{RD} = 1V$.**

after reset will also limit the highest reset voltage FD can reach during reset. In the case of device 1, FD can be reset to 1V with V_{RDHI} of 3V, and after reset V_B is about 0.9V with V_{RDLO} of 1V. In this case, the barrier is strong enough to stop electrons exchange between RD and FD, as depicted in Fig. 11(b). According to Eq. 33 the maximum FWC is 824 e-, which is relatively small for conventional CIS, but

TABLE 1. **Parameters of JFET devices.**

Symbol	Quantity	**Device 1**	Device 2
N_d	Gate Doping Concentration	$8.7e17\ cm^{-3}$	$1.35e18\ cm^{-3}$
N_a	Channel Doping Concentration	$1.41e18\ cm^{-3}$	$1.7e18\ cm^{-3}$
N_{ad}	Drain Doping Concentration	$1e20\ cm^{-3}$	$1e20\ cm^{-3}$
v_s	Hole Saturation Velocity in Si	$8.3e6\ cm/s$	$8.3e6\ cm/s$
μ_p	Low-field hole mobility	$85\ cm^2/(V \cdot S)$	$76\ cm^2/(V \cdot S)$
L	Channel Length	$0.15\ \mu m$	$0.15\ \mu m$
W	Channel Width	$0.2\ \mu m$	$0.2\ \mu m$
h	Channel Depth	$0.02\ \mu m$	$0.025\ \mu m$
V_p	Pinch-off Voltage	$1.11\ V$	$1.83\ V$
V_{bi}	Gate-Channel Built-in Voltage	$0.94\ V$	$0.95\ V$
V_{bi2}	Gate-Drain Built-in Voltage	$1.05\ V$	$1.06\ V$
g_0	Unit Transconductance	$51.1\ \mu A/V$	$69.5\ \mu A/V$
V_{RDLO}	Punch-through reset "off" voltage	0.8-1.5V	NA
V_{RDHI}	Punch-through reset "on" voltage	2.5-3.3V	NA

enough for QIS applications. For conventional CIS, a higher V_{RDHI} might be necessary as suggested in [15].

V. ENTIRE JOT DEVICE SIMULATION

A 3D device simulation for the JFET jot was executed with all components. The timing of the control signals is depicted in Fig. 12. The drain of the SF is connected to ground, and the source is connected to a current source with a $1\mu A$ bias current. V_{DD} is 2.5V. The punch-through reset signal has a pulse width of 100nsec. The "off" state and "on" state RD voltages are set to 1V and 2.5V. The TG transfer signal has a pulse width of 50nsec, and the TG "off" voltage is -0.5V and the TG "on" voltage is 2.5V. The FWC of the SW is about 200e-, and in the simulation 45 photoelectrons were collected by the SW during integration. After the punch-through reset, FD has a reset voltage of 0.77V, and the source output is at 0.72V, which yields $V_{GS} = 0.05V$. During charge transfer, the 45 electrons are completely transferred from SW to FD, and no lag is observed. The change of V_{FD}

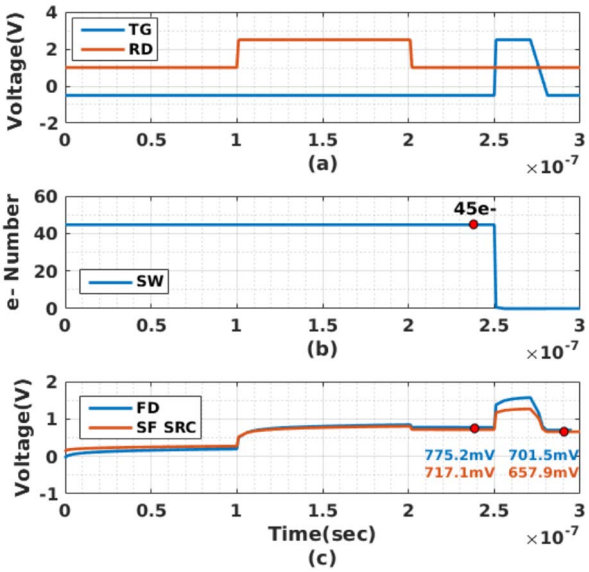


FIGURE 12. Results of entire jot device simulation. (a) Timing of control signal TG and RD. (b) Electron number in SW. (c) Output of SF source.

induced by transferred charge is equal to 73.7mV, which yields an input-referred CG of 1.64mV/e- before the in-jot SF. This corresponds to a 0.1fF total FD capacitance which matches the analytic calculation result. The voltage change at the source of the SF is equal to 59.2mV, which yields an output-referred CG of 1.32mV/e- and a gain of 0.8 from the JFET SF.

VI. CONCLUSION

To realize highly accurate photoelectron counting for QIS applications, read noise needs to be reduced to 0.15e- r.m.s. or lower. Significant progress has been made to reduce the read noise of jot devices to 0.22e- r.m.s. and into the DSERN regime, but further reduction of read noise is facing a dilemma between improving CG and increasing 1/f noise due to smaller SF area size. In this paper, a new jot device with a JFET SF is introduced. Compared to a MOSFET SF, it can reduce the parasitic capacitance added to FD capacitance and greatly improve the CG. Simulation of this device shows an output-referred CG of 1.32mV/e. Together with the relatively low 1/*f* noise from JFET devices, this device is promising for both a proof-of-concept demonstration and future commercial QIS applications. The device is designed with the Synopsys TCAD simulation tools in a 45nm BSI process. Both simulation results and theoretical analysis are presented. The device will be fabricated in the coming year and characterization results will be reported.

ACKNOWLEDGMENT

The authors appreciate the useful discussion and technical assistance from other members of our group at Dartmouth, especially D. Hondongwa, D. Starkey, and L. Anzagira.

REFERENCES

[1] E. R. Fossum, "What to do with sub-diffraction-limit (SDL) pixels?—A proposal for a gigapixel digital film sensor (DFS)," in *Proc. IEEE Workshop CCDs Adv. Imag. Sensors*, Nagano, Japan, Sep. 2005, pp. 214–217.

[2] E. R. Fossum, "The quanta image sensor (QIS): Concepts and challenges," in *Proc. Opt. Soc. America Topical Meeting Comput. Opt. Sens. Imag.*, Toronto, ON, Canada, Jul. 2011.

[3] S. Masoodian, A. Rao, J. Ma, K. Odame, and E. R. Fossum, "A 2.5 pJ/b binary image sensor as a pathfinder for quanta image sensors," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 100–105, Jan. 2016.

[4] E. R. Fossum, "Modeling the performance of single-bit and multi-bit quanta image sensors," *IEEE J. Electron Devices Soc.*, vol. 1, no. 9, pp. 166–174, Sep. 2013.

[5] R. Zizza, "Jots to pixels: Image formation options for the quanta image sensor," M.S. thesis, Thayer School Eng., Dartmouth College, Hanover, NH, USA, 2015.

[6] S. Chen, A. Ceballos, and E. R. Fossum, "Digital integration sensor," in *Proc. Int. Image Sensor Workshop*, Jun. 2013.

[7] L. Anzagira and E. R. Fossum, "Application of the quanta image sensor concept to linear polarization imaging-a theoretical study," *J. Opt. Soc. America A*, vol. 33, no. 6, pp. 1147–1154, 2016.

[8] E. Amri, Y. Felk, D. Stucki, J. Ma, and E. R. Fossum, "Quantum random number generation using a quanta image sensor," *MDPI Sensors J.*, vol. 16, no. 7, p. 1002, Jun. 2016, doi: 10.3390/s16071002.

[9] E. R. Fossum, "Photon counting error rates in single-bit and multi-bit quanta image sensors," *IEEE J. Electron Devices Soc.*, vol. 4, no. 3, pp. 136–143. May 2016.

[10] M. J. Uren, D. J. Day, and M. J. Kirton, "1/f and random telegraph noise in silicon metal−oxide−semiconductor field−effect transistors," *Appl. Phys. Lett.*, vol. 47, no. 11, pp. 1195–1197, Dec. 1985.

[11] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654–665, Mar. 1990.

[12] R. W. Brodersen and S. P. Emmons, "Noise in buried channel charge-coupled devices," *IEEE Trans. Electron Devices*, vol. 23, no. 2, pp. 215–223, Feb. 1976.

[13] X. Wang, M. F. Snoeij, P. R. Rao, A. Mierop, and A. J. P. Theuwissen, "A CMOS image sensor with a buried-channel source follower," in *IEEE Int. Solid State Circuits Conf. (ISSCC) Tech. Dig.*, San Francisco, CA, USA, Feb. 2008, pp. 62–63.

[14] Y. Chen *et al.*, "A 0.7e^- rms-temporal-readout-noise CMOS image sensor for low-light-level imaging," in *Proc. IEEE Int. Solid State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, Feb. 2012, pp. 384–386.

[15] M.-W. Seo, S. Kawahito, K. Kagawa, and K. Yasutomi, "A 0.27e^-_{rms} read noise 220-μV/e^- conversion gain reset-gate-less CMOS image sensor with 0.11-μm CIS process," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1344–1347, Dec. 2015.

[16] M. Guidash, Private communication, Mar. 2016.

[17] M. Guidash, J. Ma, T. Vogelsang, and J. Endsley, "Reduction of CMOS image sensor read noise to enable photon counting," *MDPI Sensors*, vol. 16, no. 4, p. E517, Apr. 2016.

[18] J. Hynecek, "Impactron-a new solid state image intensifier," *IEEE Trans. Electron Devices*, vol. 48, no. 10, pp. 2238–2241, Oct. 2001.

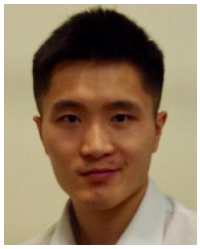
[19] B. F. Aull *et al.*, "Geiger-mode avalanche photodiodes for three-dimensional imaging," *Lincoln Lab. J.*, vol. 13, no. 2, pp. 335–350, Nov. 2002.

[20] M. Mori *et al.*, "6.6 A 1280×720 single-photon-detecting image sensor with 100dB dynamic range using a sensitivity-boosting technique," in *Proc. IEEE Int. Solid State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, Feb. 2016, pp. 120–121.

[21] J. Ma and E. R. Fossum, "A pump-gate jot device with high conversion gain for a quanta image sensor," *IEEE J. Electron Devices Soc.*, vol. 3, no. 2, pp. 73–77, Mar. 2015.

[22] J. Ma and E. R. Fossum, "Quanta image sensor jot with sub 0.3e- r.m.s. read noise and photon counting capability," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 926–928, Sep. 2015.

[23] J. Ma, D. Starkey, A. Rao, K. Odame, and E. R. Fossum, "Characterization of quanta image sensor pump-gate jots with deep sub-electron read noise," *IEEE J. Electron Devices Soc.*, vol. 3, no. 6, pp. 472–480, Nov. 2015.
[24] J. Hynecek, "Vertical JFET source follower for small pixel CMOS image sensors," U.S. Patent 8 937 272 B2, Jan. 20, 2015.
[25] H. Nomura, T. Shima, A. Kamashita, T. Ishida, and T. Yoneyama, "A 256/spl times/256 BCAST motion detector with simultaneous video output," in *IEEE Int. Solid State Circuits Conf. (ISSCC) Tech. Dig.*, San Francisco, CA, USA, Feb. 1998, pp. 282–283.
[26] S. M. Sze, "JFET and MESFET," in *Physics of Semiconductor Devices*, 2nd ed. New York, NY, USA: Wiley, 1981, ch. 6, pp. 312–362.
[27] U. K. Mishra and J. Singh, "Field effect transistors," in *Semiconductor Device Physics and Design*, 1st ed. Dordrecht, The Netherlands: Springer, 2008, ch. 8, pp. 356–432.
[28] J. Chang, A. K. Kapoor, L. F. Register, and S. K. Banerjee, "Analytical model of short-channel double-gate JFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 8, pp. 1846–1855, Aug. 2010.
[29] Y. Hu, R. V. H. Booth, and M. V. White, "An analytical model for the lateral channel electric field in LDD structures," *IEEE Trans. Electron Devices.*, vol. 37, no. 10, pp. 2254–2264, Oct. 1990.
[30] R. M. Guidash, "Solid state image sensor with fast reset," U.S. Patent 5 338 946 A, Aug. 16, 1994.



JIAJU MA (S'12) received the B.S. degree in physics from Nankai University, China, in 2012. He is currently pursuing the Ph.D. degree with the Thayer School of Engineering at Dartmouth. He is exploring low-noise CMOS image sensor pixel devices for quanta image sensor and other photon-counting imaging applications.

ERIC R. FOSSUM (S'80–M'84–SM'91–F'98) is currently a Professor with the Thayer School of Engineering, Dartmouth. He is the Primary Inventor of the CMOS image sensor used in billions of camera phones and other applications. He was inducted into the National Inventors Hall of Fame and a member of the National Academy of Engineering. He is the Co-Founder and the Past President of the International Image Sensor Society and the Director of the National Academy of Inventors. He is currently exploring the quanta image sensor.