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A Pump-Gate Jot Device With High Conversion Gain for a Quanta Image Sensor

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ABSTRACT A new photodetector designed for Quanta image sensor application is proposed. The photodetector is a backside-illuminated, buried photodiode with a vertically integrated pump and transfer gate and a distal floating diffusion to reduce parasitic capacitance. The structure features compact layout and high conversion gain. The proposed device is modeled and simulated, and its performance characteristics estimated.

INDEX TERMS CMOS image sensor, Quanta image sensor (QIS), jot, pump gate, full well capacity, high conversion gain.

I. INTRODUCTION

THE QUANTA Image Sensor (QIS) has been proposed as a possible next-generation image sensor [1], [2]. Both single-bit and multi-bit QIS devices show interesting imaging properties [3]. In the QIS concept, the specialized, sub-diffraction-limit (SDL) sized binary-output photoelement sensitive to a single photoelectron is called a “jot.” An output image pixel is created from a neighborhood of jot signals in space and time.

Central to QIS implementation is single-electron sensitivity ($\sim 0.15e^-$ r.m.s.) which can be obtained from high, in-pixel conversion gain, e.g., more than $1000\mu V/e^-$. In addition to small size (e.g., less than 500nm pitch) jots should also be able to function at low supply voltages. In single-bit QIS devices, full-well capacity (FWC) of only $1e^-$ is required, and in multi-bit QIS devices, FWC of perhaps $100e^-$ is sufficient. State-of-the-art CMOS image sensors (CIS) using pinned photodiodes (PPDs) [4] typically have read noise of about $2e^-$ r.m.s., conversion gain of about $100\mu V/e^-$, pixel pitch of greater than $1\mu\text{m}$, full-well capacity (FWC) of at least several thousand electrons, and are thus not presently well-suited for QIS application. Recently a single-photoelectron avalanche diode (SPAD) $8\mu\text{m}$ pitch “jot” was used to demonstrate a 320×240 element QIS-like device with interesting results [5], but SPADs are not anticipated to scale well to sub-diffraction limit pitch nor be manufacturable in the multi-megajot to

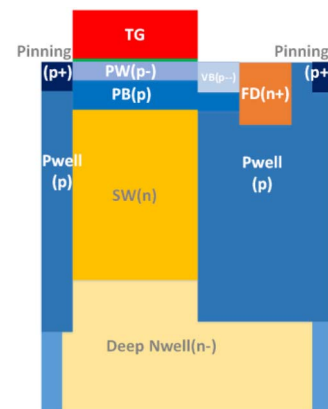


FIGURE 1. Schematic of pump-gate jot doping.

gigajot array size in the near future as needed for QIS application [6].

There is a significant worldwide effort in the shrinking of CIS pixels to reduce optics and camera size for the same resolution, and/or to increase pixel count at the same sensor size. During shrink, great effort is made to maintain FWC of perhaps $3000e^-$ or more so that dynamic range and signal-to-noise ratio (SNR) do not suffer. The capacity is required in the storage well (SW), floating diffusion (FD) and read-out signal chain. In CIS PPD pixels, after signal integration photoelectrons in the storage well are completely transferred

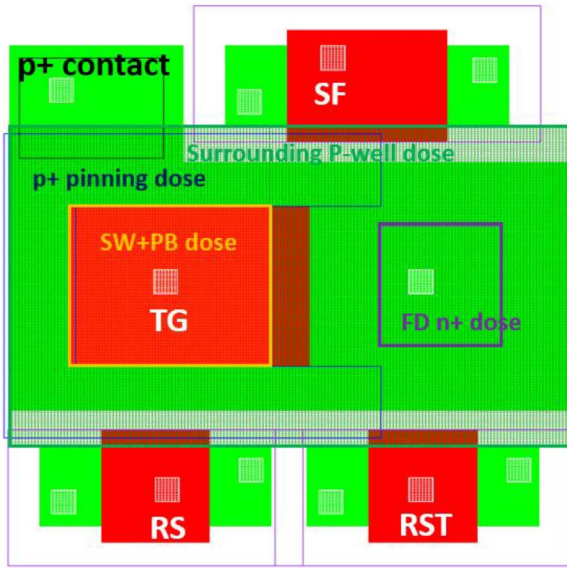


FIGURE 2. 1.4 μm -pitch pump-gate jot layout, not including isolation deep p -well masks and metal layers. The SW and PB masks are totally underneath TG.

via transfer gate (TG) to the FD node for charge-to-voltage conversion. The change in voltage on the FD is buffered by an in-pixel source-follower transistor circuit. The conversion gain and capacity depend on the capacitance of the FD node and its reset voltage. Low read-noise and no lag using complete charge-transfer and correlated double sampling (CDS) are useful in the jot, and adapting technology developed for CIS pixels is sensible in creating the QIS jot devices, speeding development and reducing barriers for adoption.

In a CIS PPD pixel, the capacitance of the FD node consists of 5 main parts: the diffusion capacitance of FD; the diffusion capacitance of the source of the reset transistor (if it is connected by wires to the FD); the overlap capacitance between FD and TG; the overlap capacitance between the reset gate (RG) and FD; and the effective gate capacitance of the source follower. For the high conversion gain needed for the QIS, the capacitance of the FD needs to be minimized. Advanced CMOS process enables smaller feature size which helps decrease FD capacitance, especially for the diffusion capacitance and the source-follower gate capacitance. Smaller feature size also decreases the overlap capacitance, but increases its proportion in FD total capacitance. In CIS devices made with the latest CMOS technology, overlap capacitance contributes around 50% of the total capacitance, and this percentage will likely increase as feature sizes are scaled down.

In this paper, we introduce a QIS jot device which has several important features. First, a distal FD is implemented to reduce the overlap capacitance between FD and TG. Second, a “pump-action” transfer gate is introduced to realize complete charge transfer with the distal FD. Third, the reset gate is tapered to reduce the overlap capacitance between RD and TG. According to layout and TCAD simulation,

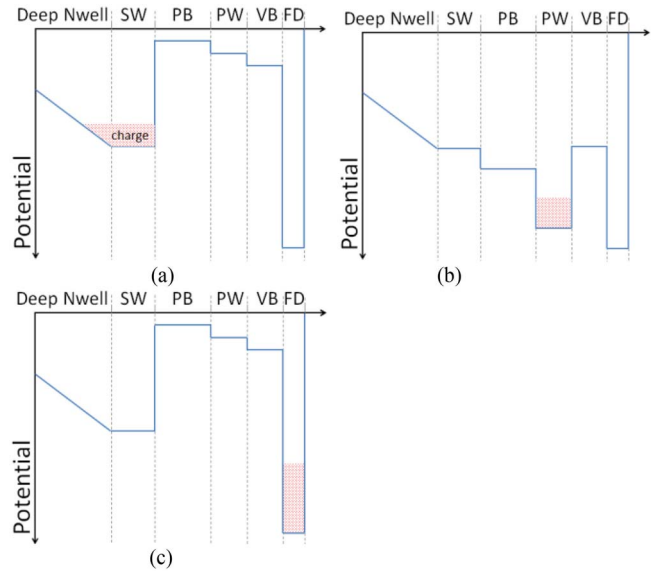


FIGURE 3. Pump action idealized charge transfer diagram. (a) Photoelectrons are collected in SW. (b) First step of the “pump” action transfer. TG is ON and photoelectrons are transferred to PW. (c) Second step of the pump action transfer. TG is OFF and photoelectrons are transferred to FD.

the proposed pump-gate jot implemented in 65nm BSI CIS technology has a full-well capacity of 200e⁻ and conversion gain of 380 $\mu\text{V}/\text{e}^-$.

II. CONCEPT

The proposed pump-gate jot is similar to CIS pixels but with several differences as described above. Like some recent BSI CIS pixels, the carriers are stored under the transfer gate (TG) to reduce jot area [7], [8]. Unlike these devices, complete

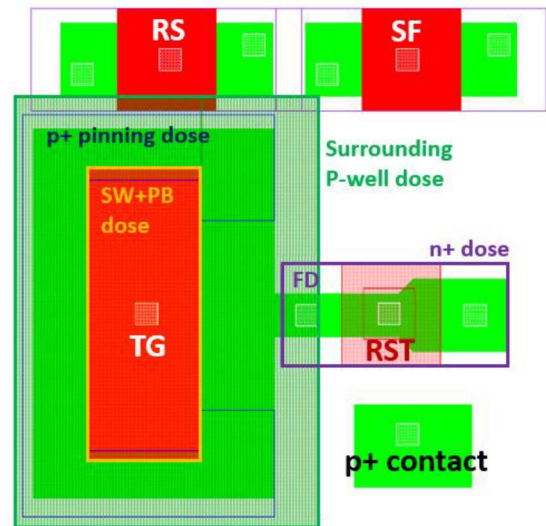


FIGURE 4. 1.4 μm -pitch pump-gate jot with tapered RST layout, not including isolation deep p -well masks and metal layers. The tapered Diff layer is shown underneath RST.



FIGURE 5. 1 μm -pitch, pump-gate jot with four-way shared readout layout, not including deep p-well masks and metal layers. The shape of TGs are optimized to avoid possible potential barrier due to 3-D effects.

transfer of charge takes two discrete steps: (a) a vertical transfer upwards to surface under TG, followed by (b) a lateral transfer over the “virtual phase” barrier (VB) between TG and FD. The two steps constitute the “pump action” of the charge transfer – similar to a technique used in two phase CCDs [9] and more recently in a global-shutter CIS [10], although these examples use lateral transfer only.

The structure of the pump-gate jot is depicted in Fig. 1. An n-type SW photodiode well is formed underneath the transfer gate, surrounded by a p-type doped well. On the top of SW, there are two p-type doped regions PB and PW, with PW more lightly doped than PB so that when TG is biased by a flat-band voltage, the potential of PW is higher than PB. Between PW and the distal FD is the p-type doped virtual-phase potential barrier (VB). It is more lightly doped than PW. Together they form a double-step potential profile. The p+ pinning layer on the side of TG helps quench surface-generated dark current.

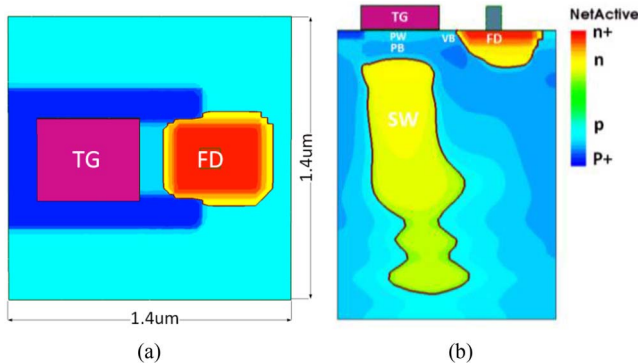


FIGURE 6. Simulated doping profile of pump-gate jot. (a) Top-view. (b) Cut-plane.

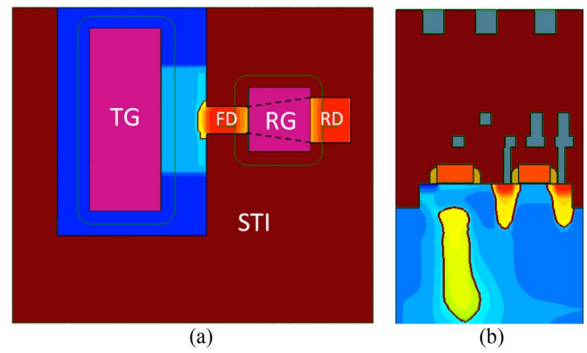


FIGURE 7. Pump-gate jot with tapered RG in TCAD simulation. (a) Top-view. (b) Cut-plane.

The layout of the 1.4 μm -pitch non-shared readout pump-gate jot is depicted in Fig. 2. An idealized charge transfer diagram is depicted in Fig. 3. During integration, TG is “off” and photoelectrons are collected in SW. After integration, TG is positively biased (“on”), and carriers are vertically transferred from SW to PW. This is the first step of the pump-action charge transfer. VB is in depletion mode and forms a virtual barrier between PW and FD. When TG is turned off, the potential of PW returns to the initial level. As soon as the potential of PW becomes lower than VB, charge in PW will flow over VB into the distal FD. Meanwhile, because of the doping concentration and its location, PB always has a lower potential than PW, which prevents charge from flowing back to SW. Thus, by a two-step “pump” action, complete charge transfer from SW to FD can be achieved with low TG overlap capacitance.

A tapered gate reset transistor is proposed to further reduce the total capacitance of FD. The layout of the 1.4 μm -pitch pump-gate jot with tapered RST is depicted in Fig. 4. The minimum area of the distal FD is limited by the smallest size of photoresist window. A tapered STI is used to constrain the size of the distal FD and its overlap width with the reset gate. Although STI will increase the sidewall capacitance of FD, overall the total capacitance can be reduced and higher conversion gain can be achieved. Since the channel width is wider on the reset drain side, due to 3D effects, carriers will tend to flow to RD rather than FD when the reset gate is on, which may reduce partition noise.

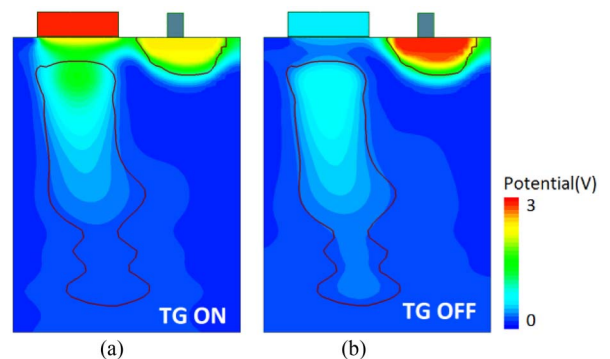


FIGURE 8. Potential in pump-gate jot for (a) TG ON and (b) TG OFF.

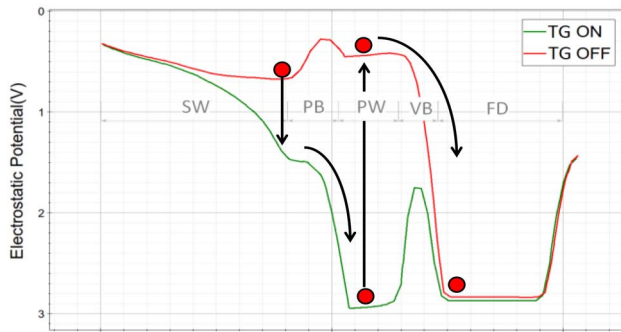


FIGURE 9. Simulated potential profile along charge transfer path for both TG ON and OFF.

Additional jot-area savings comes with 2-way or 4-way shared readout as is commonly used in CIS pixels. With the distal FD, the additional TG gates do not increase FD capacitance due to overlap. The four jots are covered by a single color filter and micro lens. Such a microlens might be implemented with a center dimple to avoid guiding rays to the FD. With such SDL jots, it is not critical which of the four adjacent jots photoelectrons randomly enter, provided they are not lost to FD. A deep p-type doping well is used surrounding four adjacent jots for isolation and photoelectron deflection from FD. Layout of a 4-way shared jot with $1\mu\text{m}$ pitch is shown in Fig. 5, in which the shapes of the transfer gates and storage wells are optimized to avoid any potential barrier to transfer created by 3D effects.

III. SIMULATION RESULTS AND PERFORMANCE ESTIMATION

A. DOPING PROFILE AND FABRICATION PROCESS

Using 3D TCAD tools, the proposed device was simulated using the TSMC 65 nm node BSI CIS process as a baseline. Using an existing commercial process as a baseline is important for possible technology adoption and risk mitigation.

The fabrication follows the standard BSI CIS process and does not increase mask count. The simulated doping profiles are shown in Figs. 6 and 7. The implants of SW were adjusted for expected full well, and various combinations of

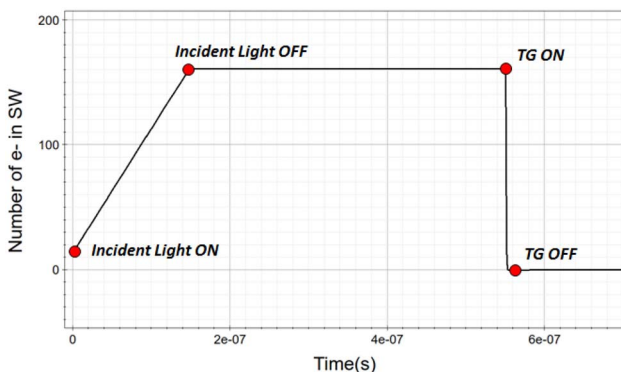


FIGURE 10. Transient simulation result showing photoelectrons collection and transfer in SW.

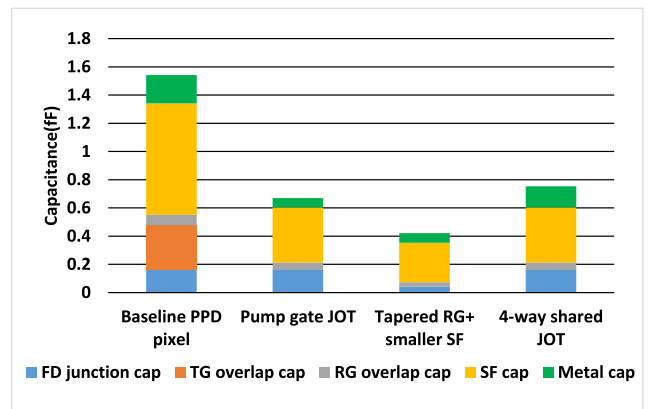


FIGURE 11. Comparison of FD capacitance components in different pixels or jots.

implant conditions were tested to realize the expected doping profile. The fabrication follows the standard BSI CIS process and does not increase mask count. The formation of the deep SW n-well and its surrounding p-well is similar to conventional BSI pinned photodiodes. Since a lower pinning voltage helps charge transfer and since small FWC is acceptable, the dose of n-type implants was modified. PB is implemented beneath TG with one p-type implant, and PW and VB are implemented with one n-type implant with relatively lower dose and energy. To realize a distal FD, the n+ implants mask for FD has no overlap with TG poly.

B. POTENTIAL PROFILE

The simulated potential profile is shown in Fig. 8 for cases of TG on and off. The full well is about $200e^-$ and V_{pin} is around 0.7V . The doping and depth of PW and PB are critical to ensure a complete transfer of charge in SW. The doping of PB must be high enough to implement a potential barrier between PW and SW to avoid backward injection of carriers from PW to SW during transfer. As the simulated potential profile shows in Fig. 9, when the TG is on, the potential along transferred photoelectron path increases nearly monotonically (barrier shown is under 50mV), and collected carriers are transferred completely to PW. Meanwhile the VB region forms a potential barrier between PW and FD. When TG is turned off, the potential of PW recovers to the initial level, and charge flows over VB to FD, and the pump-action transfer is completed.

C. CHARGE TRANSFER

The result of a transient simulation is depicted in Fig. 10. It shows complete charge transfer without back injection of signal charge. Note that the simulation does not reflect the discrete nature of photoelectron generation. Because of the small full well and physically smaller SW, fast charge transfer can be achieved and the possibility for lag caused by slow transfer is reduced. The saturated SW is completely transferred within 20ns . Compared to CIS pixels, the readout time of the pump-gate jot is greatly shortened. The distal FD design also reduces clock feedthrough to the column

bus when TG is pulsed so that shorter row time and CDS time might be achieved with this device, and lower readout noise is anticipated. Faster transfer may also decrease photoelectron trapping at the surface. This is important for the “photoelectron counting” jot and needs to be verified with experimental devices.

D. CONVERSION GAIN

Both the pump-gate jots (with and without tapered gate reset transistor) were simulated and compared. In Fig. 11, a chart of FD capacitance components shows the magnitude of components calculated from process data sheet, and the calculated capacitance match the simulation results very well. Also for comparison, a pixel with the same process and 4-way shared readout, was found to have a conversion gain of $103\mu\text{V}/e^-$. As expected, due to the reduction of TG overlap capacitance, the pump-gate jot with distal FD has a higher conversion gain of $238\mu\text{V}/e^-$. The pump-gate jot with distal FD, tapered RG and smaller SF has the highest conversion gain of $380\mu\text{V}/e^-$ because of the further reduction of FD area size and RG overlap. The 4-way shared pump-gate jot has a higher metal capacitance due to a more compact layout, and it has a conversion gain of $212\mu\text{V}/e^-$.

IV. CONCLUSION

A novel jot device modified from a conventional CIS pixel is described. It is designed for QIS and other new imaging systems which target high conversion gain to enable photoelectron counting and which need only limited FWC. The major innovations involve the distal FD, the “pump” action transfer gate, and tapered reset gate which together result in reduced FD capacitance and high conversion gain. Devices were designed in TSMC 65nm CIS process and are being fabricated. The pump-gate jot with non-shared readout has $1.4\mu\text{m}$ pitch, and the 4-way shared pump-gate jot has $1\mu\text{m}$ pitch.

While our results are based on TCAD simulations thus far, we believe the concepts of the distal FD and tapered-reset gate are robust and applicable to devices beyond the scope of the QIS. Other layouts for reducing RG-FD overlap capacitance are possible. Certainly shrink of the SF is a risk item due to the relationship between gate area, $1/f$ noise, and drive capability. While TCAD simulation is generally quite good at predicting device operation, small adjustments to implant parameters may be required to achieve the desired performance. Estimation of capacitances need to be verified in experimental devices. Further shrink of both unshared and 4-way shared devices in the same process is possible.

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USA, where he invented the CMOS active pixel sensor camera-on-a-chip technology, which is currently used in billions of camera phones, webcams, DSLRs, and other applications. In 1995, he co-founded Photobit Corporation to commercialize the technology and served in several top management roles, including the Chief Executive Officer (CEO). From 2005 to 2007, he was the CEO of Siimpel Corporation, developing camera modules with MEMS-based autofocus and shutter functions for cell phones. From 2008 to 2013, he was a Consultant with Samsung Electronics engaged in various projects including 3-D RGBZ ranging image sensors. Since 2010, he has been a Professor with the Thayer School of Engineering, Dartmouth College, Hanover, NH, USA, and Director of the Ph.D. Innovation Program. He co-founded the International Image Sensor Society (IISS) and served as the President until 2013. He has published over 270 technical papers and holds over 150 U.S. patents. He was the recipient of several awards, including the NASA Exceptional Achievement Medal and the IEEE Andrew S. Grove Award. He was the Guest Editor-in-Chief for the IEEE TRANSACTIONS ON ELECTRON DEVICES special issues on Solid-State Image Sensors in 1997, 2003, and 2009. He is a Charter Fellow of the National Academy of Inventors, and a member of the National Academy of Engineering. In 2011, he was inducted into the National Inventors Hall of Fame.