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Characterization of Quanta Image Sensor Pump-Gate Jots With Deep Sub-Electron Read Noise

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ABSTRACT Characterization of quanta image sensor pixels with deep sub-electron read noise is reported. Pixels with conversion gain of 423μV/e- and read noise as low as 0.22e- r.m.s. were measured. Dark current is 0.1e-/s at room temperature, and lag less than 0.1e-. This is one of the first works reporting detailed characterization of image sensor pixels with mean signals from sub-electron (0.25e-) to a few electrons level. Such pixels in a nearly-conventional CMOS image sensor process will allow realization of photon-counting image sensors for a variety of applications.

INDEX TERMS CMOS image sensor, quanta image sensor, jot device, photon counting, high conversion gain, low read noise, low dark current.

I. INTRODUCTION

The Quanta Image Sensor (QIS) is defined as a CMOS image sensor containing a large number of specialized pixels called jots, where all jots have photon counting capability and where each output image pixel is ultimately formed from a "cubicle" of jots [1]–[3]. For many QIS applications, an ideal jot should be sub-diffraction limit in pitch, perhaps 500nm or less, and have a full-well capacity of 1e- to ∼100e-. According to one theoretical model [4], besides high quantum efficiency, to achieve photon counting the read noise needs to be less than 0.3e- r.m.s., though the model of [2] suggests a read noise less than 0.15e- r.m.s. is ultimately desired. Noise below 0.5e- r.m.s., where single photoelectron detection becomes possible, is referred to as the deep sub-electron read noise regime.

Nearly all CMOS image sensors have an in-pixel source-follower (SF) transistor. In low read-noise devices, the SF output voltage noise currently dominates the pixel's read noise, typically about 1-2e- r.m.s. (input referred) in most commercial devices, and below 1e- r.m.s. in some scientific and experimental devices. Gain can be provided prior to the SF to boost the voltage signal from a single photoelectron above the voltage-noise of the SF.

One gain mechanism that has been used in CCDs and recently used in a CMOS image sensor is avalanche multiplication [5]–[7]. Single-photon avalanche diode (SPAD) arrays of 8μm pitch were used to demonstrate QIS devices [8], [9]. However, SPAD arrays are not anticipated to scale well to the sub-diffraction-limit pitch needed for reasonable flux capacity [10], nor be manufacturable in the multi-megajot to gigajot array size in the near future as needed for QIS applications.

Deep sub-electron noise has been achieved by non-destructive readout and summing hundreds or thousands of reads without avalanche under cooled conditions [11], [12]. Dark current limits the maximum number of useful reads. However, a non-destructive readout approach is not feasible for QIS application due to low temperature requirements, slow net readout speed and large pixel pitch.

Reducing the noise of the source-follower and subsequent electronics is also an approach to achieve deep sub-electron read noise. Use of PMOS for the source-follower has very recently allowed low noise [13] and limited photon-counting

capability at low temperature [14]. The lower speed of PMOS transistors is a concern for QIS application.

Another way to achieve deep sub-electron read noise is to reduce the capacitance of the floating diffusion (FD) sense node in the pixel. There is usually some tension between the resultant conversion gain (CG) and the full-well capacity of the sensor, since high conversion gain means voltage rail limits or other limits are encountered for fewer photoelectrons. In the digital integration sensor [15] and QIS concepts, loss in full-well capacity is compensated by higher frame or field readout rate and digital integration of the signal.

An approach for increasing CG to the 200-400μV/e- range in a pump-gate jot implemented in a 65nm BSI CIS process was recently proposed by our group [16], [17]. Two techniques were used to reduce the FD capacitance, the "pump-gate" transfer gate with distal FD, and a tapered reset gate. Other approaches have also been recently proposed [18] to achieve 240μV/e- in a 180nm CIS process. The pump-gate jot is the first device to experimentally show photon-counting capability by a single correlated-double sampling (CDS) readout due to the reduction of read noise to below 0.3e- r.m.s. [19].

In this paper, which expands upon our previous letter [19], further electrical characterization of the pump-gate jot implemented in a 65nm BSI CIS process, and its design variations are reported. Quantum efficiency was not measured since it is expected to be similar to other BSI CIS devices fabricated in the same process, and our fab run did not include microlenses or color filter arrays. An available noise-reducing SF transistor mask was (inadvertently) not utilized so our SF devices are surface-channel, making the low-noise results of [19] more remarkable. Our main interests at this time are conversion gain, read noise, lag, dark current, and a rough idea of the scatter of those parameters. The best measured device (the "golden jot") showed conversion gain after the in-pixel SF of 423μV/e-, and read noise as low as 0.22e- r.m.s. at room temperature with a single CDS readout. Dark current is less than approximately 0.1e-/s at room temperature in the 1.4μm pitch devices.

II. REVIEW OF DEVICE CONCEPT

The pump-gate jot device is described in more detail in [16], [17], and [19] and is briefly reviewed here. In a conventional 4T pixel with a pinned photodiode [20], the capacitance of the FD consists of 5 major components: the junction capacitance of the FD, the overlap capacitance between the FD and the transfer gate (TG), the overlap capacitance between the FD and the reset gate (RG), the effective source follower (SF) gate capacitance and the inter-metal capacitance. The SF gate capacitance is related to its area, which is inversely related to 1/f noise [21]. The 1/f noise cannot be fully suppressed by CDS [22].

To reduce the FD capacitance, the pump-gate jots use an idea similar to the "virtual phase", which is well-known in CCDs, to create a specialized potential profile in the charge transfer path which enables a distal FD that has no overlap with the TG. The structure is shown in Fig. 1.

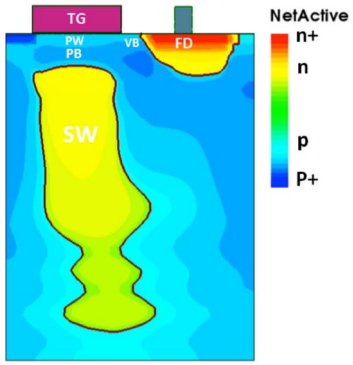

FIGURE 1. Cross-section doping profile of a pump-gate jot in the TCAD simulation from [17].

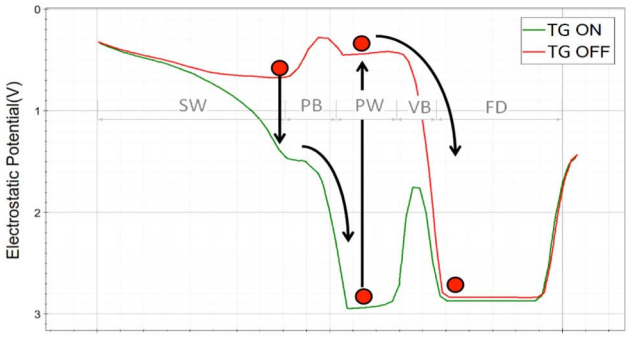

FIGURE 2. Simulated potential profile along the charge transfer path when TG is "on" and "off" from [17].

During the integration phase, the photoelectrons will accumulate in the storage well (SW) underneath the TG. When the TG is turned "on" by being pulsed to a positive voltage, the potential in the PB and the PW region will be increased, and there will be a monotonic potential increase from the SW to the PW, as shown in Fig. 2. The photoelectrons in the SW will flow to the PW. When the TG is turned "off", the potential in the PW and the PB will reduce and the photoelectrons will be "pumped" over the VB region to the FD. Because the PB region has a higher doping concentration than the PW, it creates a potential to prevent photoelectrons from flowing back to the SW when the TG is turned "off". With the pump-gate, a jot device can eliminate the overlap capacitance from the TG and still be able to achieve complete charge transfer.

To further improve CG, we employed a tapered reset gate [23]. The idea is to use shallow-trench isolation to taper the channel of the reset transistor on the FD side, so as to shrink the channel width and reduce the overlap capacitance between the FD and the RG. It also helps to reduce the junction capacitance of the FD, and the 3D effect caused by the gradient channel width is also anticipated to reduce the partition noise during the reset. Layout was shown in [17].

With these two techniques, both the pump-gate (PG) jots and the tapered pump-gate (TPG) jots have lower FD

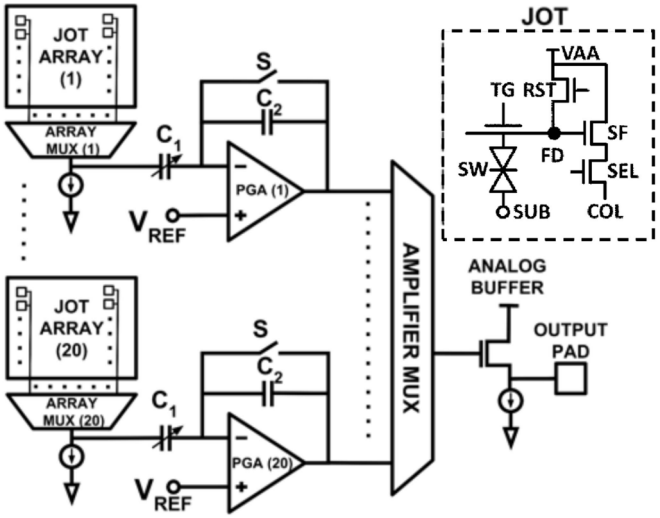

FIGURE 3. **Block diagram of the on-chip readout chain. A new symbol with TG MOS gate and PNP photodiode underneath has been used for the pump-gate photodetector. SUB is connected to ground in each jot.**

capacitance compared to a typical pinned-photodiode pixel, and thus higher conversion gain. Specifically, the TPG jots have the highest conversion gain because of the reduced RG overlap capacitance and a smaller SF area (WxL of 0.2 x 0.2μm compared to 0.2 x 0.4 μm for the PG jot).

III. READ OUT CHAIN DESIGN

A. ON CHIP

In the fabricated test chip, because of a severe limitation of layout space and number of pads available to us, a simple approach for the readout electronics was adopted. Twenty small 32x32 jot arrays with different variations were designed. Fig. 3 shows a block diagram of the on-chip readout signal chain. A single current-source bias at the bottom of the column array is multiplexed to the columns of each jot array. A switched-MOM-capacitor programmable gain amplifier (PGA) with gains of 8, 16 and 24 was implemented for each test array. A folded-cascode-topology amplifier with current, $I_{amp} = 5$ μA, is used to achieve an open-loop gain of 78dB and unity gain bandwidth of 60Mhz. The output-referred noise of the PGA is 100uV r.m.s., so that at a gain setting of 24, the input-referred noise is 4uV r.m.s. The output of the amplifiers are multiplexed into a single source-follower analog buffer, which drives the output pad. The analog buffer uses twice the current of the amplifier since it has to drive an output pad of capacitance ~0.8pF. Because the space and the number of pads was limited on the test chip, the bias current for jot arrays is designed to be hard wired to the amplifier current source with a fixed ratio $I_{col} = I_{amp}/12$, which is sufficiently large to overcome the parasitic capacitances, and the bandwidth is small to reduce the noise contribution. Cascode current mirrors are utilized to achieve accurate current ratios for the current sources of the column, amplifier and analog buffer.

Aside from enabling implementation of the test chip, this architecture has several drawbacks. First, only one jot per row can be readout, depending on which column is selected. This makes characterizing arrays tedious and limited the amount of data we could acquire on a practical basis. Second, exploring the effect of bias current on noise was difficult since the PGA would come out of optimum bias since its current bias was hardwired to that of each column.

B. OFF CHIP

An off-chip 14-bit ADC is used to perform digital CDS. Multiple samples of the reset level and then signal level are taken to reduce noise due to the off-chip electronics. With d.c. input, the noise of the off-chip electronics could be reduced by averaging multiple samples. With actual chip signals, it was found that increasing the number of samples beyond 10 of each did not further reduce noise, likely due to a concomitant increase in 1/f noise from the jot itself, and we concluded we were then jot-noise limited. With an improved board design with less board noise, we might be able to achieve lower measured jot noise if the jot noise is indeed 1/f-noise dominated.

The highest gain of the PGA is used to also help suppress the noise from off-chip components. Although it makes the useful input voltage swing limited, it is acceptable for the jot application since the required signal range is from one photoelectron to a few hundred photoelectrons, or a few tens of millivolts.

Calibration of the readout signal chain was performed using a test input pin to the on-chip PGA, with jot arrays deselected. A 14kHz square wave analog input signal of 80mV p-p was applied to the test input pin and the ADC output recorded. This procedure allowed calibration of DN/μV for each PGA gain setting from after the in-jot SF to the ADC. The PGA and analog buffer gain were calibrated by applying the test input signal to the ADC board, and by comparing to the first calibration.

IV. CHARACTERIZATION RESULTS

A. PHOTOELECTRON COUNTING HISTOGRAM

The photoelectron-counting histogram (PCH) was introduced in [19] as a technique to accurately determine conversion gain and read noise in QIS devices and will be discussed in more depth in [24]. An example of a PCH is shown in Fig. 4 for a TPG jot with 4 different levels of exposure made by changing the integration time for constant light intensity. The discrete peaks correspond to different numbers of electrons, with amplitude corresponding to the Poisson distribution. The peaks are broadened by the read noise of 0.28e- r.m.s. as determined by the valley-peak modulation (VPM) [19]. For accurate photoelectron counting, VPM close to unity is desired, corresponding to 0.15e- r.m.s. or less of read noise. For higher values of read noise, the peaks become less distinct and are finally blurred by read noise above approximately 0.50e- r.m.s., resulting in a smooth distribution.

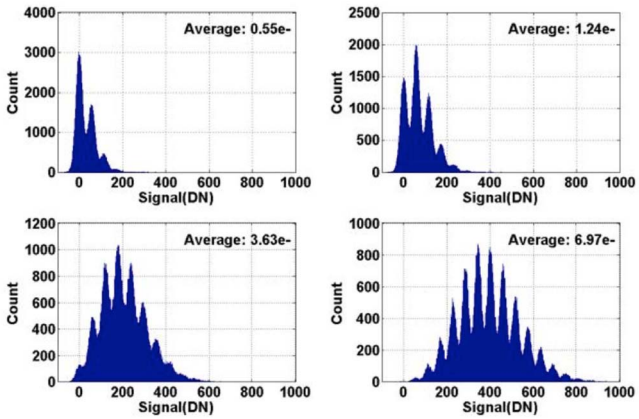

FIGURE 4. Measured photoelectron-counting histograms (PCH) of a single TPG jot for different exposures of 0.55e-, 1.24e-, 3.63e- and 6.97e-. Each PCH is created from 200,000 samples. Read noise is 0.28e- r.m.s.

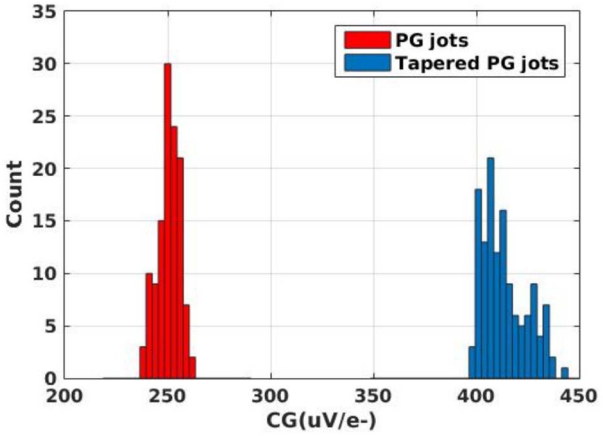

FIGURE 5. Measured histograms of the CG of PG jots and TPG jots in two 12x12 arrays. The CG of each jot is measured from the PCH method with 200,000 samples.

B. CONVERSION GAIN AND CONVERSION GAIN VARIATION

The PG jots and the TPG jots were characterized with the PCH method. Each jot is selected and read out using digital CDS 200,000 times at a fixed illumination level to generate one PCH. Each bin of the histogram corresponds to one LSB or DN of the ADC. The peak spacing corresponds to one electron, and can be used to determine DN/e- for that jot. From the calibration of the gain of the PGA plus output buffer (V/V), and the ADC (μV/DN), the conversion gain (μV/e-) of the jot after its source-follower can be determined.

Due to the limitation of the number of pads, and the resultant readout design, testing multiple jots was tedious since manual intervention is required to select different jots within the 32x32 array. Consequently, we focused on a 12x12 subarray of adjacent jots (144 jots, 200,000 samples each). CG can be determined from peak spacing and read noise from VPM. We also tried a best fit for the data from a PCH model with both read noise and CG as fitting parameters. Excellent agreement was found for the two PCH methodologies.

A histogram showing CG for the PG and TPG jots is shown in Fig. 5. The mean CG of PG jots is 250.5μV/e- with 2.1% standard deviation, and the mean CG of TPG jots is 413.4μV/e- with 2.6% standard deviation. The reason for the variation in CG is not known but area variation due to lithography of small features resulting in capacitance variation is a likely suspect.

Conversion gain variation will lead to errors in photoelectron counting in a multi-bit QIS even with read noise less than 0.15e- r.m.s.. In an n-bit multi-bit QIS, multiple photoelectrons are collected and read out in one read, where n is the bit depth of a hypothetical on-chip ADC with one LSB or DN corresponding to one electron. For example, a 2-bit QIS would have a 2-bit ADC with 4 conversion levels or bins, corresponding to 0, 1, 2 and 3 or more electrons. A multi-bit QIS requires the CG variation $\gamma \triangleq \Delta CG/CG$ to be less than $1/2^n$, and for fewer errors, less than $1/2^{n+3}$, where CG is the nominal conversion gain [10]. The impact of γ on error rate depends on the electron number N, quanta exposure H (e-), and read noise σ_n (e- r.m.s.). The histogram peak for electron number N is shifted by relative amount γN in the ADC conversion bin. The shift in the peak position increases the false negative bit error rate for that bin, and false positive bit error rate for adjacent bins, by an amount that depends on the shift, read noise and quanta exposure. The relationship among these factors will be discussed in a separate paper [25], but total bit error rate (BER_T) for all bins can be written as:

$$BER_T = \sum_{N=0}^{2^n-2} \frac{1}{2} \frac{e^{-H} H^N}{N!} erfc\left[\frac{1-2\gamma N}{\sqrt{8}\,\sigma_n}\right] + \sum_{N=1}^{2^n-1} \frac{1}{2} \frac{e^{-H} H^N}{N!} erfc\left[\frac{1+2\gamma N}{\sqrt{8}\,\sigma_n}\right] \quad (1)$$

Total bit error rate as a function of exposure is shown in Fig. 6. The complexity of the graph reflects the complexities of Eq. 1. The solid lines are BER_T for a gain variation γ of 2.6% and read noise of 0.29e- r.m.s., corresponding to a nominal jot reported here. The BER_T for $n = 1$, a single-bit QIS, is about 4% for low exposures, and decreases for higher exposure. The BER_T for $n = 2$, a 4-level jot, is about 4.6% at low exposures, rises to about 6.5% at $H = 1$, and then drops with increasing exposure. For 3-bit and 4-bit jots, BER_T rises to higher levels before dropping with larger exposures. This is primarily the effect of the read noise rather than the gain variation, as evidenced by the dashed curves calculated for no gain variation. Also shown are dotted curves that correspond to a gain variation γ of 2.6% but a lower read noise of 0.22e- r.m.s.. It can be seen that the BER_T is substantially reduced by about 4x. The BER_T rise for higher exposures for the 3-bit and 4-bit QIS is attributable to conversion gain variation since peak shift grows with bin number resulting in more errors. Conversion gain variation and read noise are both detrimental to higher bit depth multi-bit QIS realization.

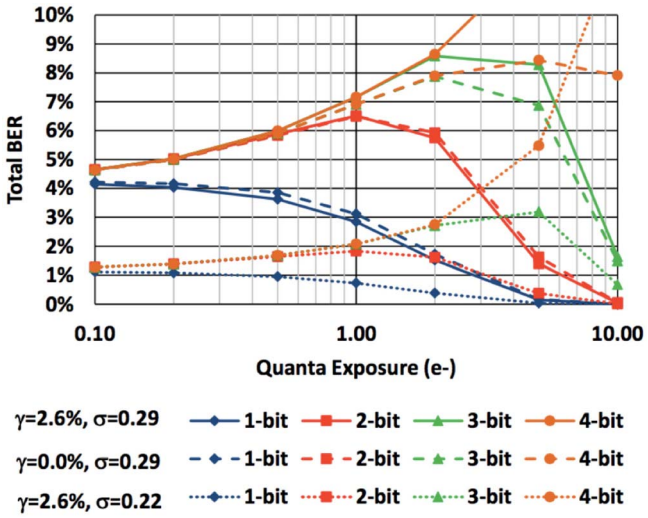

FIGURE 6. Theoretical total bit error rate for a jot of a multi-bit QIS as a function of exposure for different bit depths, and for 3 combinations of conversion gain variation and read noise.

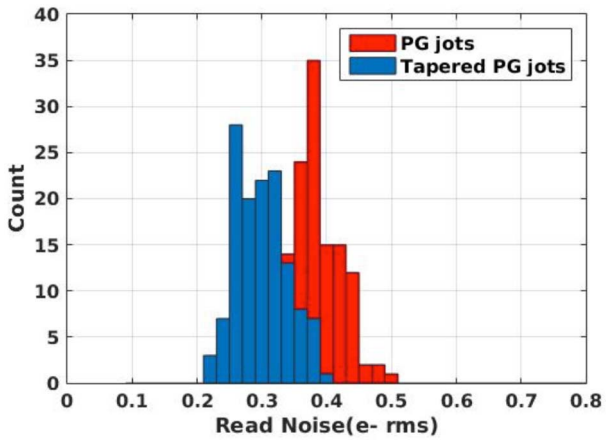

FIGURE 7. Histograms of the read noise for PG jots and TPG jots in two 12x12 arrays. The read noise of each jot is measured from the PCH method with 200,000 samples.

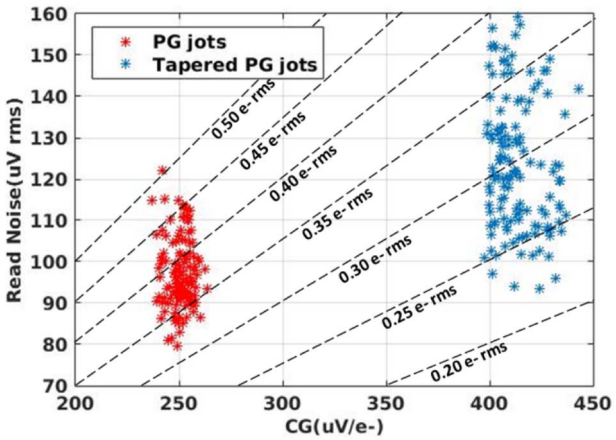

FIGURE 8. Scatter plot of measured read noise vs. CG for 12x12 PG jots and TPG jots.

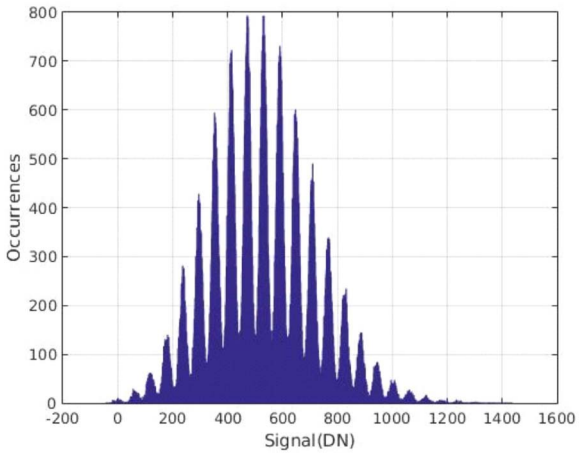

FIGURE 9. PCH for a "golden jot" with 0.22e- r.m.s. read noise and CG of 423μV/e- for a mean signal of ~9.0 e- at room temperature.

C. READ NOISE AND READ NOISE VARIATION

A histogram of read noise of the measured jots is shown in Fig. 7. The average read noise of PG jots is 0.38e- r.m.s. with 8.7% standard deviation, and the average electron read noise of TPG jots is 0.29e- with 13.2% standard deviation.

A scatter plot is shown in Fig. 8 for the same data showing read noise in volts on the vertical axis and conversion gain on the horizontal axis. Lines of constant electron read noise are shown for reference purposes. It is seen that the PG jot scatter in voltage read noise is quite substantial, from 80μV r.m.s. to 120μV r.m.s. giving rise to the broad distribution of electron read noise in Fig. 6. The TPG jot scatter is greater, ranging from 90μV r.m.s. to 160μV r.m.s., likely due to the smaller area of the SF gate for the TPG jots. Because of the substantially higher CG of the TPG jots, electron read noise is generally lower than that of the PG jots. The best (golden) jots achieve about 0.22e- r.m.s. read noise. An example PCH from a golden jot is shown in Fig. 9.

Since the SF gate capacitance is the dominant contributor to total FD node capacitance, one might expect that the dominant cause of CG variation is variation in SF gate area. One might then expect that variation in CG should be correlated to variation in voltage read noise since 1/f noise or RTS noise is directly related to SF gate area, that is, the number of interface traps in the channel, However, from Fig. 7 it appears this is not the case and the voltage read noise is randomly distributed independently of CG, perhaps indicative of random fluctuation in the actual number of traps at the Si and gate-insulator interface. Since the total number of traps may only be 10-100 per gate (e.g., $0.04\mu m^2 x5x10^{10}/cm^2 = 20$) high fluctuation in the number of traps between devices might be expected even if the gate area had no variation, leading to a variation in noise.

The scatter plot also suggests that further reduction of the dominant source of capacitance, the SF gate area, will lead to a further increase in 1/f, RTS noise and CG scatter, and

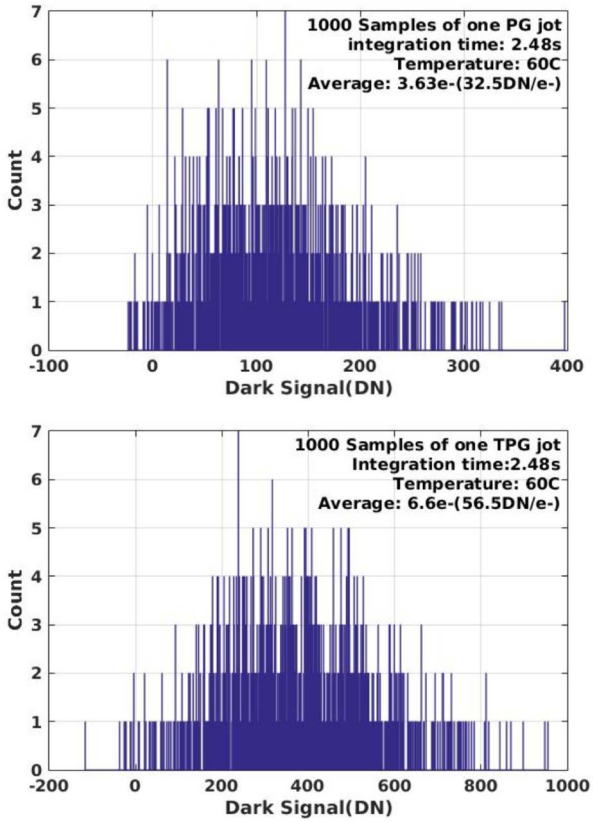

FIGURE 10. Histogram of 1000 dark samples of one PG jot (top) and one TPG jot (bottom) at 60C with 2.48s integration time.

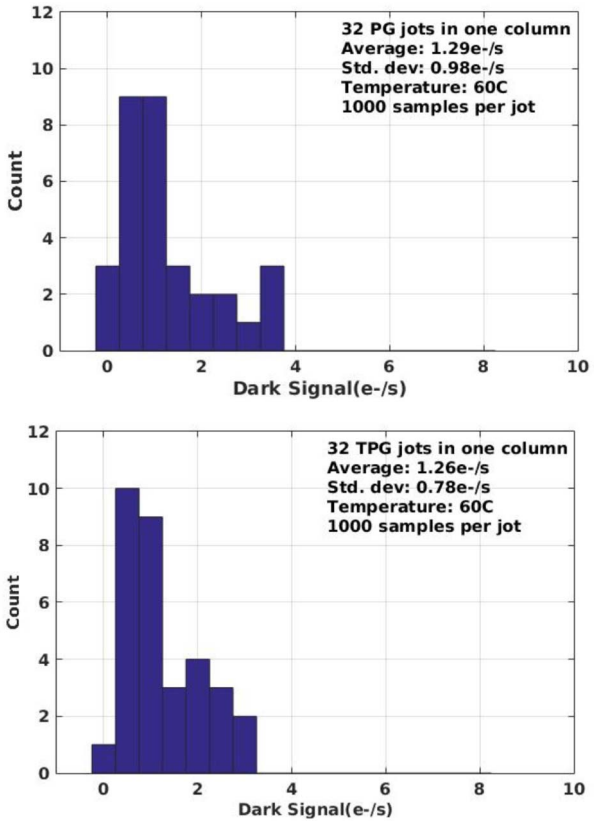

FIGURE 11. Histogram of dark current among 32 PG jots in one column at 60C. The standard deviation of the dark current is 0.98e-/s. 1000 samples are taken for each jot. Also shown is the histogram of dark current among 32 TPG jots in one column at 60C. The standard deviation of the dark current is 0.78e-/s. 1000 samples are taken for each jot.

diminishing returns for improving CG with scaling. While some improvement will be achieved, a gross extrapolation suggests that with an increase in CG to 1mV/e-, average read noise might be in the 0.22-0.24e- r.m.s. realm. This motivates us to consider either p-channel jots, or consider a buried-channel MOS SF or JFET SF in future designs if we wish to achieve 0.15e- r.m.s. read noise or lower.

The effect of bias current on SF noise was briefly examined. Unfortunately, increasing the bias current negatively impacts the PGA gain in our design since they share a ratioed current source. Backing out PGA gain deterioration to obtain the electron noise as a function of bias current is tenuous, but generally it seemed the noise might increase by approximately 0.1e- r.m.s. as the SF bias current is increased from the nominal level of 0.5μA to 5.0μA, which is important for QIS applications.

D. DARK CURRENT

In a pump-gate device, the signal storage well SW is buried underneath the TG and isolated from the Si-SiO_2 interface by a potential barrier. Interface-generated dark current flows to the FD during signal integration which helps improve the dark current performance because the Si-SiO_2 interface at the TG edge usually contributes a major part of dark current in pinned-photodiode pixels. Consequently a low dark current was anticipated for both PG and TPG jots.

The SW dark current in the pump-gate jot was found to be quite low, about 1 pA/cm^2 at room temperature for both PG and TPG jots, or about 0.1e-/s. This makes measurement of many devices tedious since an integration time of about a minute is needed per jot per measurement, and 1000 measurements are taken per jot. Due to the readout electronics, parallel integration and readout of the array is not possible. Thus, only 32 jots were measured of each type, at room temperature (25C) and at 60C.

A histogram showing 1000 samples of a single PG jot and a single TPG jot at 60C is shown in Fig. 10. The 1000 samples are not enough to create a histogram that shows quantization in electron number.

At room temperature, the mean measured dark current for PG jots is 0.09e-/s or 0.73pA/cm^2, and 0.12e-/s or 0.98pA/cm^2 for TPG jots. At 60C, the measured dark current for PG jots is 1.29e-/s or 10.5pA/cm^2, and for TPG jots, 1.26e-/s or 10.2pA/cm^2. Histograms showing the data at 60C are shown in Fig. 11.

The measured dark current at 60C is about 14x of the dark current at 25C, which suggests the dark current in the jot devices has an activation energy of half the bandgap and is likely dominated by mid-gap traps.

A second source of dark signal was also observed that remains unresolved. The dark signal increases with the

duration and amplitude of the TG "on" pulse width, and corresponds to approximately 0.1e-/μsec when TG is on at 3V. This dark signal does not depend on SW integration time and seems to be TG related, and ranged from a few tenths to a few electrons per transfer. It was subtracted as an offset from the integration-time-dependent dark signal in the reported dark current results. The anomalous dark signal has a PCH signature with peaks and valleys and roughly Gaussian shaped envelope, but with a peak amplitudes distribution different from the Poissonian model. The source of this unresolved and interesting signal may be explored in later work.

E. LAG

In the PG and TPG jots, charge is first transferred from the SW to under the TG gate, and then from there to the FD. The TG pulse "on" period was a relatively long 4μsec due to the nature of the readout electronics, and TG "on" was reduced to 2.5V to minimize the mean anomalous dark signal to less than 0.1e-. Incomplete charge transfer due to barriers or trapping can occur leading to lag. Measurement of lag is more difficult in the 0-10e- quanta exposure range since the signal is strongly influenced by Poisson statistics and will vary significantly from one read to the next.

Lag was checked by pulsed illumination. PG jots were illuminated for 5 frames and not illuminated for the next 5 frames, with this on-off cycle repeated. Signal for one jot was accumulated over 200,000 cycles for each of the 10 frame positions, and then the resultant PCH data was analyzed to obtain a mean signal value (and CG and read noise) for each frame position. However, PCH is difficult to use below about 1e- mean signal so conventional calculation of the mean signal was performed. Typical results are shown in Fig. 12 for 12 different exposure levels. The lowest exposure level was approximately 0.295e- (first bar of each frame set) during the first 5 illuminated frames, with an average residual signal of 0.024e-, or 8% in the trailing 5 dark frames. As the exposure is increased (successive bars in each frame set) the residual signal also generally increases (but not consistently as seen in frame set 7 vs. frame set 8). For example, when the exposure is 1.6e-, the average residual signal is 0.047e-, or 3%. At the highest exposure (last bar of each frame set) the mean signal is 11.1e- with a residual signal of 0.19e-, or 1.75%.

We hesitate to call the residual signal lag, because it persists for at least dozens of frames if the light remains off. The total signal in the discharge lag (frames 5 and beyond) far exceeds the total signal lost in charging lag (possibly seen between frame 0 and frame 1). It is also influenced by TG "on" voltage level and "on" period, increasing with both, counter to most models of lag. One conjecture is that photoelectrons are collected in adjacent parts of the structure, and transferred to FD as the residual signal. Note that for most exposures of interest for the QIS, the residual signal or lag is below 0.1e-.

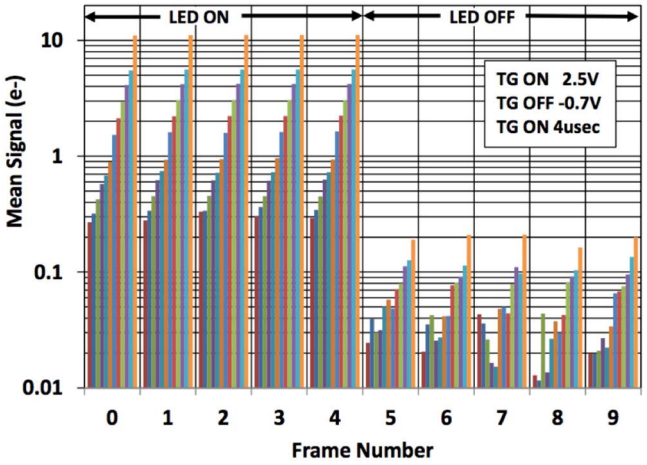

FIGURE 12. Lag measurement for PG jot for 5 illuminated frames followed by 5 dark frames and repeated (frame 0 follows frame 9). Note log scale of vertical mean signal axis. Each frame set represents 12 different exposure levels.

More detailed measurements such as the effect of TG transfer time, temperature, and voltage levels, are warranted in the future with more amenable readout circuits, but at this time it is felt that pump-gate jot lag at the sub-0.1e- level is acceptable for most photoelectron counting applications.

V. DESIGN VARIATIONS

In addition to the baseline PG jot design, there were 15 variations that were explored including 3 TPG jot designs. Most of the changes involved adjusting relative sizing and spacing of various mask layers. In fact, it appears the baseline PG jot design and the baseline TPG jot design yielded the best results, but the impact of variations appears minor.

We expected a stronger influence of spacing between TG and the distal FD but saw little effect in the range 0.06um to 0.28um, where 0.28um was the baseline. It is possible that the charge transfer efficiency from SW to FD would be affected by the spacing between TG and FD, but we saw no evidence of that. However, a more complete assessment of lag is planned for the future.

Changes that would affect VB and SW, seemed to primarily have a small influence on responsivity (a few percent) and impacted full-well capacity as expected.

We noticed that the responsivity of the TPG jots seemed to be slightly lower than the PG jots despite significantly higher CG, suggesting that carrier collection efficiency needs to be improved in future TPG jots.

While the design variations did not lead to a clear optimum design for this process, the device performance appears to be robust relative to design variations, suggesting that pixel shrink in the process is a viable option for the future.

VI. SUMMARY AND DISCUSSION

In this paper, the characterization results of two types of jot devices with single-CDS-read, room-temperature photoelectron-counting capability were discussed. A summary of characterization results is listed in

TABLE 1. Jot characterization results (average values).

	PG jots	TPG jots
Pitch Size	1.4um	1.4um
SF Size	0.4um x 0.2um	0.2um x 0.2um
Col. Bias Current	416nA	416nA
PCH CG	250.5μV/e-	413.4μV/e-
CG Variation	2.1%	2.6%
PCH Read Noise	0.38e- r.m.s. (96.9μV r.m.s.)	0.29e- r.m.s. (123.0μV r.m.s.)
Read Noise Std. Dev.	8.7%	13.2%
SF 1/f noise	95.3μV r.m.s.	121.7μV r.m.s.
Dark Current @ RT	0.09e-/s (0.73 pA/cm^2)	0.12e-/s (0.98 pA/cm^2)
Dark Current @ 60C	1.29e-/s (10.5 pA/cm^2)	1.26e-/s (10.2 pA/cm^2)
Lag @ RT	<0.1e-	Not measured
Full Well Capacity	288e-	210e-

Table 1. Implemented in a commercial BSI CIS process with minimal changes, a pixel pitch of 1.4um was easily achieved. The measured read noise of the PG jot devices ranged from 0.32e- r.m.s. to 0.50e- r.m.s., with a mean of 0.38e- r.m.s.. The measured read noise of the TPG jots ranged from 0.22e- r.m.s. to 0.38e- r.m.s. with a mean of 0.29e- r.m.s.. The low read noise, due mostly to high conversion gain, will enable realization of practical photoelectron counting image sensors in the near future, including the Quanta Image Sensor. The measured CG variation is less than 3% for both devices and is sufficiently low to permit modest multi-bit QIS operation with low bit error rate. Both devices have extremely low dark current. The measured dark current at 60C is under 11pA/cm^2 for both devices and is one of the lowest dark current rates reported, for electron-carrier image sensors, and far lower than dark count rates reported for SPAD sensors. Lag was measured to be under 0.1e- for signals less than 10e-.

The use of the buried-channel SF option in the process should further reduce read noise. It has been suggested by colleagues elsewhere with image sensors fabricated in the same multi-project wafer run that device parameter variation was unusually high and perhaps this is related to the high variation we observed in CG.

This is one of the first works on characterizing image sensor pixels at mean exposures of a few electrons to as low as 0.25e-, made possible in part by the high conversion gain and deep sub-electron read noise. New characterization challenges were found in this regime due to the strong impact of Poisson statistics, especially regarding dark current and lag.

The reported jot devices will have broad application in low light imaging, scientific imaging, high dynamic range applications, and possibly consumer photography. Photon-counting capability in nearly-conventional CMOS image sensors may also open up new opportunities for replacing electron-multiplying CCDs in some applications with improved resolution and performance.

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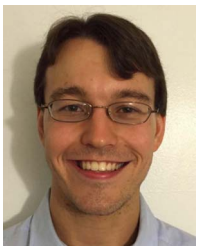

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