A 1Mega-pixel 1000fps Path-finder Single-bit Quanta Image Sensor

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Quanta Image sensors (QIS) are proposed as a paradigm shift in image capture to take advantage of shrinking pixel sizes [1]. The key aspects of the single-bit QIS involve counting individual photoelectrons using tiny, spatially-oversampled binary photodetectors at high readout rates, representing this binary output as a bit cube (x,y,t) and finally processing the bit cubes to form high dynamic range images. One of the challenges for the QIS is the design of internal high-speed and low-power addressing and readout circuitry. A QIS may contain over a billion specialized photodetectors, called jots, each producing just 1mV of signal, with a field readout rate 10-100 times faster than conventional CMOS image sensors. This paper presents a pathfinder image sensor for exploring the low-power binary readout circuits needed for commercial implementation of giga-jot single-bit QIS devices.

The 1376Hx768V pixel image sensor uses a conventional 3T, 3.6µm pixel and readout architecture implemented in a 0.18µm process, as shown in Figure 1. 4T-PPD pixels were not yet available at XFAB at the time of tapeout. True jot implementation requires a smaller technology node and is underway separately. Our focus here is on the signal chain from pixel to digital output, though specialized implants were used to increase conversion gain to about 200µV/e- according to TCAD simulation. The sensor is operated in a single-row rolling shutter mode so true CDS is utilized, otherwise kTC noise exceeds the target LSB.

A column-parallel single-bit ADC using a charge transfer amplifier (CTA) -based design detects a >0.5mV output swing (~2.5e-) from the pixel. The ADC is capable of sampling at speeds of 768kSa/s to produce the binary output while consuming 1.9µW per column. Figure 2 shows the 1-bit ADC circuit. The analog readout comprises 4 stages of fully-differential CTA-based sense amplifiers, followed by a D-Latch comparator. The cascade of CTAs provides a gain of 400 (gain of 4 to 5 per stage), which reduces the ADC's input-referred offset, mainly due to transistor mismatch in the comparator, to less than 500µV. A detailed description of the CTA operation can be found in [2, 3]. Compared to [3], use of a differential CTA and column-parallel ADC layout in an actual image sensor required more power dissipation. The timing and signal waveforms of the functioning of one column and ADC are shown in figure 3. The sensor operates at 1000fps, which corresponds to a row time of 1.3µs, a signal integration time, T_{int}, of 1µs, and an output data rate of 1Gb/s. The ADCs working in tandem with digital circuits consume an average power of 6.4mW. A second concern in a giga-jot QIS is clock distribution power in the row selection circuits. To address this concern, flip-flops in addressing circuits are implemented as pseudo-static circuits, which combine the low power consumption of a dynamic circuit with the robustness of a static one [4].

The final specifications of the sensor are shown in Figure 4, and Figure 5 shows one frame of bits that was measured from the sensor. The zoomed image of Figure 5 shows roughness in the edges of characters. This is likely caused by the resolution (600dpi) of the printer used to print the word “IEEE”, leading to a less distinct edge. The power consumption of the entire chip (including I/O pads) is 20mW. The die microphotograph is shown in Figure 6 depicting various sections of the chip. We define an energy/bit figure of merit *FOM=Chip power/(# of pixels×fps×N)*, where N represents the ADC resolution in bits, which for algorithmic converters is the number of comparator strobes per conversion. The pathfinder sensor has an FOM=19pJ/b. We calculate that SOA 12b CMOS image sensors of [5], [6], have a FOM of 53pJ/b and 120pJ/b, respectively.

The power reduction circuit strategies proven in the pathfinder chip allow us to proceed with confidence to giga-jot single-bit QIS implementations in advanced processes. Energy FOM of 19pJ/b scaled down with smaller parasitic capacitances and rail voltages for advanced technology nodes gives power dissipation in the sub-Watt level range for giga-jot QIS devices, sufficient for commercial purposes.

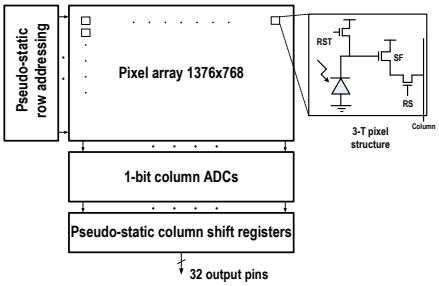

Figure 1. Architecture of the pathfinder sensor.

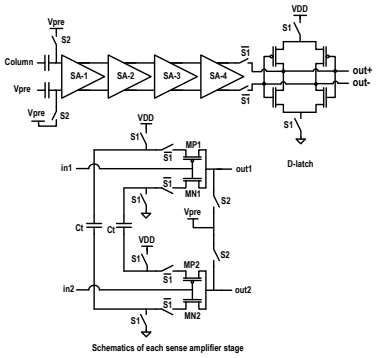

Figure 2. Single bit ADC based on charge transfer technique.

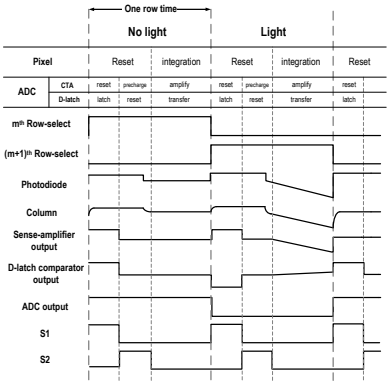

Figure 3. Timing diagram and various phases of operation for each column and ADC.

Process		XFAB, 0.18 µm, 6M1P (non-standard implants)
VDD		1.3 V (Core), 1.8 V (Array), 3 V (I/O)
Pixel type		3T-APS
Pixel pitch		3.6 µm
Photo-detector		n+-p Photodiode
Conversion gain		~200 µV/e- (CAD simulation)
Array		1376 (H) X 768 (V) (WXGA 16:9 ratio)
Field rate		1000 fps
ADC sampling rate		768 KSa/s
ADC resolution		1 bit (LSB = 1 mV)
Output data rate		32 (output pins) X 33 Mb/s = 1 Gb/s
Package		PGA with 256 pins
Power	Pixel array	8.6 mW
	ADCs	2.6 mW
	Addressing	3.8 mW
	I/O pads	5 mW
	Total	20 mW

Figure 4: Specifications of the 1MP Binary Image Sensor

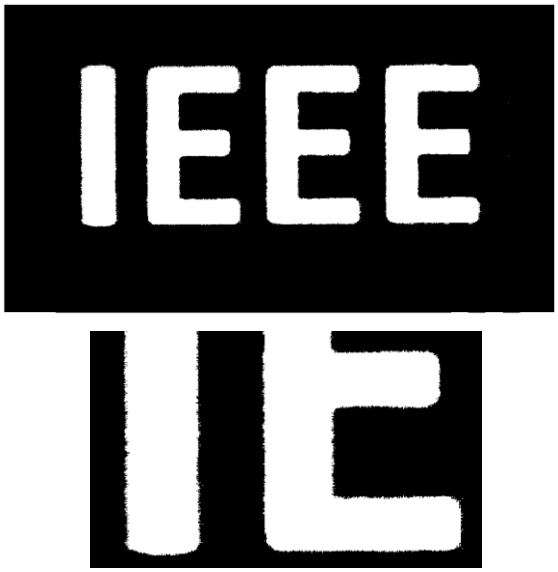

Figure 5: Single captured binary frame with blowup to show more details as described in text.

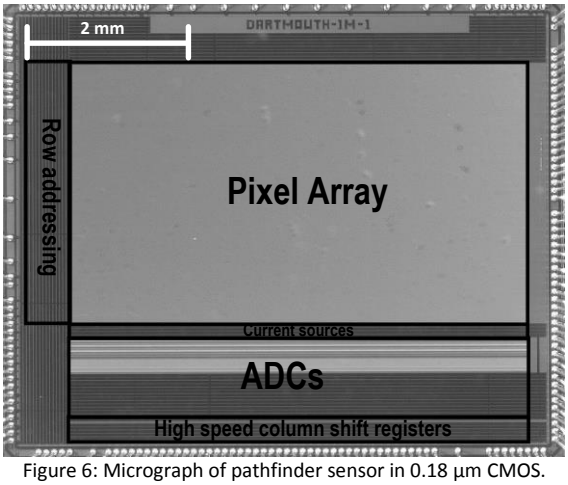

Figure 6: Micrograph of pathfinder sensor in 0.18 µm CMOS.

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