THAYER SCHOOL OF ENGINEERING AT DARTMOUTH

TCAD Modeling of Devices for Quanta Image Sensors

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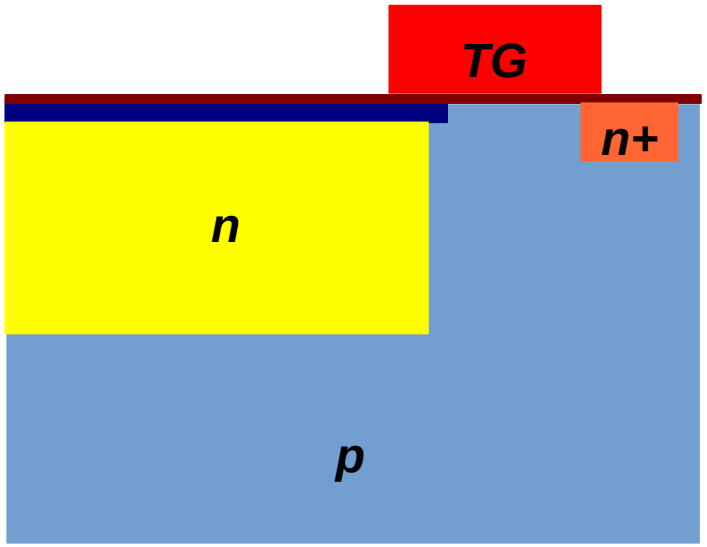
Review of CMOS Image Sensor with a pinned photodiode



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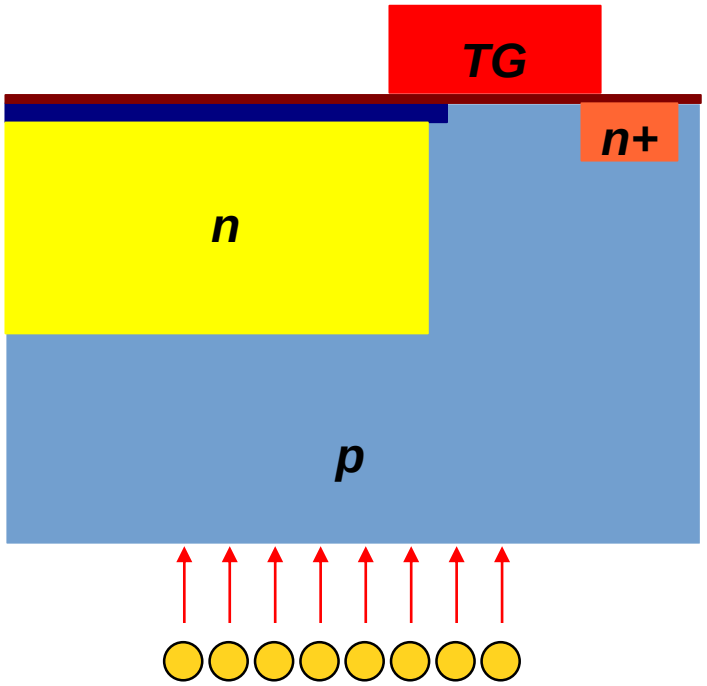

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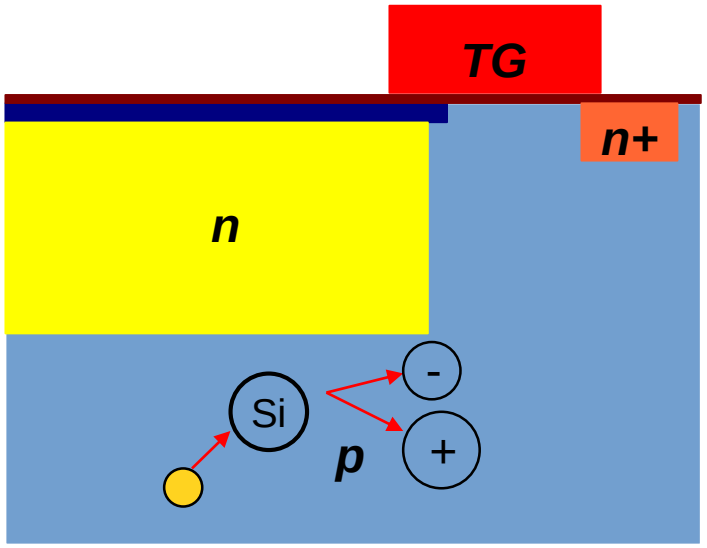

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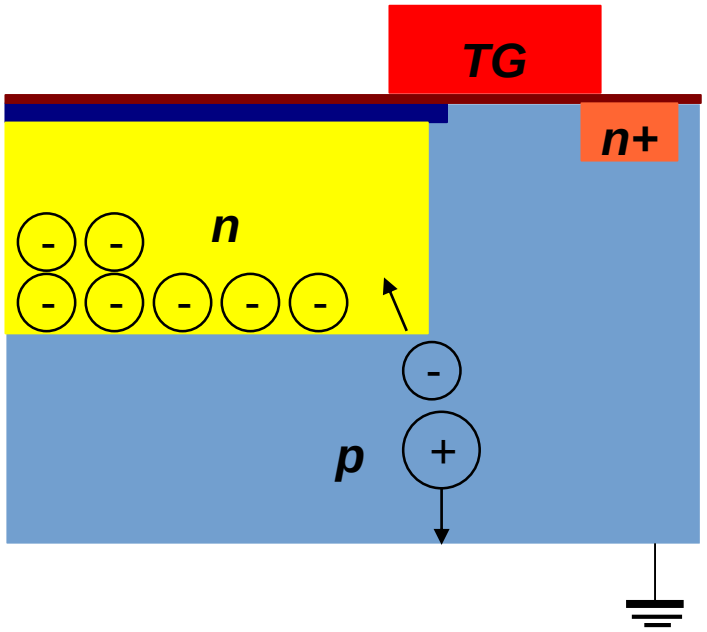

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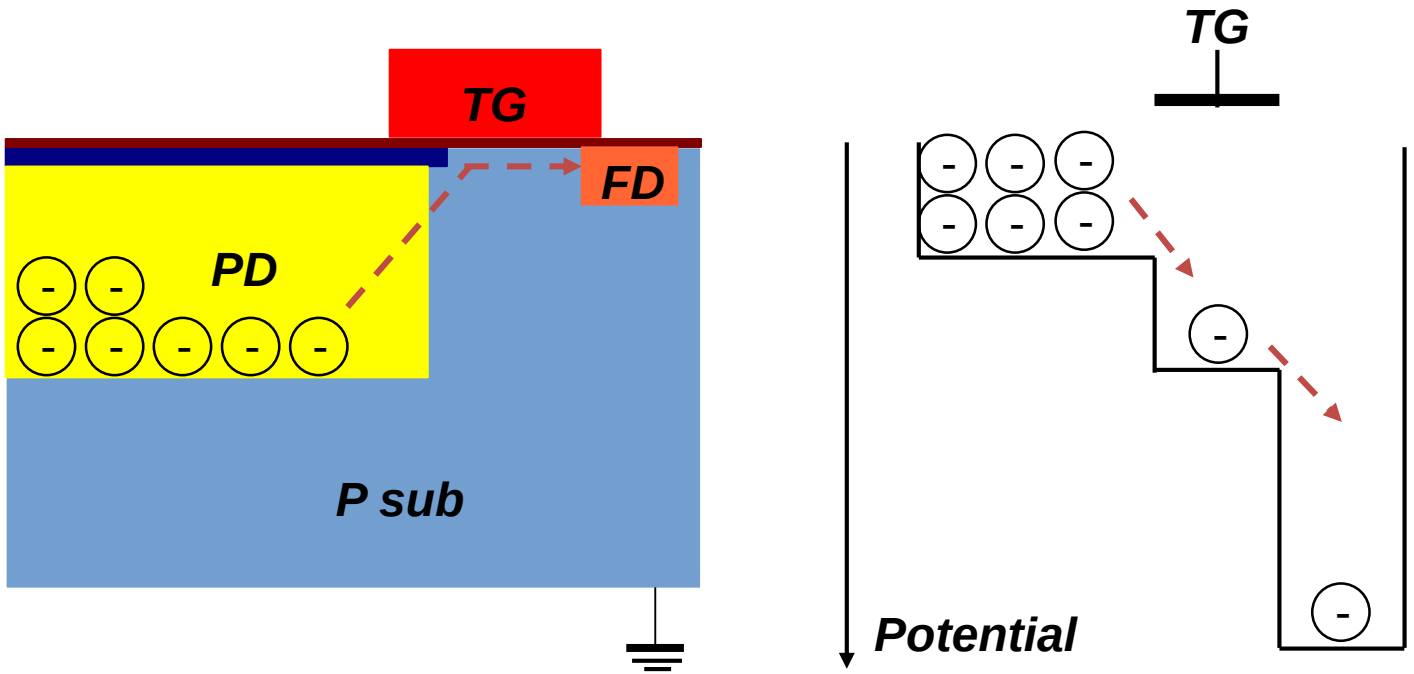

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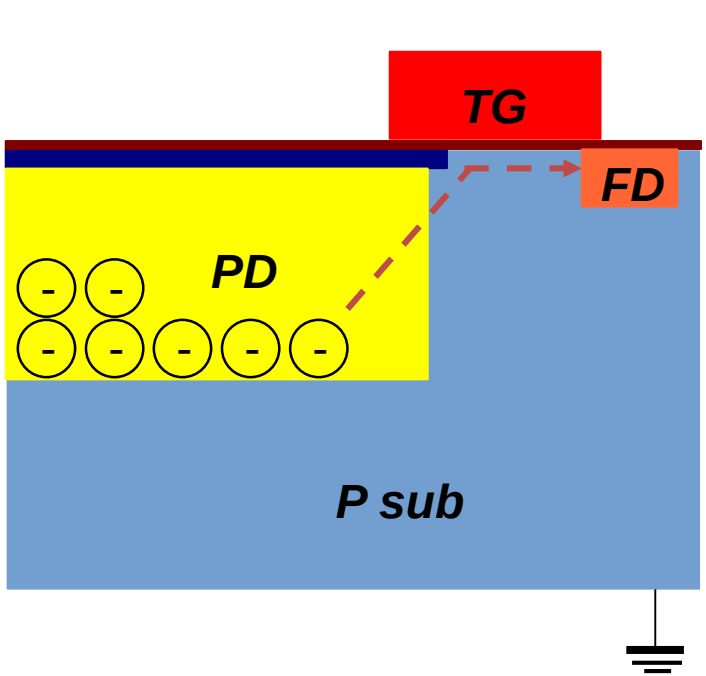

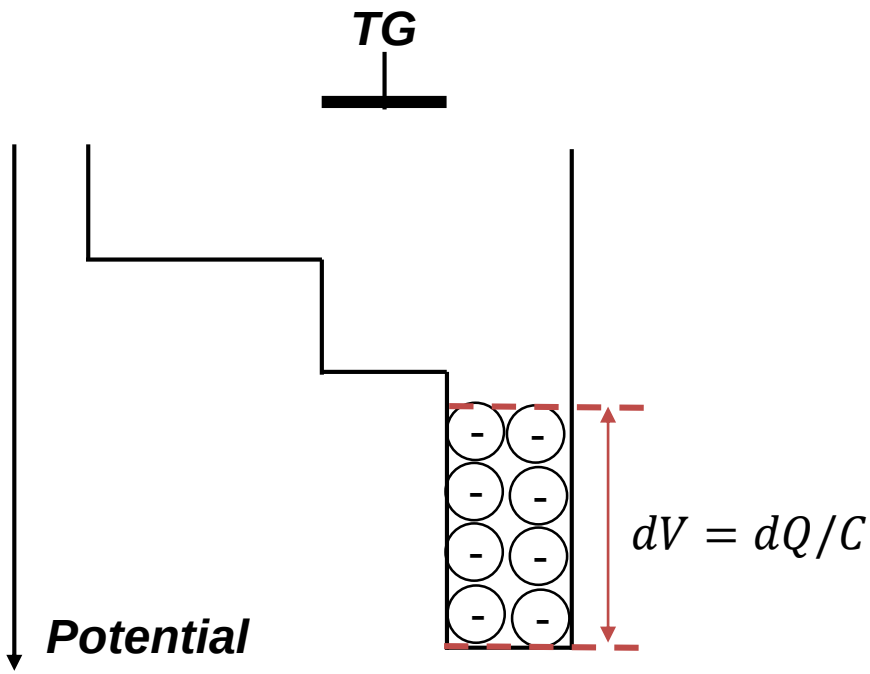

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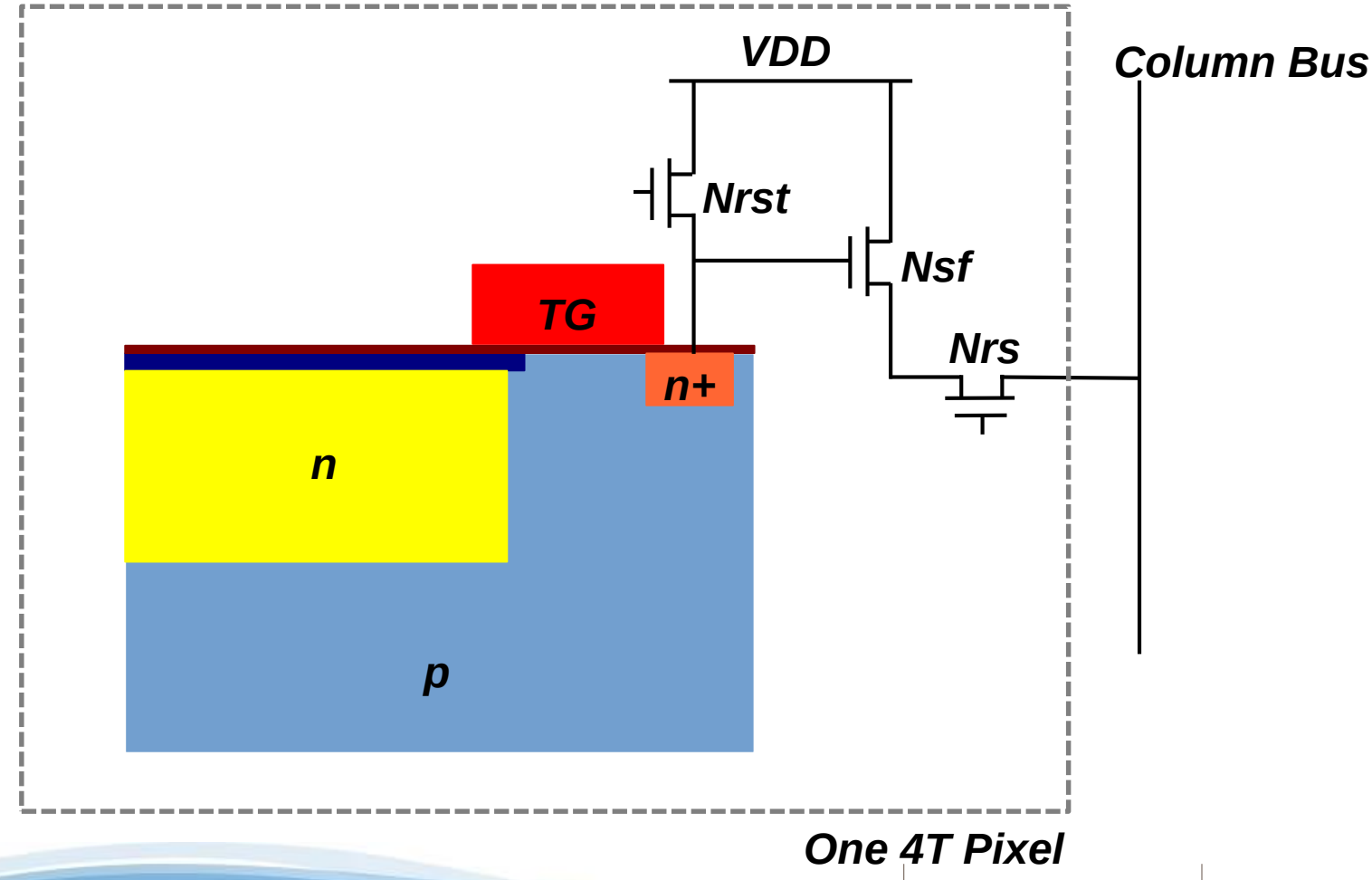
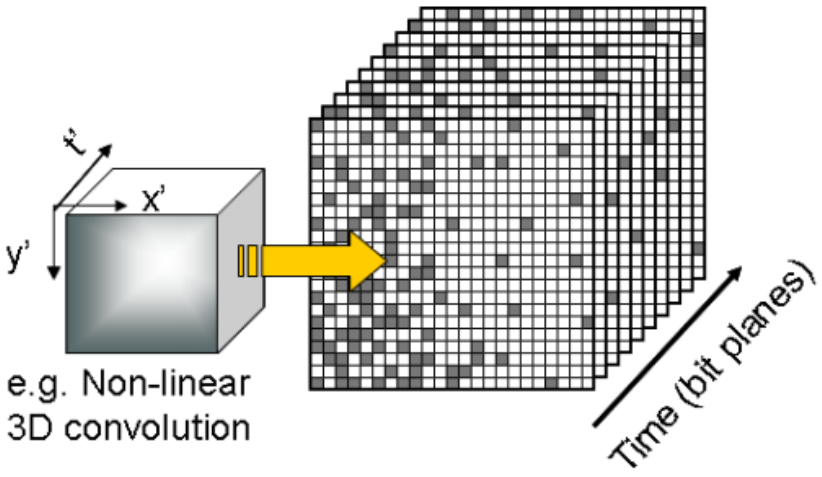


Quanta Image Sensor (QIS) Concept

- The goal for QIS is to make a very ***tiny***, specialized pixel ("jot") which could sense a ***single*** photo-electron and output ***binary*** data.
- Jots array would be readout by scanning at a ***high frame rate*** to avoid likelihood of multiple hits in the same jot and loss of accurate counting.
- Image pixels could be created by combining jot data over a local ***spatial*** and ***temporal*** region using image processing.



Quanta Image Sensor (QIS) Motivation

- Photons are digital in nature according to particle view of light and can be represented by binary data
- Better images can be obtained by oversampling in time and space.
- More applications, such as motion blur correction.

Jot Device Concept

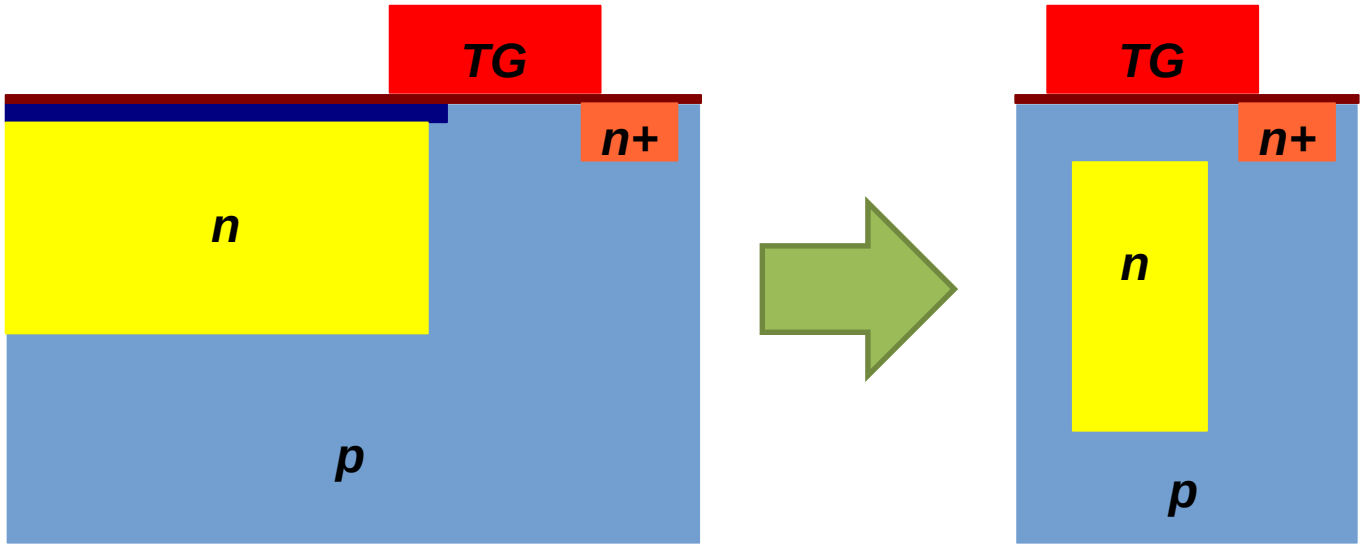
*Specialized **tiny** pixel, sensing **single** photo-electron, output **binary** data*

	Jot	Pixel
Size	650nm(10L)	1.1um*(17L)
Storage Capacity	1-100e-	~10000e-
Conversion Gain	>1mV/e-	100uV/e-
Read Noise	0.15e- rms	~2e- rms

65nm CMOS CIS process

Jot Device Design

Shrink size



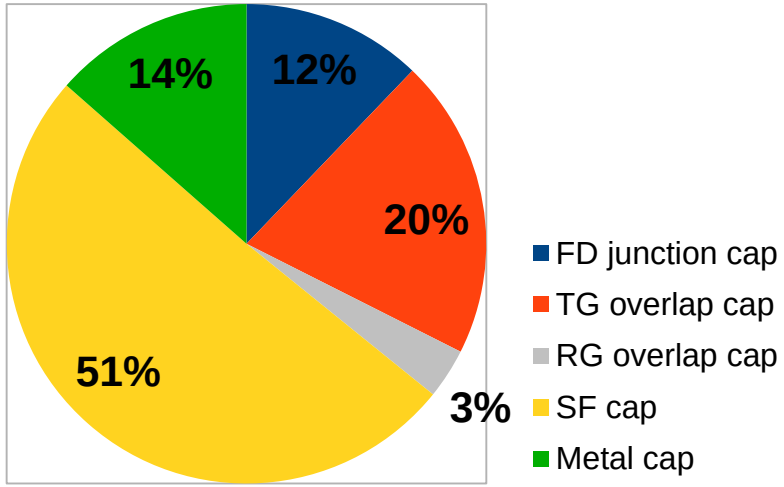
Jot Device Design

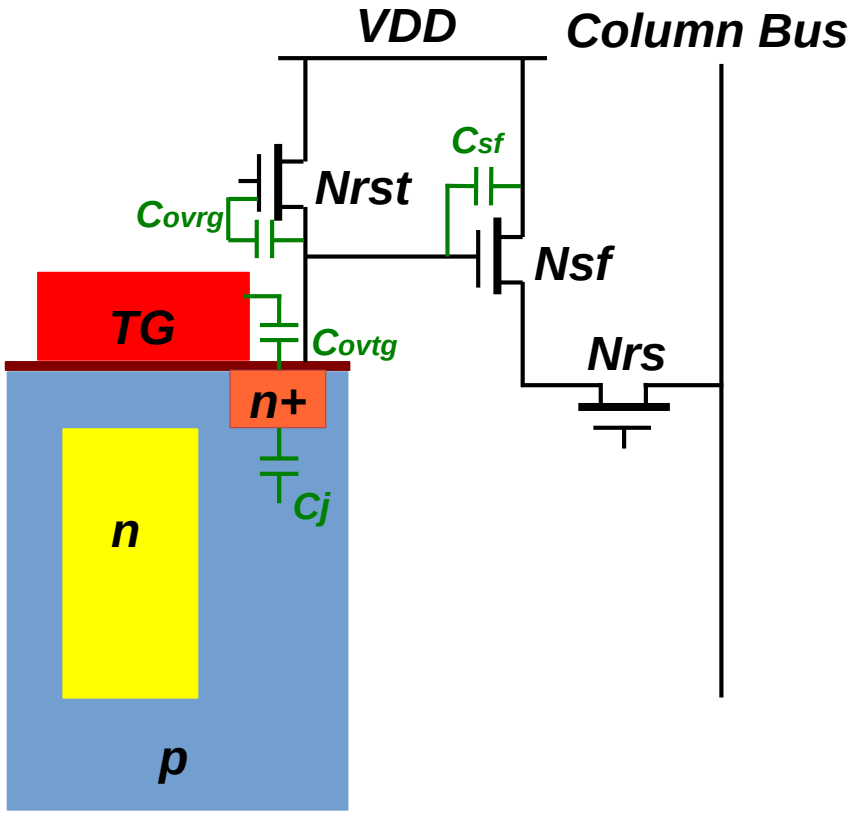
Improve sensitivity

$$dV = dQ/C_{FD}$$

$$C.G. = \frac{dV}{dQ} = \frac{1}{C_{FD}}$$

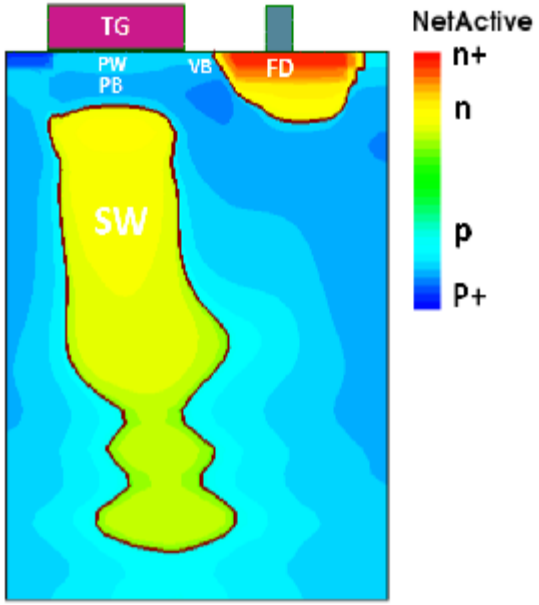
$$C_{FD} = C_j + C_{ovtg} + C_{ovrg} + C_{sf} + C_{metal}$$

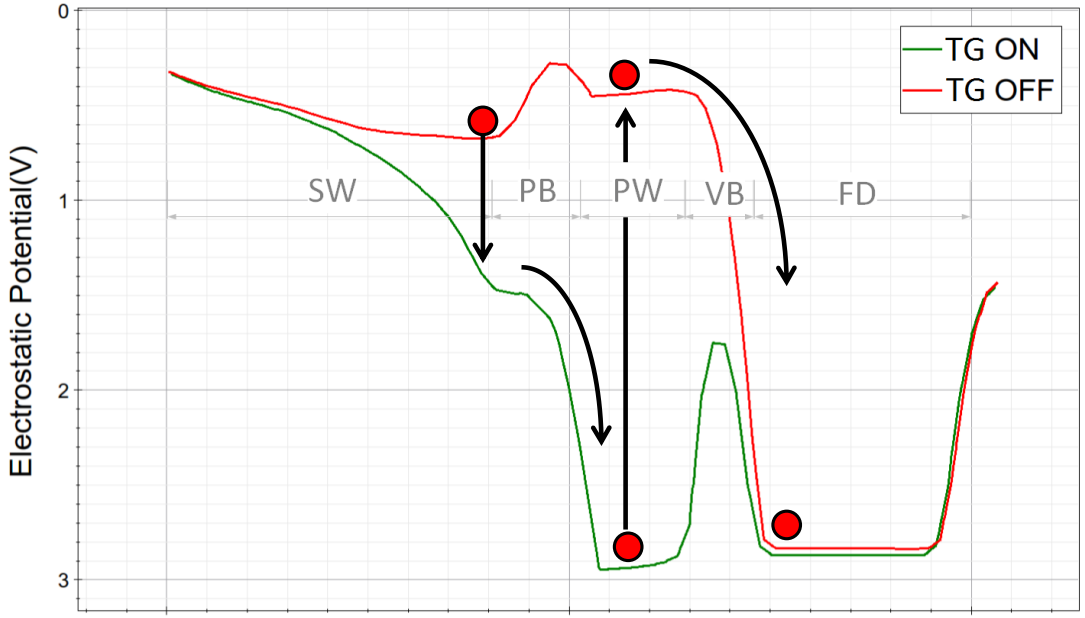




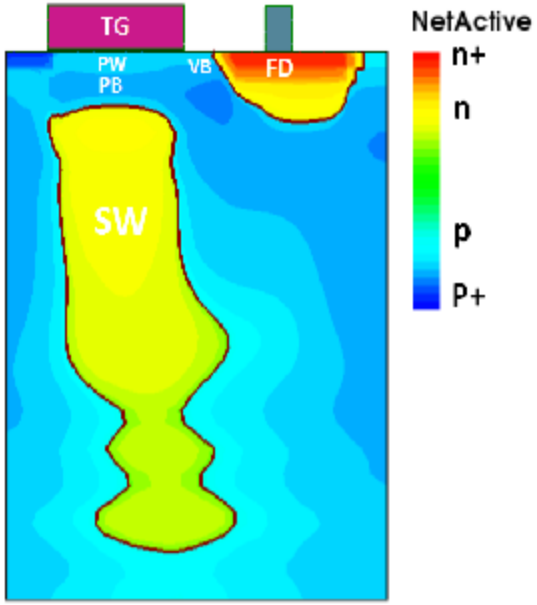
**1.4um PPD Pixel*
CFD=1.55fF
C.G.=103uV/e-

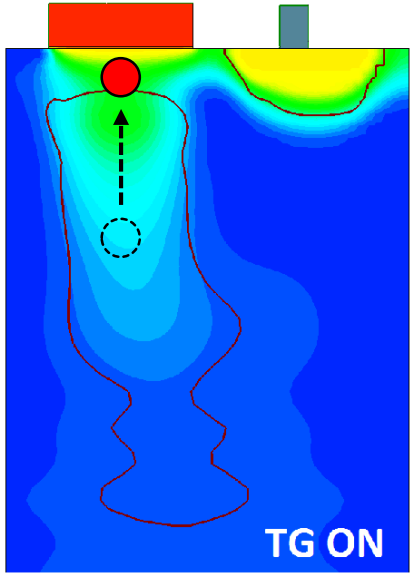
Pump gate charge transfer

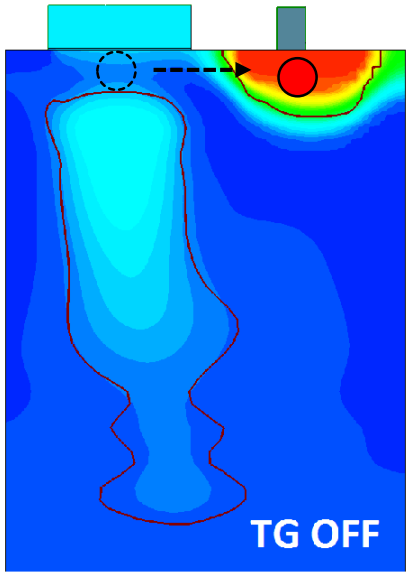




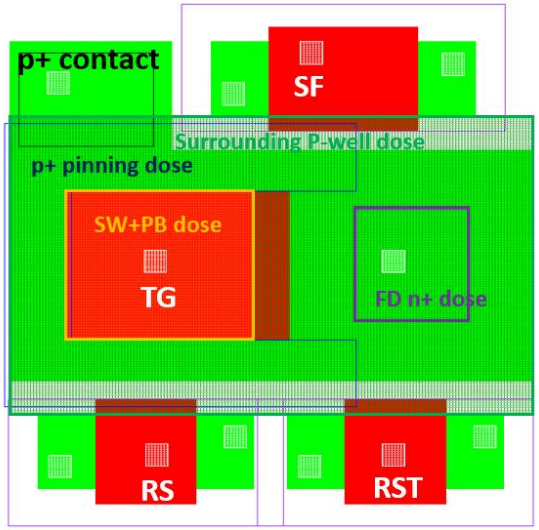
Pump gate charge transfer



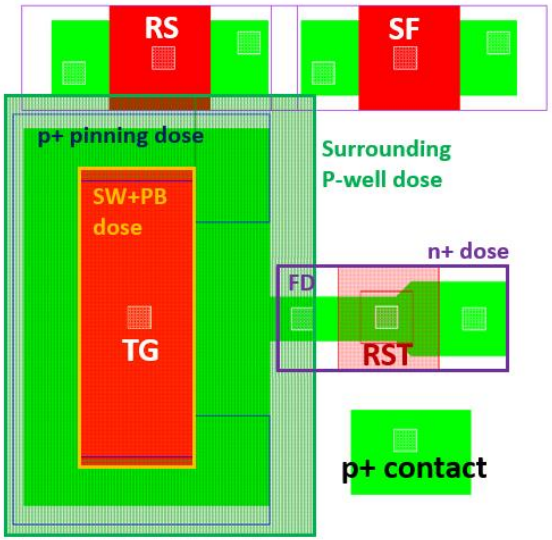




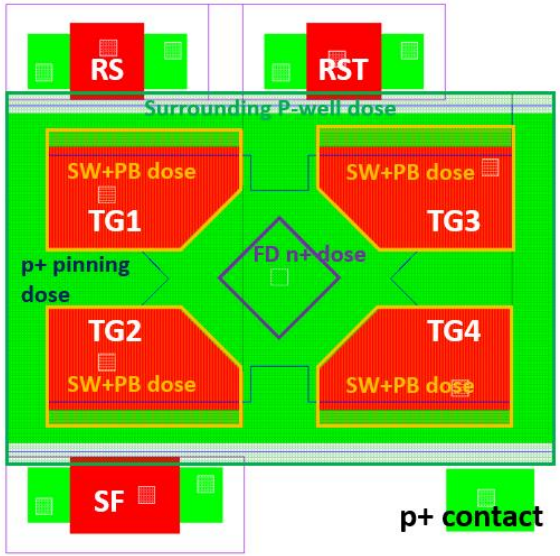
Tape-out chip with 65nm CIS process



Jot with pump gate TG
1.4um, FWC=200e-

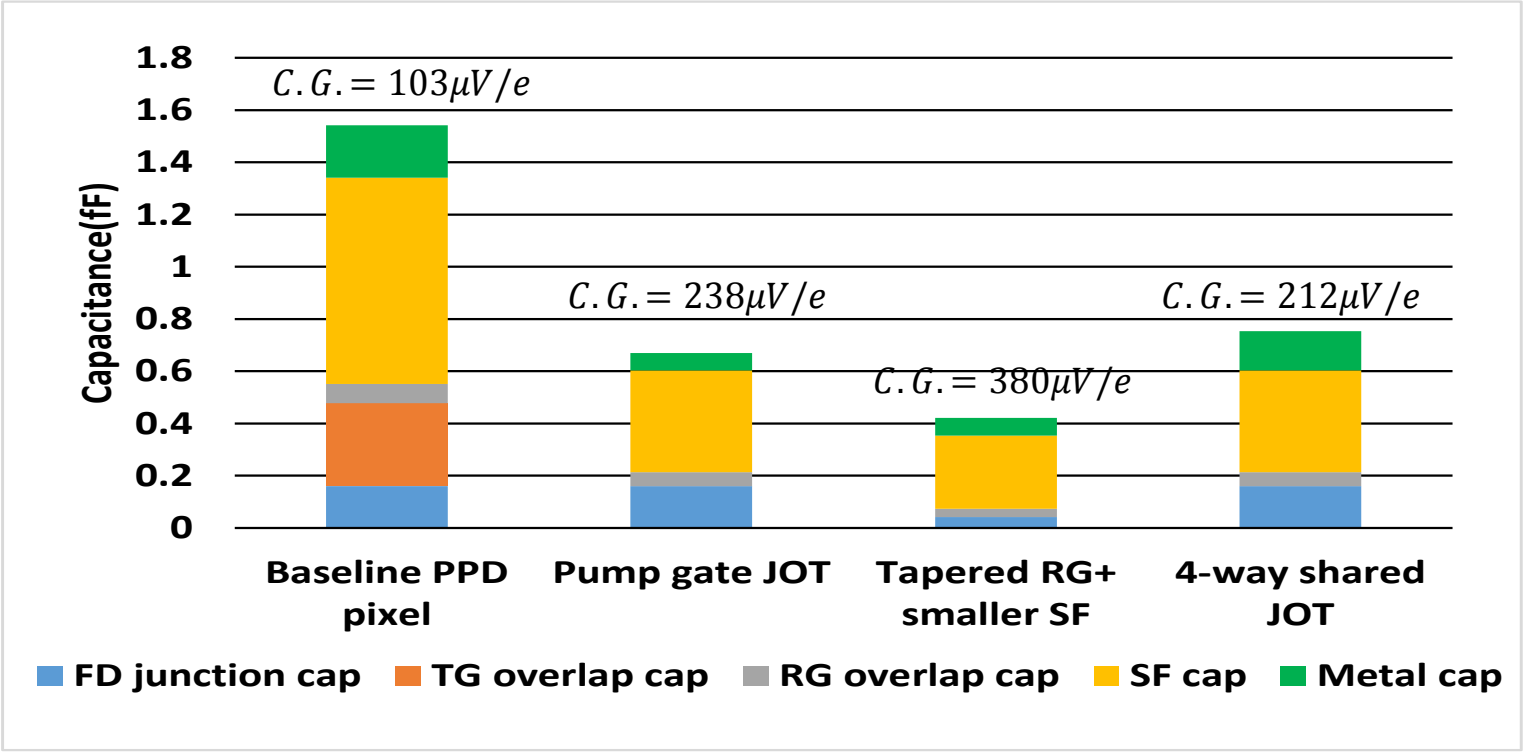


Jot with pump gate TG
and tapered RG
1.4um, FWC=200e-



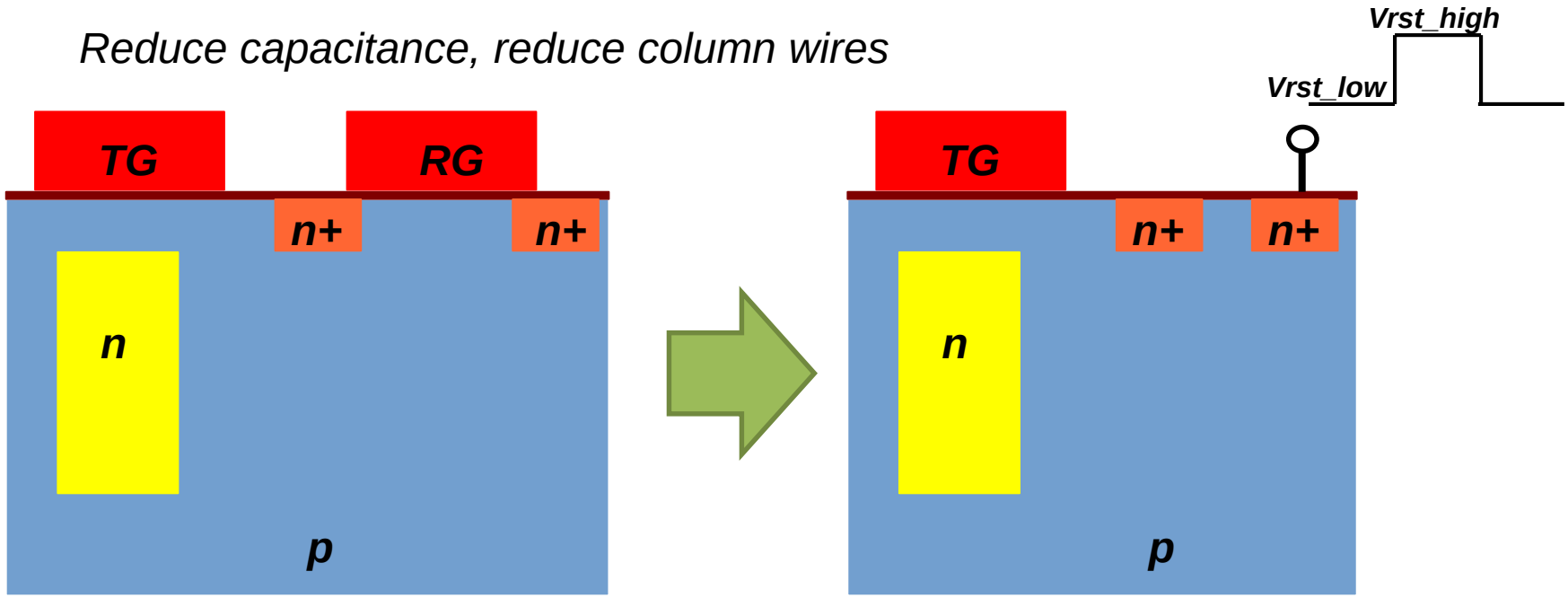
Jot with pump gate TG
and 4-way shared readout
1 um, FWC=200e-

Tape-out chip with 65nm CIS process

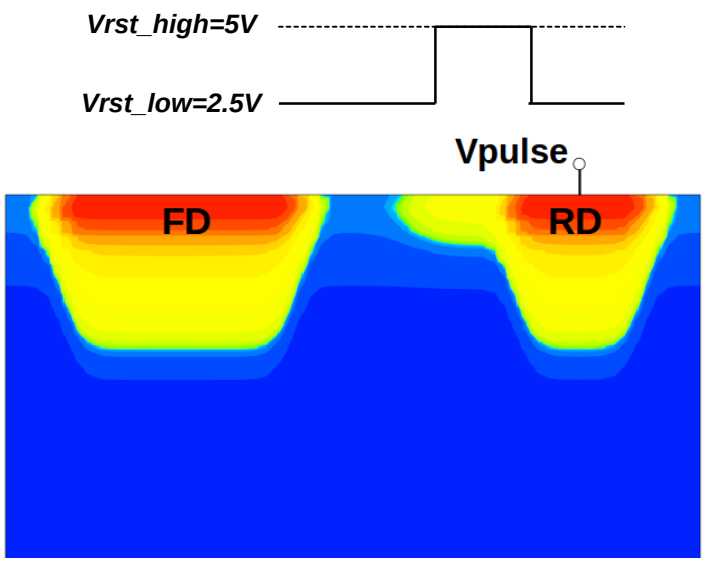


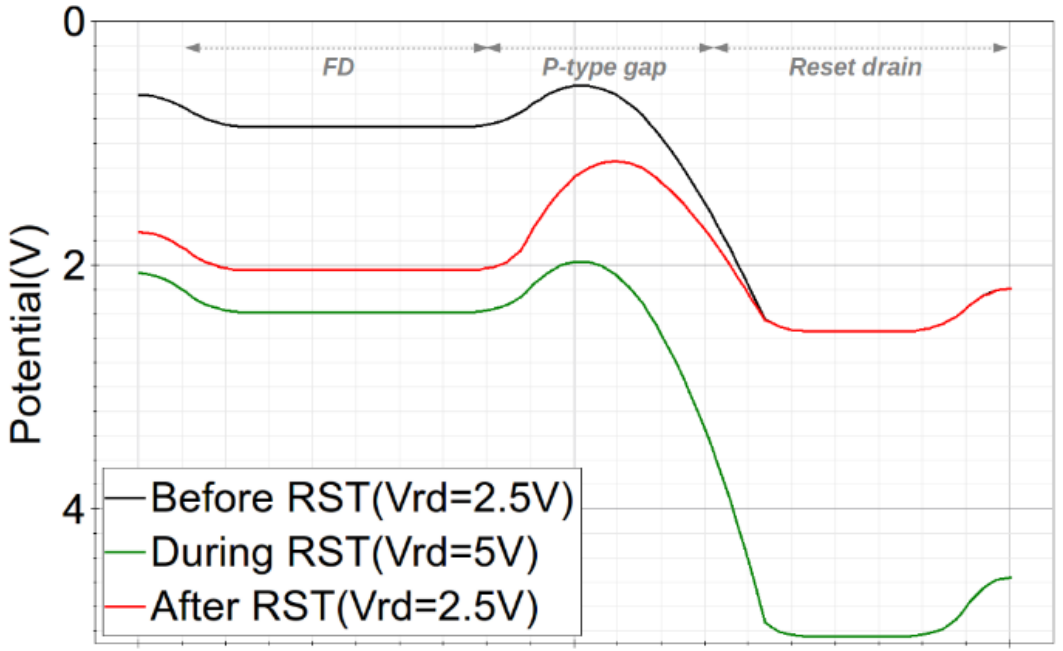
Gate-less Reset

Reduce capacitance, reduce column wires



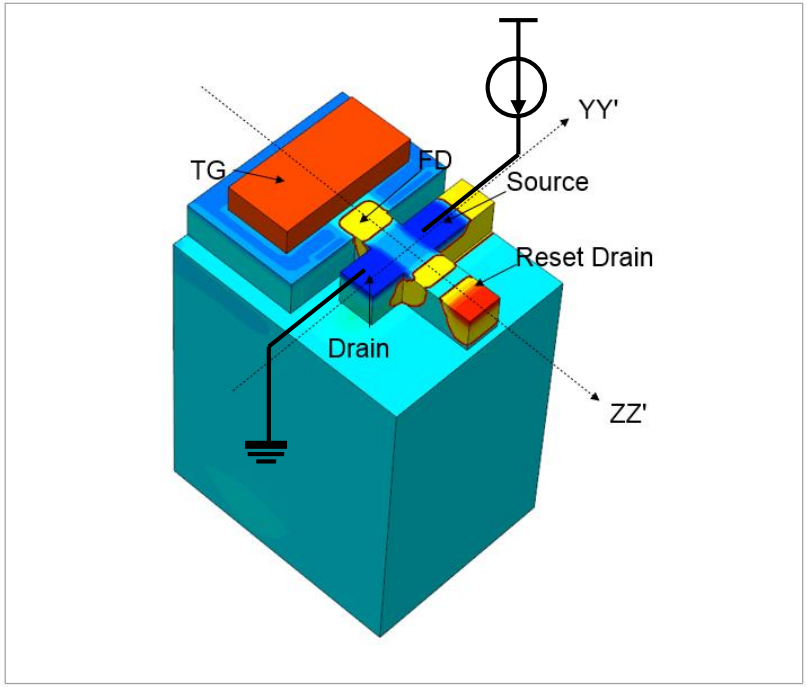
Gate-less reset

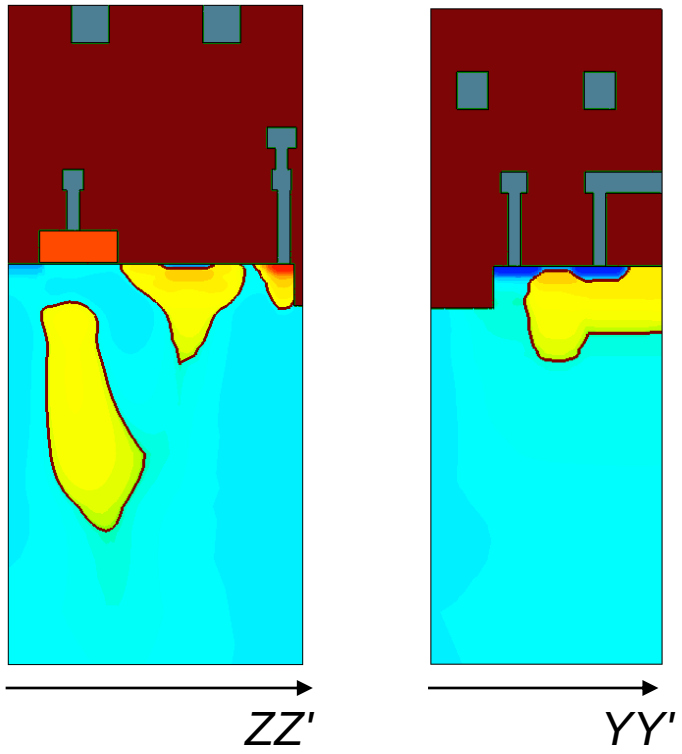




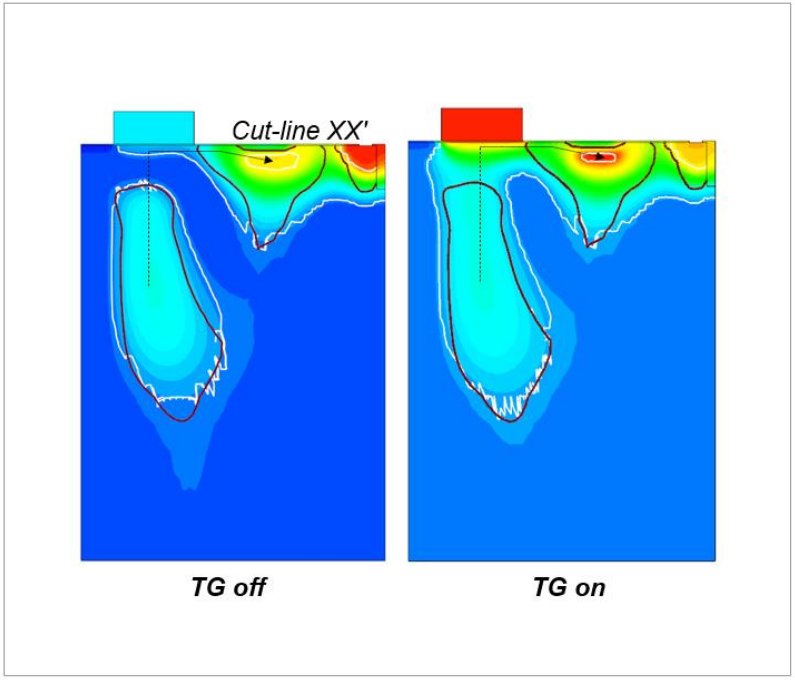
JFET source follower with FD being the virtual gate

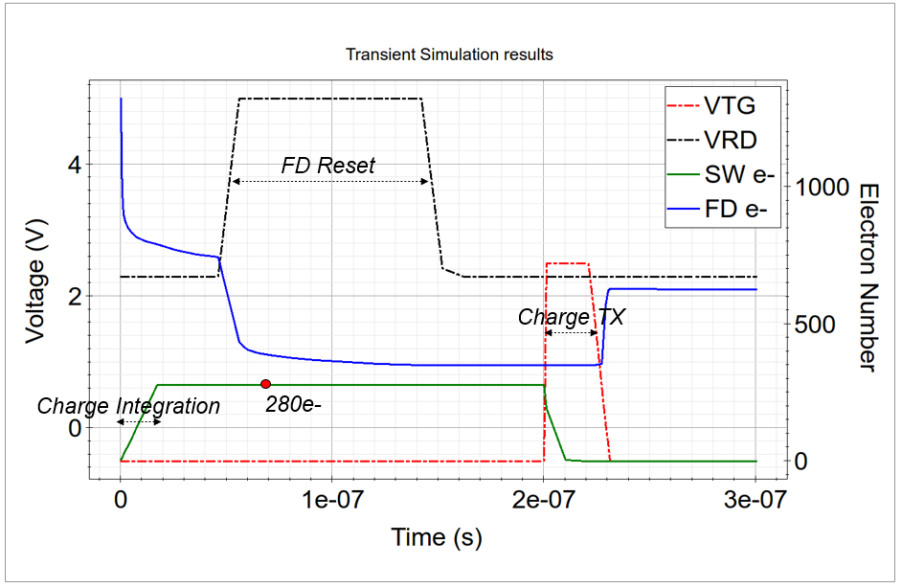
Reduce capacitance, reduce readout noise





JFET source follower with FD being the virtual gate





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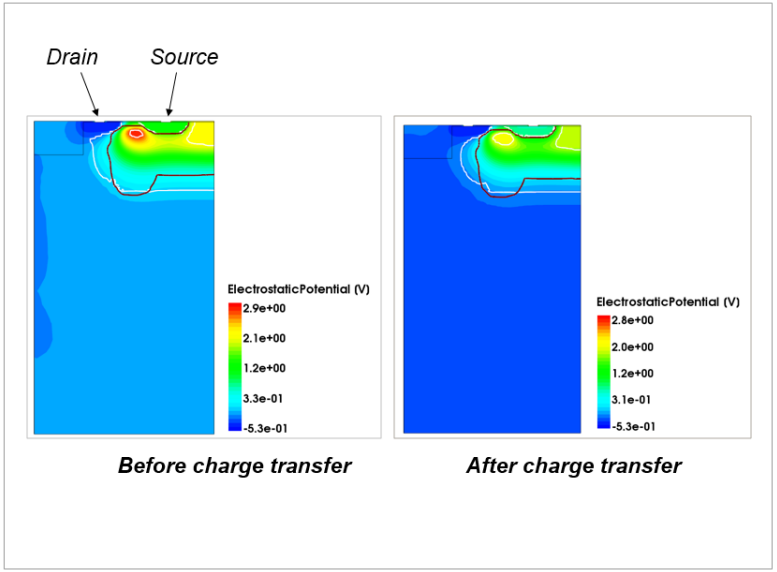

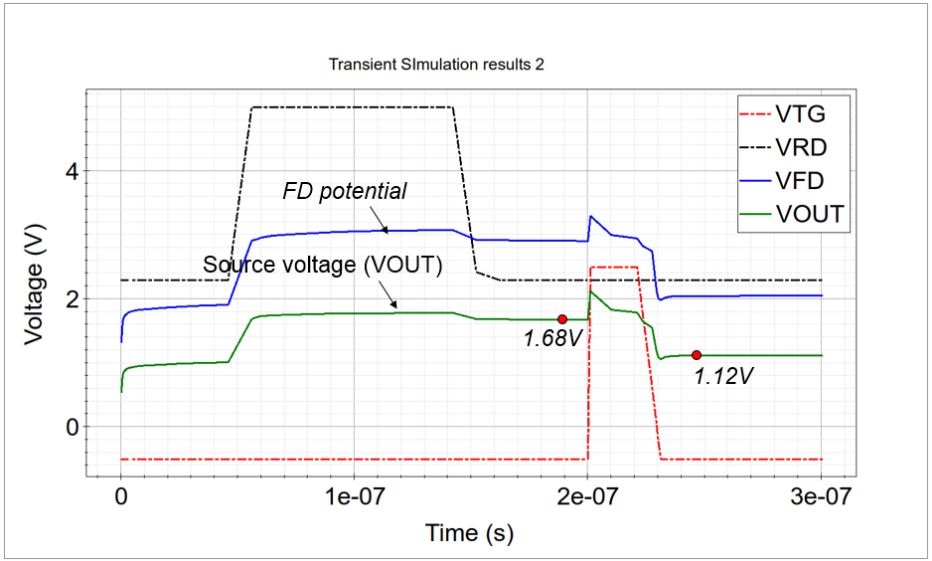

Jot device summary

	Jot	Target
Size	800nm(12L)	650nm*
Storage Capacity	100e-	1-100e-
Conversion Gain	1.7mV/e-	>1mV/e-
Read Noise	Waiting for test results	0.15e- rms

65nm CIS process

Reference

- E.R. Fossum, ***The Quanta Image Sensor (QIS): Concepts and Challenges*** (invited) in Proc. 2011 Opt. Soc. Am. Topical Meeting on Computational Optical Sensing and Imaging, Toronto, Canada July 10-14, 2011.
- J.J. Ma, D. Hondongwa, and E.R. Fossum, ***Jot Devices and the Quanta Image Sensor***, (invited) in Technical Digest of the 2014 IEEE International Electron Devices Meeting (IEDM), pp. 247-250, San Francisco, CA December 15-17, 2014.
- J.J. Ma and E.R. Fossum, ***A Pump-Gate Jot Device with High Conversion Gain for Quanta Image Sensors,*** IEEE J. Electron Devices Society, Vol. 3(2), pp. 73-77, March 2015.

Thanks for your attention!