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Quanta Image Sensor (QIS): Early Research Progress

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Abstract: Early research progress in the realization of the Quanta Image Sensor is reported. Simulation of binary data acquisition and image formation was performed. Initial analysis and simulation of a readout signal chain has been performed and bounds on power dissipation established. Photodetector device concepts have been explored using TCAD. (Invited[1])
OCIS codes: (040.0040) (040.5160) (100.2550) (110.0110) (110.2970) (120.1880) (250.0040)

I. Introduction

The Quanta Image Sensor (QIS) was first proposed in 2005 in conjunction with an algorithm to form a "digital film sensor." [1,2] Advances in SPAD devices [e.g., 3] and binary pixel theory and imaging algorithms [e.g., 4] have been made since then, and the ensemble of work has encouraged us and our sponsor to engage in a research program to investigate methods to realize binary pixels, photoelectron counting and the QIS. Key elements of this research include sub-electron read noise, high scan rates, massive binary data handling, and low power dissipation. Investigating methods of creating high quality images from the binary data is another part of the effort.

The QIS is comprised of an array of specialized binary pixels called jots that provide sensitivity to a single photoelectron. To improve the storage capacity of the sensor (bits/um^2) jots are anticipated to be sub-diffraction-limit (SDL) in size (e.g., 100-200 nm pitch). To improve SNR and dynamic range, the readout scan rate of the jot array may be 16x or higher than that of conventional image sensors (e.g., 480 or 960 fields per sec.). Thus a QIS may consist of 0.1-100Gjots with data rates from 0.1-100Tbits/s.

II. End-to-end system simulation

Generating The Jot Data Cube

Modeling of the QIS system starts with simulating the acquisition of binary jot data. The data can be artificially generated from existing images. A standard 256x256 image was used ("Lena"). Each pixel was converted to *sxs* subpixels using bicubic interpolation. Each subpixel was then converted to a binary jot value (0,1) using Poisson statistics [5]. The process is repeated *m* times (e.g., *m*=16) to generate *m* time slices of jot data. Starting with an original image of 256x256 pixels yields a binary jot data cube (x,y,t) of 4096x4096x16 bits. Essentially each original pixel has been translated to 16x16x16 jots.

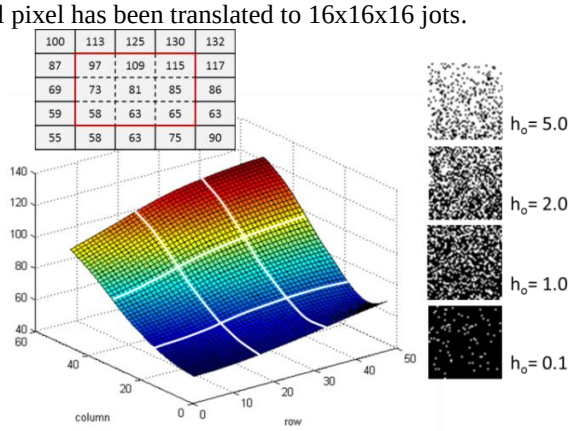

Fig. 1. Example of 3x3 pixels from original image interpolated to 48x48 subpixels, and jot data corresponding to 48x48 jots for 4 different exposure settings.

Read noise and dark current noise corruption can be included in the jot data cube. The bit error rate (*BER*) – the probability of a bit flip - is determined from the signal chain input-referred read noise n_r according to:

$$BER = \frac{1}{2} erfc\left(\frac{1}{\sqrt{8}n_r}\right) \qquad (1)$$

Generally, we target QIS design with *BER* less than 0.001 corresponding to $n_r \cong 0.15$ e- rms. Dark bits from thermally generated electrons are expected to be below this rate but can be included in the total *BER* for simulation.

[1] *This paper is a shortened version of work by the authors appearing in the Proc. 2013 Int. Image Sensor Workshop (IISW), Snowbird, Utah, USA June 12-16, 2013.*

Image Formation

The simplest method, perhaps, to form an image from the jot data cube is to sum the binary data over some region to form each pixel where *jxj* is the number of jots utilized in *x* and *y* to create the reconstructed pixel (e.g., 16x16, 4x4, or even 2x2). For the case of 16x16, the maximum sum is 4096. For 4x4, the maximum sum is lower and the shot noise is proportionally higher.

In essence, the summation approach is equivalent sampling of a box filter convolution, with filter weight of unity inside the box and zero outside. The filter weight need not be just binary in value. We have explored filter weights that result in a Gaussian-like distribution, but where the actual weights are weighted in powers of 2. An example of such a filter is shown below in Fig. 2. Results from the filter typically gave better results than simple summation and noise depends on the size of active kernel. Generally for output pixel pitch corresponding to *j* jots, a kernel size of 2*j* gave the best trade between spatial resolution and noise.

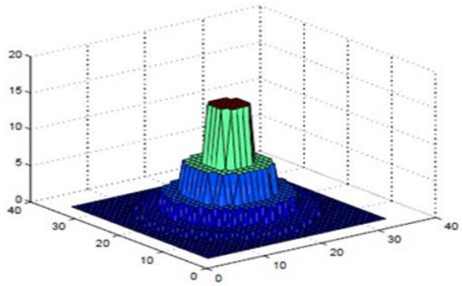

Fig. 2. Example of binary-power-weighted pseudo-Gaussian filter extending over 32x32 jots for 16 jot output pixel pitch.

Many different filters were explored with varying degrees of trade-off between modulation transfer function (MTF) and noise. Dynamic filters, where the kernel size is dynamically adjusted in accordance with spatial frequency in the output images, has been an interesting avenue, but requires more processing since it is a sort of recursive algorithm.

Synthetic Images

To quantify the relationship between noise and MTF, we created synthetic jot images based on ideal gray patches and spatial frequency patterns. An example of using the synthetic image as the starting point for exploring a digital film algorithm (basically, region-growing) is shown below. The results of each step are shown below in Fig. 3.

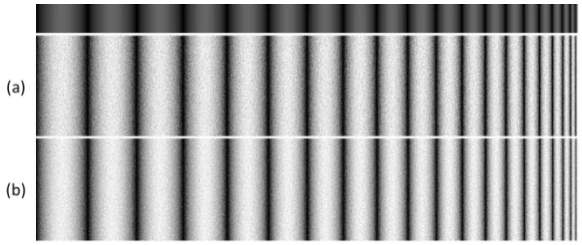

Fig. 3. (a) DFS algorithm (b) followed by dynamic-kernel-size pseudo-Gaussian filter (Original synthetic image shown at top for reference)

III. Readout signal chain simulation

Sense Amplifier

An early concern with the QIS concept was the required power dissipation for readout. To address this concern, design, simulation and layout of a strawman signal chain in 0.18 um CMOS was performed. A test chip is presently in fab.

To conserve power, a low power preamplifier [6] was adapted, followed by a D-latch. The preamplifer applies a gain of about 10 to the jot signal – enough to overcome threshold variations in the D-latch as determined by Monte-Carlo simulations. The design uses V_{DD}=1.8V, a column bias current of 3.6 uA and comparator power of 1.3 uW. Simulation shows that for 100 fps readout (10k jots per column) or 1Mj/s, the design achieves total power of 7.7 uW/column. For a 0.1 Gjot sensor (10k x 10k) this corresponds to 77 mW for 10Gb/s internal readout of the array. Of course any digital signal processing will add to the total power, and off-chip drive of data, if not compressed, will add significantly to the power budget.

Scaling

Scaling of the design results using normal scaling rules was performed [7-9]. The results of scaling are shown below in Fig. 4. Using the present approach with scaled designs in 16:9 aspect ratio, array power can become large at 1 Gjot (1 Tb/s) and prohibitive at 10 Gjot (10 Tb/s). Improved architectures for power reduction are being pursued and an order of magnitude reduction in power is considered possible.

Process	V_{DD}	Jot array	Column Speed	Column power	Comp power	Total	Array Power
CURRENT DESIGN							
0.18um	1.8V	0.001 Gjots (1k X 1k)	1MJ/s (1000fps)	0.71uW	1.28uW	1.99uW	1.99mW
0.18um	1.8V	0.1 Gjots (10k X 10k)	1MJ/s (100fps)	6.44uW	1.28uW	7.72uW	77.2mW
SCALED DESIGN							
0.18um	1.8V	0.1 Gjots (10k X 10k)	10MJ/s (1000fps)	64.4uW	12.8uW	77.2uW	772mW
45nm	1.1V	1 Gjots (24k X 42K)	24MJ/s (1000fps)	57uW	2.9uW	59.9uW	2.5W
22nm	0.8V	1 Gjots (24k X 42K)	24MJ/s (1000fps)	20uW	0.74uW	20.74uW	0.87W
45nm	1.1V	10 Gjots (75k X 133k)	75MJ/s (1000fps)	553uW	9uW	562uW	75W
22nm	0.8V	10 Gjots (75k X 133k)	75MJ/s (1000fps)	197uW	2.3uW	199.3uW	26.5W

Fig. 4. Projected power in scaled designs.

IV. Jot design

There are many interesting avenues to explore for jot implementation [2] and many early 1T or 2T active pixel technologies can also be considered [e.g., 10,11]. Presently we are investigating two approaches congruent with current CMOS image sensor technologies. Our basic philosophy is to change as little as possible from what industry is making today. Both investigations are at an early stage and complicated by not having an actual baseline process flow at competitive technology nodes.

The first approach is scaling a 1.5T BSI CMOS APS (shared readout) to meet the size, conversion gain and noise requirements of a jot. In the second approach, we are considering a bipolar transistor structure with the base fully depleted and used to store the photocarrier(s) (electron or hole).

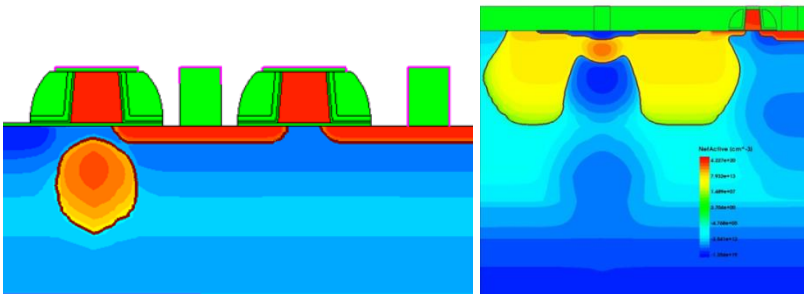

Fig. 5. Screen shot of work in progress on two candidate structures for jot implementation.

V. Conclusions

Creating a practical realization of the Quanta Image Sensor involves a plenitude of fun problems to solve. However, initial work has revealed many of the critical challenges and is starting to yield approaches to conquer those challenges. The research is still at an early stage.

VI. Acknowledgments

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VII. References

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