A 3-Pin 1.5 V 550 μW 176 x 144 Self-Clocked CMOS Active Pixel Image Sensor

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ABSTRACT
This paper addresses the development of a micropower 176 x 144 self-clocked CMOS active pixel image sensor that dissipates one-to-two orders of magnitude less power than current state of the art CMOS image sensors. The chip operates from a 1.5 V voltage source and the power consumption measured for the chip running from an internal 25.2 MHz clock yielding 30 frames per second is about 550 μW. This amount enables the sensor to be run from a watch battery. It is believed that this chip is the world's lowest power image sensor and the first image sensor designed for a watch battery operation. The camera-on-a-chip operates as a self-clocked 3-pin sensor (GND, VDD (1.2 - 1.7 V), and DATAOUT). The die occupies 4 mm^2 of silicon.

Keywords
Active Pixel Sensor, Image Sensor, CMOS, Low-Power, Low-Voltage, Self-Clocked.

1. INTRODUCTION
Low-power consumption is a fundamental demand for battery-operated devices [1,2] such as cellular phones, portable digital assistants (PDAs), and wireless security systems. Cellular videophones that emerge on the market will utilize state-of-the-art CMOS image sensors consuming 5-30 mW of power. The requirements of the next generation of portable devices to components are expected to be more stringent in terms of power and size.

In traditional CCD based imaging systems, at least one companion chip is required to generate timing, adjust gain, perform analog-to-digital conversion, color processing and image compression. Advanced CMOS technology and submicron design rules yield miniaturized systems-on-a-chip (SoCs) which integrate these multiple functions on the single imaging chip. CMOS systems-on-a-chip also benefit from local signaling which results in smaller interconnect capacitance and, hence, less power. Because the sensor is designed in standard CMOS, application specific functions can be readily embedded into the sensor and prototyping of the designs can occur rapidly at relatively low cost [3].

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This paper presents an image sensor which is a prototype of a future generation of micropower image sensors that consume less than 1 mW of power. This value is one-to-two orders of magnitude less than the power in current state of the art CMOS image sensors. The chip is designed for 1.2 - 1.7 V operation, supposedly from one battery, and dissipates 550 μW. The image sensor architecture and analog and digital blocks used in this micropower CMOS active pixel image sensor are described in details in section 2. Summary of a low-voltage sensor design methodology is given in the next section. The final part of the paper deals with the results of the sensor characterization and discussions on internal on-chip clock generation issues.

2. SENSOR CHIP ARCHITECTURE
The sensor's block diagram is shown in Figure 1. The core pixel array consists of 176 (H) x 144 (V) photodiode active pixels [quarter common intermediate format (QCIF)] with a 5 μm pitch. The array of pixels is accessed in a row-wise fashion using a shift register and row driver with a reset bootstrapping circuit so that all pixels in the row are read out into column analog readout circuits in parallel. Each of the 176 column-parallel readout circuits performs both sample-and-hold (S/H) and delta double sampling (DDS) functions, eliminating pixel offset variations and pixel source-follower 1/f noise. The signal is stored in the charge domain. The global charge-sensitive amplifier at the front end of the analog-to-digital converter (ADC) provides a fixed gain for the column charges being read using the column select logic. The amplifier reset and the amplifier signal values are sent to the 8-bit self-calibrating successive approximation ADC. The ADC generates the 8-bit digital output. The digital timing and control logic block generates the proper sequencing of the row address, column address, ADC timing, as well as generates the synchronization pulses for the pixel data going off-chip. The on-chip clock generator generates an internal clock with on-chip bandgap reference circuitry and power-on-reset circuit for the timing and control logic.

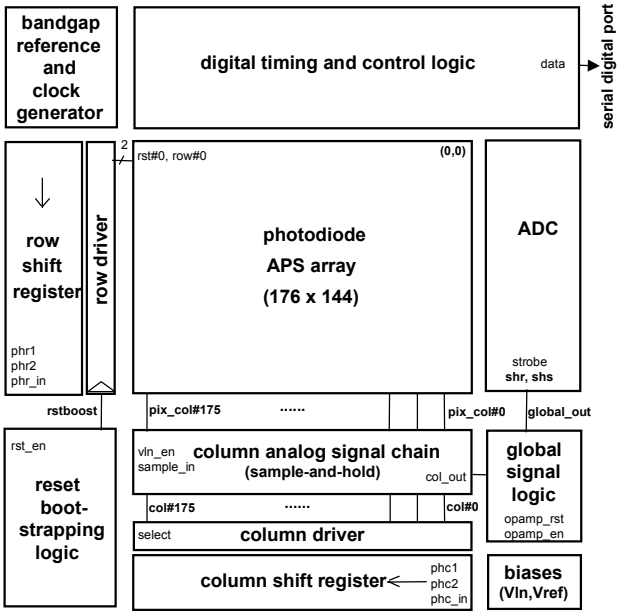

Figure 1: Sensor's block diagram.

A signal path from pixel to ADC is shown in Figure 2.

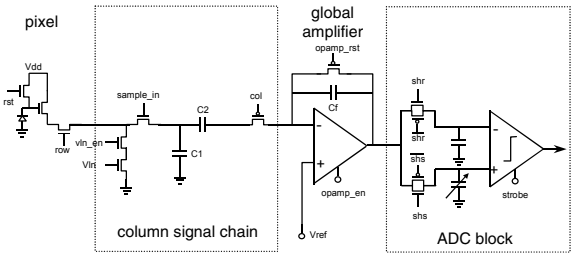

Figure 2: Pixel to ADC signal path.

A photodiode pixel is the sensing structure used for this micropower image sensor. Increasing the amplitude of the *rst* signal to *Vdd + threshold voltage* using the bootstrap switch circuit adopted from [4] should increase the pixel reset voltage and extend the pixel dynamic range.

The biasing for each column's source-follower is 1.4 µA permitting charging of the sampling capacitors in the allotted time. The source-followers can then be turned off by *vln_en*. Once *row* and *sample_in* switches are selected, the photogenerated pixel signal value is stored in the column capacitors *C2* clamped to an operational transconductance amplifier input voltage *Vref*. After resetting the pixel, the pixel reset value is stored in the capacitor *C1*, and the difference between pixel reset and signal is stored in the capacitor *C2*. The charge difference between pixel reset and signal is transferred to the operational amplifier by turning on *col* switch.

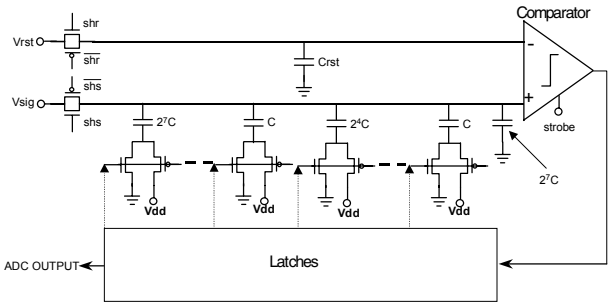

Figure 3: Low-power 8-bit successive approximation ADC.

The low-power 8-bit successive approximation ADC is shown in Figure 3. The ADC consists of a capacitor bank, a comparator, decision latches, and correction latches. In the current implementation we use the rail supply voltage *Vdd* as the ADC reference voltage and PMOS switches to connect this voltage. An extra capacitor 2^7C is for the adjustment of effective ADC reference voltage $Vref_{adc}$. The effective ADC reference voltage in Figure 3 can be

$Vref_{adc} = Vdd\ (C_{conv} / C_{tot}) = 0.61\ Vdd,$

where $C_{conv} = (2^8\text{-}1)C$ and $C_{tot} = (2^8+2^7+2^5\text{ -}2)C$.

The calibration portion of the ADC serves to eliminate the dynamic comparator offset, which is typically 30mV. It has 5 capacitor bit cells. The main ADC conversion uses 8 binary-scaled capacitors to sample the amplifier signal and reset capacitor to store the amplifier reset voltage. These capacitor networks are connected to the input of the comparator. After saving these signal and reset voltages on the top plate of the capacitors, the bottom plates are successively connected to *Vdd*. The comparator output determines whether or not the signal side maintains the updated signal in the top plate. During the convergence process, the variable signal is matched to a fixed amplifier reset voltage *Vref*. Not only does this allow the use of a limited input swing comparator, but it causes the comparison to happen at the same level each time, eliminating the potential comparator offset vs. signal dependence.

The 3-stage ring oscillator as an on-chip clock generator is used as shown in Figure 4. Clock power *Vclock* comes from on-chip bandgap reference circuitry. The output voltage $Vref_{conv}$ of the conventional bandgap reference is 1.25 V. This fixed output voltage of 1.25 V limits the low-voltage operation. So we need to think about a bandgap reference that can successfully operate with sub-1.2 V supply [5]. Figure 4 shows the low-voltage bandgap reference circuit. The output voltage of this low-voltage bandgap reference circuit becomes

$$Vref_{low\_voltage} = R4\left(\frac{Vf1}{R2} + \frac{dVf}{R3}\right) = \frac{R4}{R2} Vref_{conv},$$

where *Vf1* is the built-in voltage of the diode, and *dVf* is the forward voltage difference between diode *D1* and *N* diodes *D2* with proportional to the thermal voltage, respectively.

Therefore $Vref_{low\_voltage}$ as *Vclock* can be freely changed from $Vref_{conv}$ and *Vdd* can be lowered below 1 V if the amplifier is properly working. The signal *rstb* is generated by power-on-reset circuitry as shown in Figure 4. A power-on-reset circuit provides the stable generation of a reset signal without being affected by the rising characteristic of a power-supply voltage. This power-on-reset circuit includes two MOSFETs (*M1* and *M2*), a capacitance (*C*), and two inverters. In the power-on-reset circuit, *M1* is acted as the resistance *R* with a large threshold voltage and *M2* is a pull-down switch, the reset signal is determined by the difference of threshold voltages between *M1* and *M4* in the first inverter and *RC* constant of *M1* and *C*.

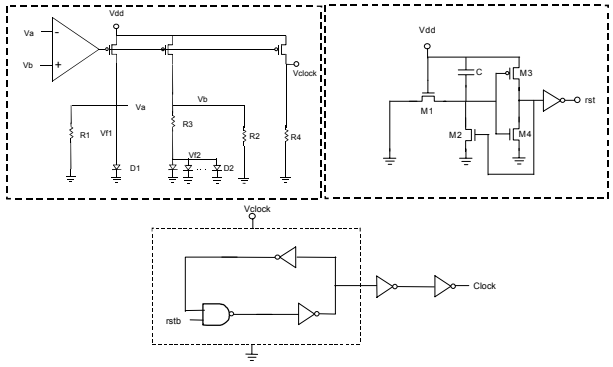

Figure 4: On-chip clock generator.

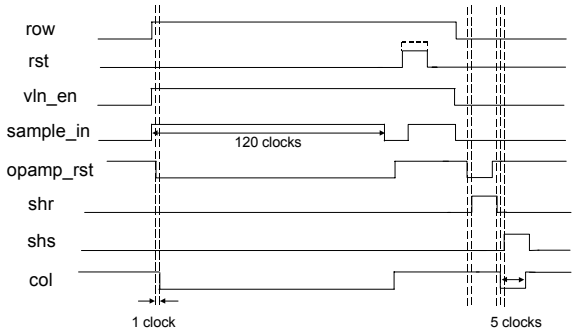

Figure 5: Relative row and column timing.

Figure 5 shows the relative timing for row and column operation of the sensor. At 30 frames per second, the sensor is clocked from a 25.2 MHz source. The total row time at this frame rate is 231.1 μsec ((192 + 176 x 32) clocks). This period is divided between the time required for column analog operations (192 clocks) and the ADC conversion time (32 clocks). The analog readout sequence starts with the selection of a pixel row, whose output is sampled onto the column S/H capacitor in parallel. Each ADC processing time is the global S/H (16 clocks) and the ADC conversion (16 clocks). At the full 30 Hz frame rate, the ADC used in this sensor needs to operate at 0.75 Msamples/sec. The ADC is calibrated at the beginning of the very first frame for compensating the DC offset at the input of the comparator.

3. Low-Power Techniques

Low-power design methodology is considered at all levels – technology, circuit and logic, architecture, algorithm, and system integration. Figure 6 summarizes low-power design steps from process technology to system integration.

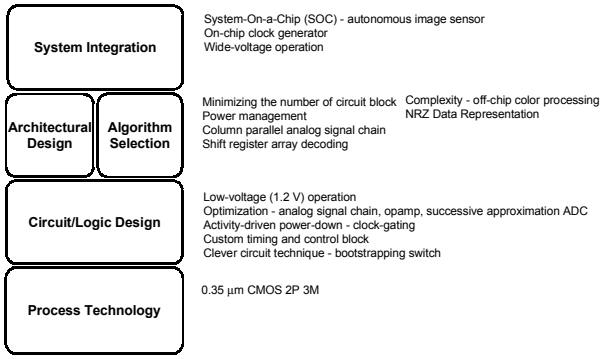

Figure 6: Low-power design steps in this research.

For power reduction through process technology, generally digital circuitry can have a benefit most from the next generation technology such as area, speed, and power performance. From the scaling laws, the most advanced technology is needed for low-power consumption. However, CMOS image sensors are more performance sensitive than digital circuitry, thus they require a stable, well-characterized technology. From this point of view, a 0.35 μm CMOS technology is chosen as the preferred design technology.

For power reduction through circuit/logic design, reduction of the power supply voltage can be a key element in low-power CMOS image sensors. However, the design of a low voltage CMOS sensor involves several well-known challenges such as a) the reduced dynamic range of pixel, b) the low-voltage MOS switch problem, c) low-voltage opamp and ADC design, and d) low-power internal bias generation.

The challenges discussed above are addressed in the following way: a) the pixel voltage dynamic range is increased by using a bootstrapped reset pulse; b) the column analog readout circuit is designed so that only unipolar MOS switches are required. For instance, the S/H switch is of an n-type and is good for sampling pixel signals that are always "low". While the column select switch is of a p-type, which is good at connecting high level signals, such as for the reference voltage, etc.; c) the charge mode readout fixes the readout bus voltage so that the requirements on the amplifier input voltage swing are relaxed. On the other hand, an inverting current-mirror OTA used in this design yields almost rail-to-rail output and a capacitive ADC is selected so as to avoid some low-voltage design problems that would be faced with different types of ADC such as flash, pipelining, or folding converter; d) column readout circuits receive the reference voltage

from the readout opamp, eliminating the need for a power consuming reference voltage generator. In this case, the reference voltage is loaded only onto the high impedance opamp input, so the *Vref* voltage source can be implemented as a high-resistance one. Also power supply *Vdd* is used for ADC reference voltage, which is eliminating the need for a power consuming ADC reference voltage generator.

In addition, the following measures have been undertaken to reduce the sensor power. First, unused blocks such as the pixel current load in the column circuit, and the comparator and opamp in the ADC have been cut from power during the time they do not operate. Second, the column S/H circuit does not have an active buffer. It was replaced with a passive capacitor storage.

For power reduction through architectural design, we reduce power consumption by reducing the chip function and utilizing the resource-sharing concept. Also the chip architecture is divided with selectively enabled blocks. For reducing the operation for decoding and execution, shift register array type is chosen. Although window and random access functions are sacrificed, which are not necessary in a small-format image sensor, shift register array type reduces the number of global buses.

For power reduction through algorithm selection, the operation and hence the number of hardware resources are minimized. The non-return-to-zero (NRZ) representation is chosen that reduce the bandwidth needed to send the pulse-code modulation (PCM) code.

For power reduction through system integration, the overall system pin requirement is reduced by combining functionality into system-on-a-chip. The master clock generator and other ICs such as digital and analog peripherals are integrated. At the system level, off-chip buses have capacitance C that is orders of magnitude greater than those found on internal signal lines in a chip. Therefore, transitions on these buses result in considerable system power dissipation. Hence, the signal-encoding approaches in literature achieve power reduction by reducing transition probability η while keeping C more or less unaltered. Also the system can be operated without a voltage regulator, there will be greater savings, but then a more variable supply voltage must be tolerated

4. TEST RESULTS

The sensor is implemented in a 0.35 µm, 2 P, 3 M 3.3 V CMOS process with Vtn = 0.65 V and Vtp = -0.85 V. The micrograph of the image sensor is shown in Figure 7. The size of the chip is about 2 mm x 2 mm, which includes the pixel array, row/column logic, analog readout, ADC, biases, on-chip clock generator, timing and control block, and 16 pads. This chip is packaged by 28-pin ceramic leadless chip carrier (CLCC).

The chip can operate autonomously with 3 pads (GND, VDD (1.2 - 1.7 V), DATAOUT). Also with an external master clock the chip can operate from 1.2 to 3.6 V power supply.

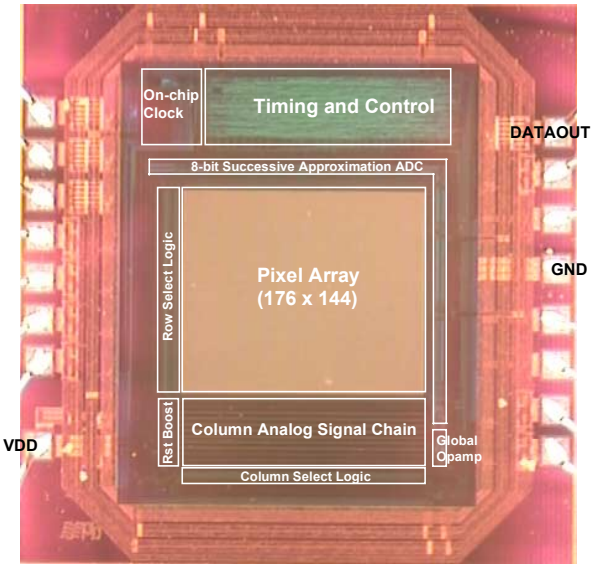

Figure.7: The micrograph of the image sensor.

Table I summarizes the sensor chip characteristics at 5 frames per second (fps) and 1.5 V power supply with the external 4.125 MHz clock.

Table I: Specification and measured sensor performance at 1.5 V and 5 fps.

Technology	0.35 µm, 2 P, 3 M CMOS
Pixel array size	176(H) x 144(V) (QCIF)
Pixel size and type	5 µm x 5 µm Photodiode APS
Pixel fill factor	30 %
Chip size	2 mm x 2 mm
Sensor output	8-bit serial digital
On-chip ADC	8-bit single successive approximation
ADC DNL/INL	1 LSB / 2 LSB
Conversion gain (pixel PD-referred)	34 µV/e-
ADC conversion gain	3.5 mV/LSB
Dark signal	6.97 LSB/sec or 24.4 mV/sec or 718 e-/sec
Saturation (pixel PD-referred)	253.2 LSB or 886.2 mV or 26,065 e-
Noise	0.85 LSB or 3.0 mV or 88 e- r.m.s.
Operating voltage	1.2 – 3.6 V
Maximum frame rate	40 fps
Maximum pixel readout rate	1 Mpix/sec
Power consumption	550 µW at 1.5 V, 30 fps, 16 pads

The measured power consumption of the overall chip, which includes the pixel array, row/column logic, analog readout, ADC, biases, timing and control block, on-chip clock generator, and pads, is shown in Figure 8 with the internal 25.2 MHz on-chip

clock (30 fps) from 1.2 to 1.7 V power supply. At 1.5 V, the measured power consumption is about 550 µW.

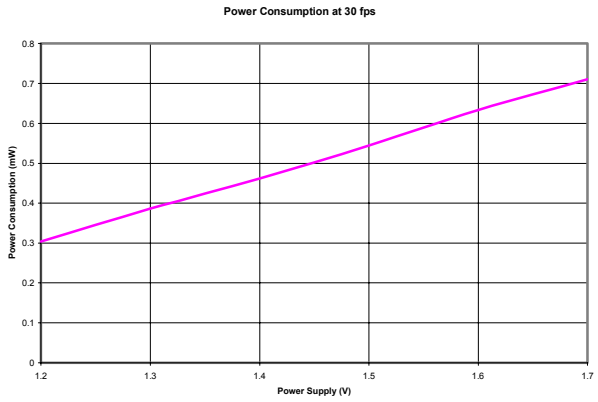

Figure 8: Measured power consumption at 30 fps from 1.2 to 1.7 V with 25.2 MHz on-chip clock.

The estimated overall chip power consumption is 547.5 µW at 1.5 V and 30 fps with the internal 25.2 MHz clock as shown in Table II. Note that the timing and control block consumes about half of total power. The measured power consumption of the overall chip is shown in Figure 9 with the external 16.5 MHz clock (20 fps) from 1.2 to 3.3 V power supply.

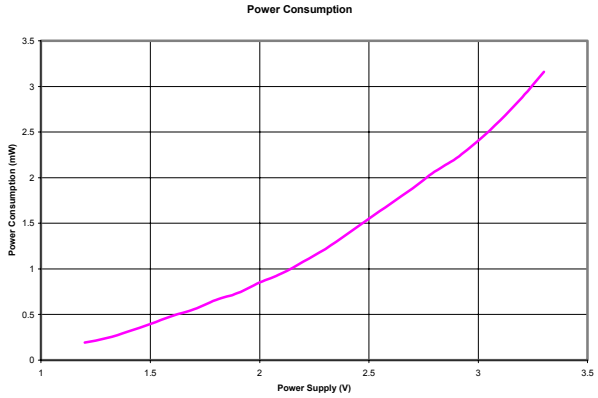

Figure 9: Measured power consumption with the external 16.5 MHz clock (20 fps) from 1.2 to 3.3 V power supply.

Figure 10 shows the measured power consumption of the overall chip at 1.5 V and 2.7V power supply for different frame rates.

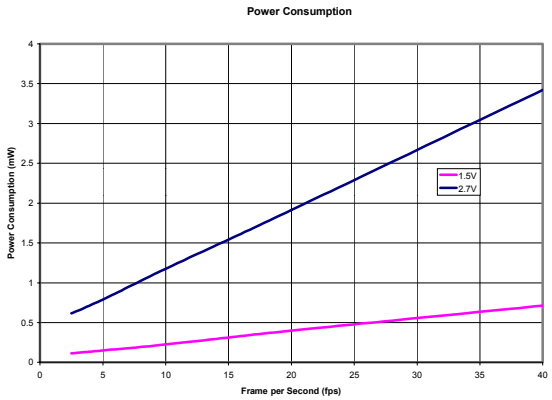

Figure 10: Measured power consumption at 1.5 V and 2.7 V power supply for different frame rates.

Images taken with the sensor at 30 fps (25.2 MHz on-chip clock) with 1.5 V and 1.7 V power supply are shown in Figure 11. Also images taken with the sensor at 20 and 40 fps with 1.5 V power supply and external clock are shown in Figure 11.

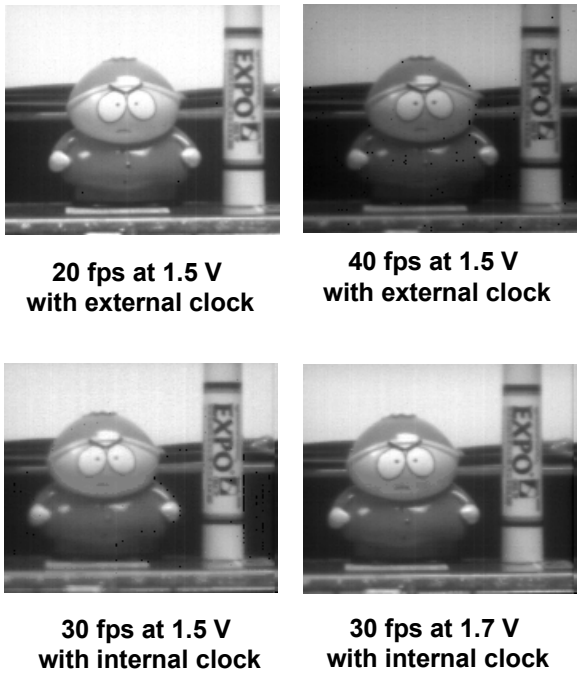

Figure 11: Test images

We use the 3-stage ring oscillator as an on-chip clock generator with clock power from the on-chip low-voltage bandgap reference circuitry. The on-chip low-voltage bandgap reference circuitry

generates 0.9 V at 1.5 V power supply. Measurement result is shown in Figure 12. On-chip clock frequency shows from 26 MHz to 22.5 MHz with respect from 1.7 V to 1.1 V, which is corresponding less than 15 % variation. This means bandgap reference circuitry generates less than 5 mV variation from 0.9 V, which is less than 1 % variation.

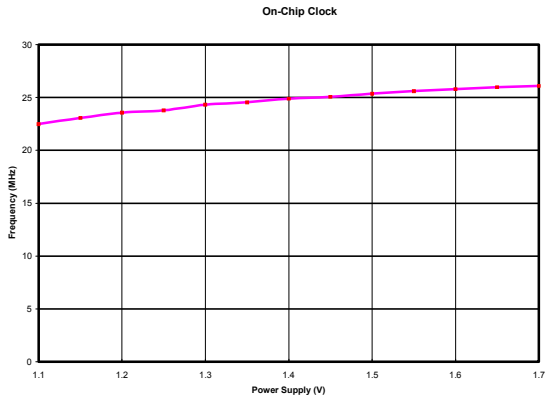

Figure 12: Measured frequency response of on-chip clock generator.

5. CONCLUSION

An active pixel image sensor designed for 1.2 – 1.7 V operation with an on-chip clock generator and 1.2 – 3.6 V operation with an external clock to provide 176 (H) x 144 (V) QCIF 8-bit monochrome video was presented. As a self-clocked sensor, it can be operated with only 3 pads (GND, VDD (1.2 - 1.7 V), DATAOUT). The measured power consumption of the overall chip with the internal 25.2 MHz on-chip clock (30 fps) at a 1.5 V power supply is about 550 µW. Low-voltage image sensor techniques have been successfully tried and the possibility has been shown of wide voltage-range operation (1.2 - 3.6V). This sensor moves us closer to the realization of the 'Dick Tracy' video watch because of its ability to run on a watch battery and its tiny footprint. It is the world's lowest-power CMOS image sensor, and it is expected that the technology will lead to exciting new kinds of wireless digital cameras.

6. ACKNOWLEDGMENTS

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Table II: Estimated chip power portfolio with 30 fps at 1.5 V power supply.

Main components	Current (µA)	Quantity	Average current (µA)
Column analog signal chain (vln^)	1.4	176 x (1/50)^^	5
Global opamp	30	1 x (1/2)^^	15
ADC (comparator)	16	1 x (1/4)^^	4
Biases (Vln + Vref)	16	1	16
Peripheral (row & col logic + rst bootstrapping circuit + drivers)	20	1	20
Clock generator	75	1	75
Timing and control	170	1	170
Dataout	60	1	60
Total Current (µA)		365	
Total Power (V x I) (µW)		1.5 x 365 = 547.5	
^ peak current : 220 µA ^^ duty cycle factor			