TP 6.5: 128Mb/s Multiport CMOS Binary Active-Pixel Image Sensor

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A 128x128 photo-diode active pixel sensor (APS) with an on-chip array sequencing controller and 1b thresholding circuitry processes 8,192-frames/s at a 128Mb data rate onto a 8b wide parallel-digital output port. In addition, the on-chip controller can be commanded to output data through either a serial digital port for lower bandwidth requirements or through a serial analog port for higher-resolution off-chip analog-to-digital conversion.

The sensor chip is for a real-time helicopter oil debris monitoring system requiring the sensing and processing of 1,024 laser-strobed snapshot images per second of oil flowing through a transparent tube in the operating engine. The light exiting the tube opposite the laser source is projected onto the sensor leaving shadows where particles (e.g. metal chips or sand) in the oil obstruct the passage of light. Because of the high-contrast nature of the image,the analog pixel data is converted to only a 1b digital representation. This binary pixel data is sent off chip to a set of parallel processors performing particle discrimination.

The 4.3x4.5mm^2 image sensor uses a 1μm n-well standard CMOS process. All sensor array control and readout electronics are implemented on-chip. In each of the 128x128 active pixels there is a photodiode for collecting electrons generated by the laser source, a source follower for buffering the photodiode, a selection transistor for enabling the pixel source follower, and a transistor for resetting the photodiode. The pixel contains only n-channel transistors and is similar to previously reported pixel designs [1]. The photodiode is formed between a n+ diffusion and the p-type substrate. For this process the pixel is 16x16μm^2 and 31% of the pixel area is occupied by the photodiode n+ diffusion.

As shown in the chip block diagram in Figure 1, the active pixel array contains 128 rows and 128 columns (16k pixels). When a row is selected, active pixels in that row output data onto a shared column output through the pixel source follower. The datapath for a single pixel is shown in Figure 2. A pointer in the vertical 128b shift register (Figure 1) preloaded with a 1 is used by logic in each row to select a row of pixels and enable pixel reset for that row. For the digital output ports, per column output circuitry at the bottom of the array clamps pixel output data onto a capacitor and compares it to an externally applied threshold voltage (Figure 2). This thresholded pixel data is loaded into a register. The time for accessing a row of pixels, sampling the column onto the clamping capacitor, and performing the comparison is 1μs.

The on-chip controller in the lower left of Figure 1 then selects a byte at a time from the register for readout onto the 8b 16MHz parallel data output bus. To read out all 128b from the register requires 16 internal clock cycles for a total of 1μs at a 16MHz clock rate. In serial mode, the controller enables the register to shift the digital data out serially. As data from the register is read out, the next row in the array is being processed by the per column 1b conversion circuitry. In this pipelined process as the last of the bits from the register are read out, this next set of thresholded data is loaded. To read out all 128 rows of the array in the parallel port output mode requires 128μs (8kHz frame rate).

For the analog output ports, per column output circuitry at the top of the array clamps the pixel output data onto a capacitor that is connected to the gate of a source follower (Figure 2). A shift register located above the source follower selects the individual columns for readout through the analog port.

The on-chip control logic performs the array timing for the three modes of operation for the three different ports. Two chip inputs set the readout mode. In addition, there are control inputs to reset the control logic (to put the sensor into a known state at power up), a chip enable control to make the sensor pause between frames (not normally used), and a 16MHz clock. On-chip logic state machines sequence the array to generate the output data and control flags. The control flags signal the start of a frame and a row and also identify when the output data is valid. A signal is also generated at the end of a frame to command the laser to generate a pulse. Digital timing and control functions plus digital control for row/column circuitry comprise approximately 29,500 transistors as shown in Table 1.

The analog output port is used to characterize the pixel array (Table 1). The low sensor quantum efficiency is a factor of 4 to 5 times smaller than previous designs due to an opaque silicide on the photo-active n+ implanted regions (Figure 3). The maximum output response on the analog output port is 1.2V. Because there is no column-wise fixed-pattern noise (FPN) suppression circuitry, approximately 30mVpp of variation in analog output signal exists across the array for uniform illumination.

Images at a 30Hz frame rate from the serial analog port and parallel digital port are shown in Figures 4 and 5. At video-rate speeds the three separate output modes of the sensor function as expected. However, at much higher frame rates the parallel-digital output mode produces interline noise coupling that is believed to come from output-pad-to-substrate coupling.

To avoid digital-output driver noise coupling back into the comparator circuitry, the timing and control logic should disable output drivers during sensitive 1b thresholding. To offset the reduced time to read out the digital data from the chip due to this break in the pipelined sensor readout, the output bus bandwidth can be increased. An ASP micrograph appears in Figure 6.

Acknowledgments:

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Reference:

[1] Mendis, S., et al., "Progress in CMOS active pixel image sensors," Charge-Coupled Devices and Solid State Optical Sensors IV, Proc. SPIE, Vol. 2172, pp. 19-29, 1994.

0-7803-3136-2 / 96 / $5.00 / © IEEE

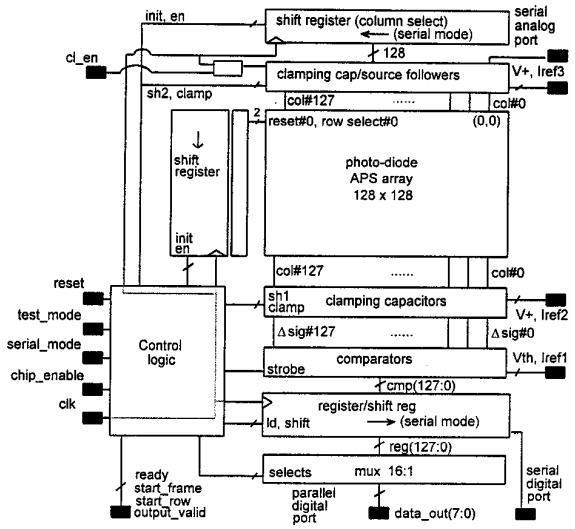

Figure 1: Multiport CMOS binary APS block diagram.

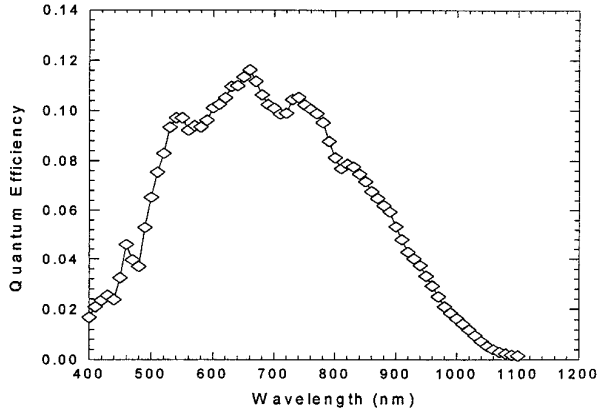

Figure 3: Sensor absolute quantum efficiency.

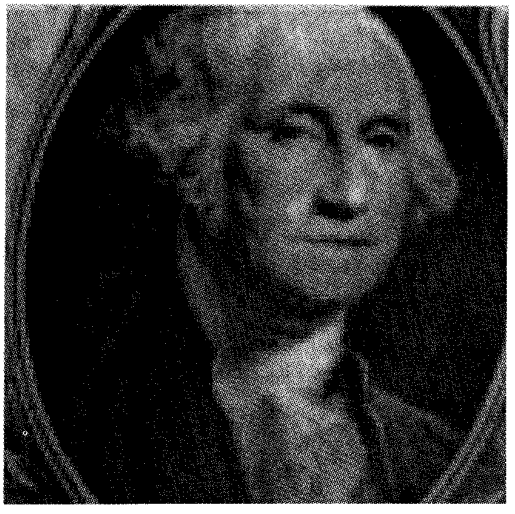

Figure 4: Serial-analog port data.

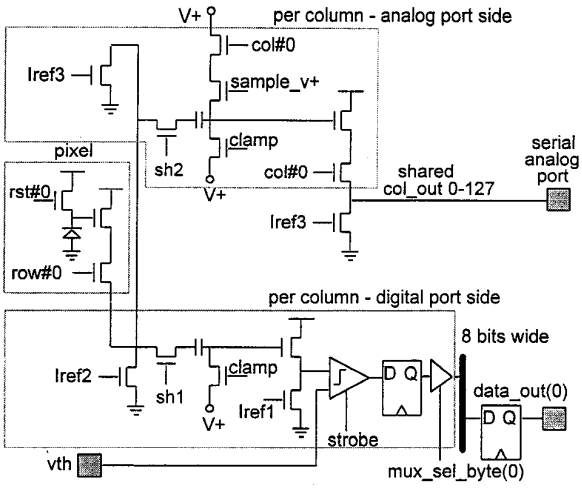

Figure 2: Circuit diagram of pixel datapath

Conversion gain	2.34μV/e⁻
Quantum efficiency at 660nm	0.12
Dynamic range	70.8dB
Saturation	1.2V
Dark rate	9.3mV/s
Fixed pattern noise	29.7mV
Fixed pattern noise, % of saturation	2.48%
Number of transistors:	
digital logic	29,518
analog circuits	3,983
pixel array	49,152
Total	82,653
Power: 5V supply	
analog mode(13.6Hz frame rate)	32mW
digital mode(1.5kHz frame rate)	100mW

Table 1: Multiport APS image sensor characteristics.

Figure 5: Digital-parallel port data.
Figure 6: See page 427.

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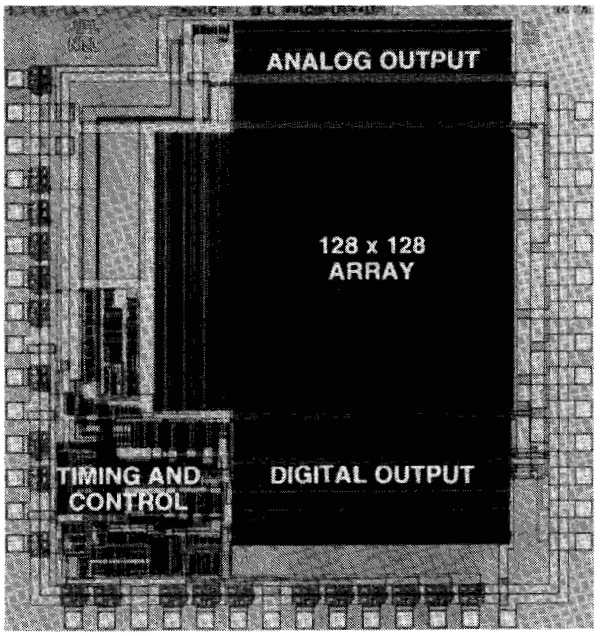

Figure 6: 128Mb/s multiport CMOS binary APS sensor micrograph.

FA 7.1: Custon ASIC VLSI Device for Asynchronous Transfer Mode (ATM)

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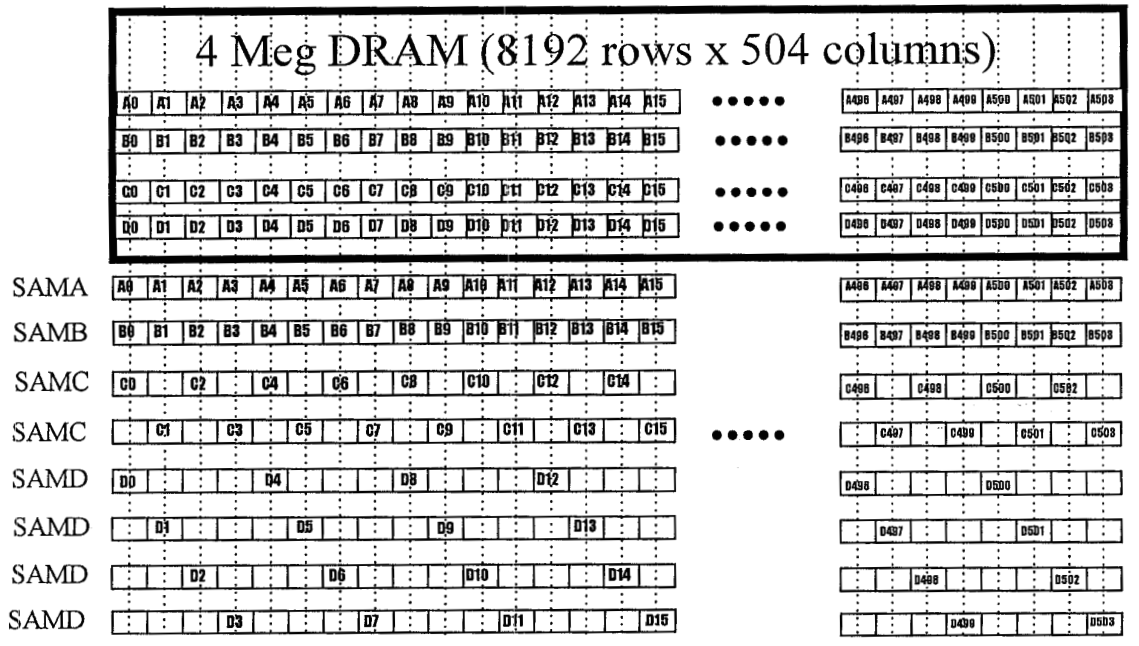

Figure 4: x4, x8, x16 modes.