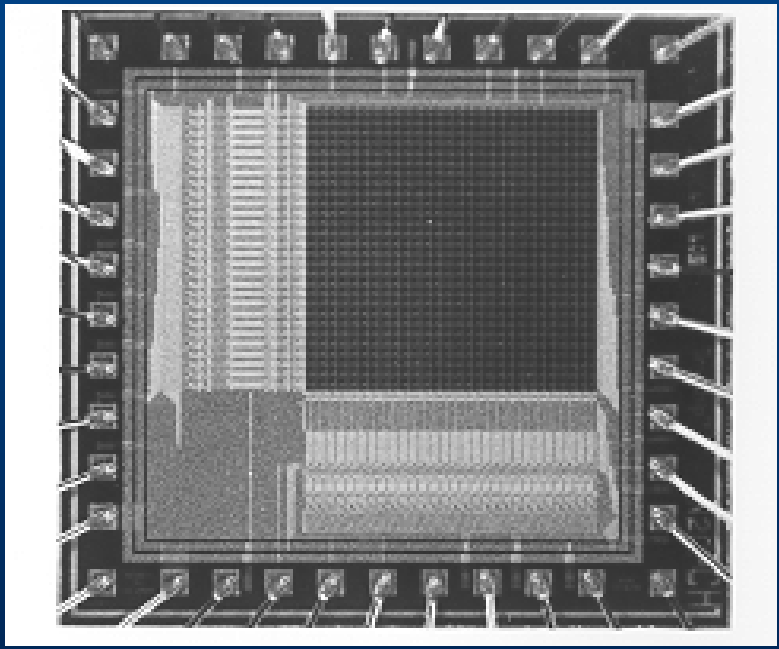
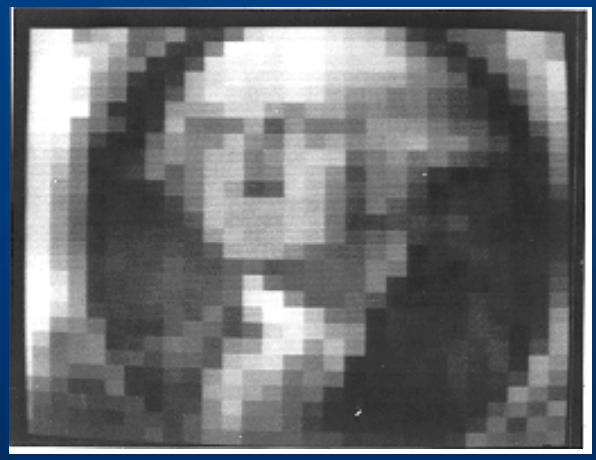
INITIAL CMOS APS DEVELOPMENT AT JPL

FIRST CMOS APS CHIP 4/93

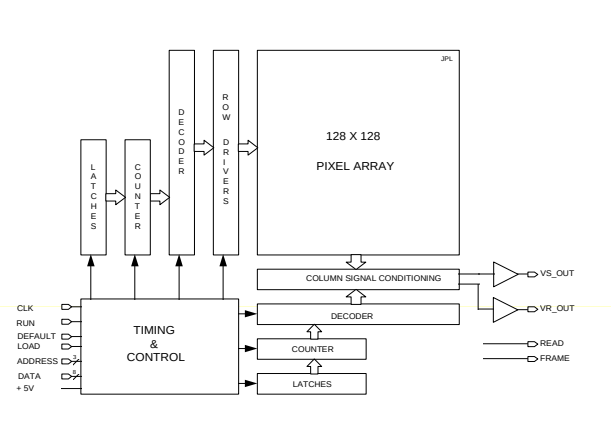


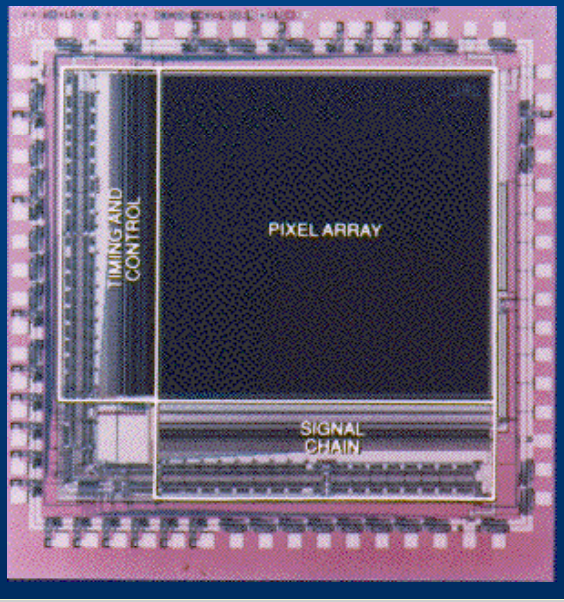


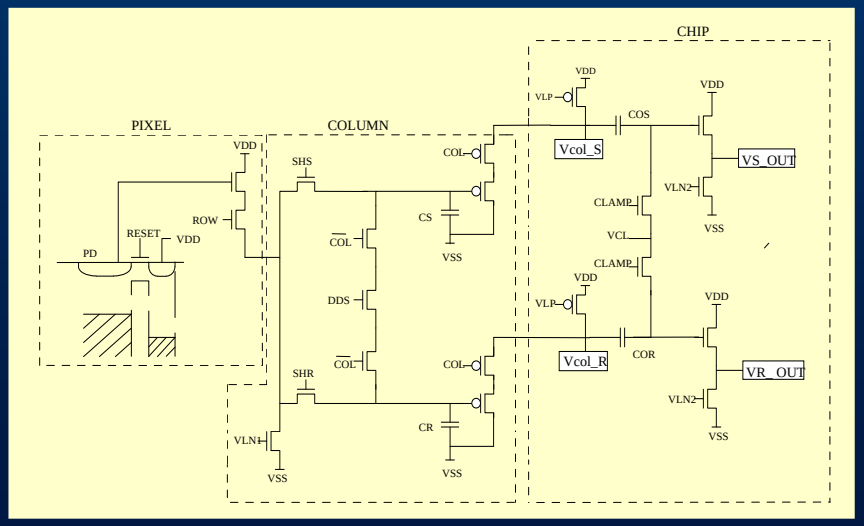
- 28 x 28 element array
- 2 μm CMOS
- 40 μm x 40 μm pixels
- No on-chip timing or control

JPL: Mendis & Fossum

CC128 - ANALOG OUTPUT

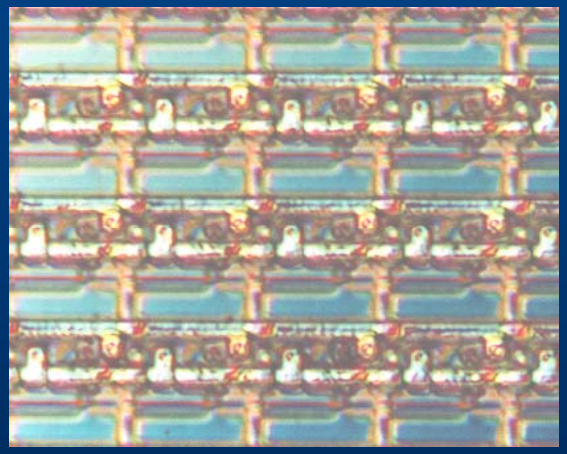


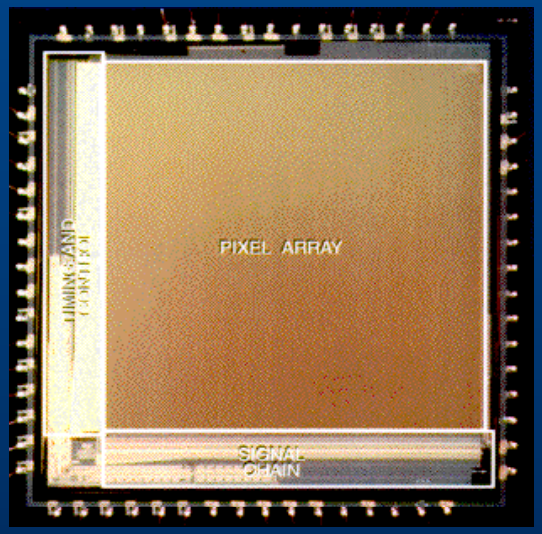




Parameter	5 Volt Operation		3 Volt Operation	
Saturation level	1300 mV	370,000 e	500 mV	142,000 e-
Conversion gain	3.5 μV/e-		3.5 μV/e-	
Read Noise	<< 300 μV	<< 86 e-		
Power			13.8 mW	
Peak QE	~ 60 %			
Fixed Pattern Noise	< 2mV p-p	<0.15 % sat		
Dark Current	15 mV/sec	<200 pA/cm^2	5 mV/sec	< 66 pA/cm^2

CC256 - ANALOG OUTPUT





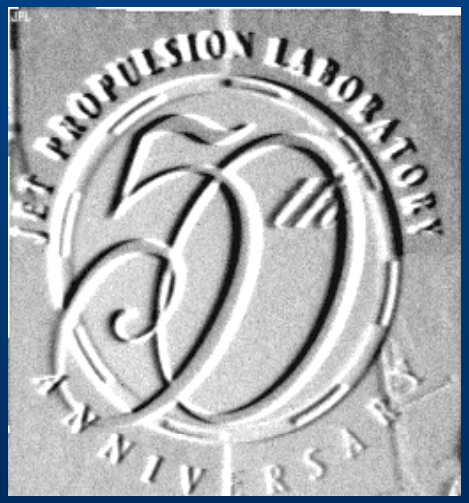
Pixel size:	20.4 μm
Pixel type:	photogate
Fill factor:	21%
Technology:	HP 1.2 μm n-well

Array size: 256x256
Timing, control, CDS
FPN suppression
Motion detection
Window readout
Program. integration time

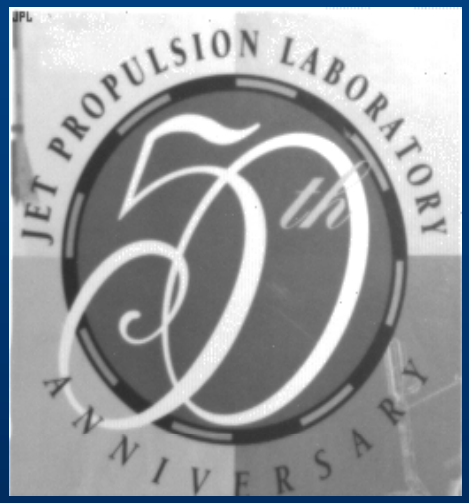
Conv. Gain:	10.6 μV/e-
Saturation:	800 mV
Noise:	13 e- rms
FPN:	0.15% sat
Dyn. range:	76 dB
Power:	3 mW

Nixon, Kemeny and Fossum 1995

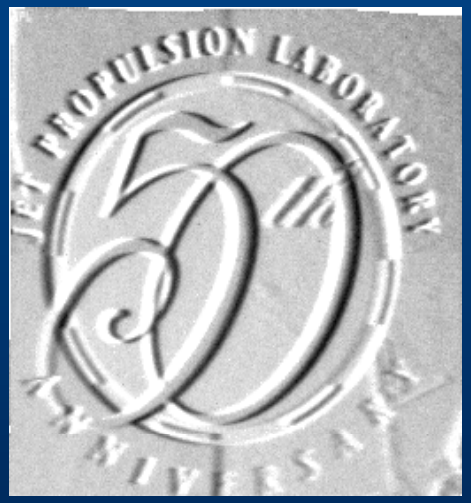
MOTION DETECTION



Motion to left



Normal image

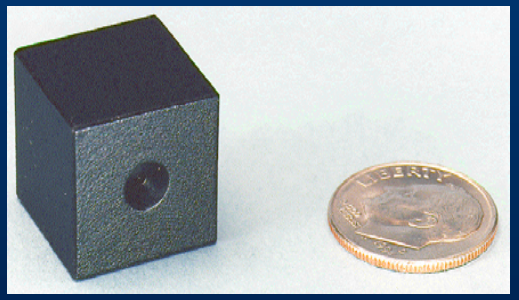


Motion to right

- Use floating diffusion as analog frame memory
- No change to pixel design, just timing

MINIATURIZED CMOS APS CAMERAS

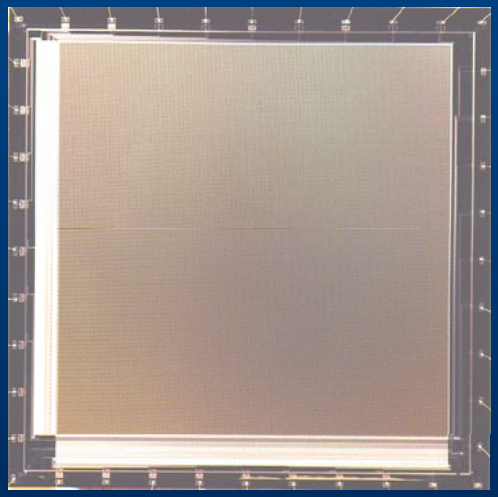
Technology demonstration camera
- 256x256 CMOS APS Camera
- Full digital interface
- Electronic pan and zoom

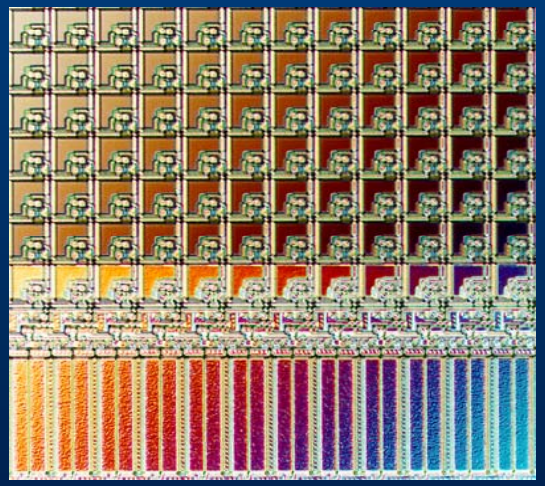


Next demonstration camera
- On-chip ADC
- Automatic exposure control

JPL/KODAK PPD CMOS APS

- Pinned photodiode CMOS APS
- No poly obscuration
- Good blue response
- Lower dark current
- 256 x256 element sensor

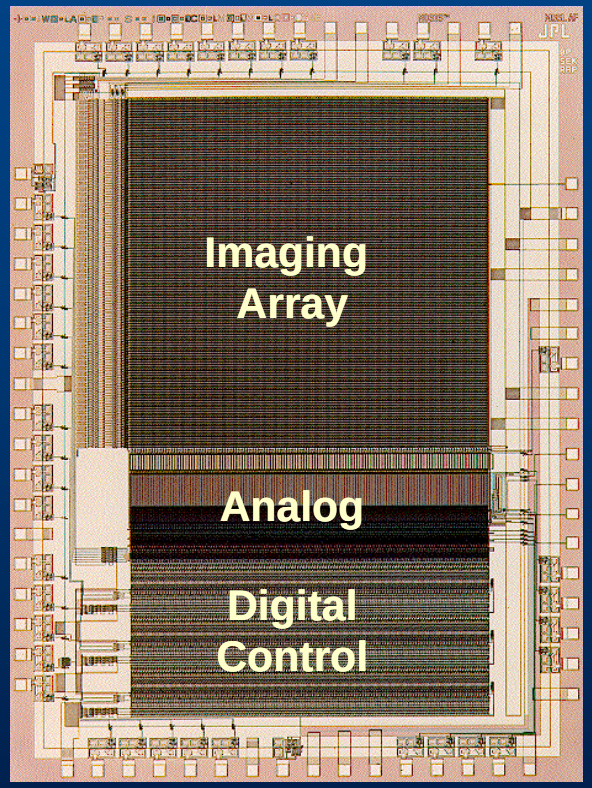




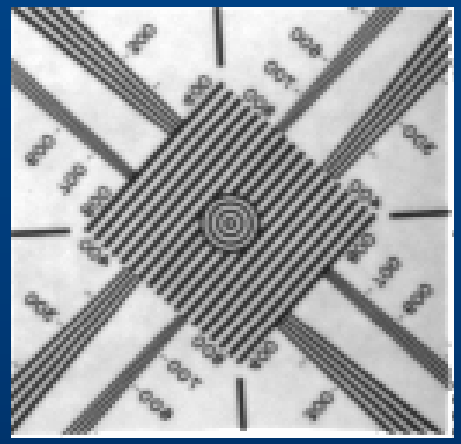
Pinned photodiode (PPD) APS pixels

P. Lee, R. Gee, M. Guidash, T. Lee, and E. Fossum, 1995

JPL MULTIRESOLUTION SENSOR



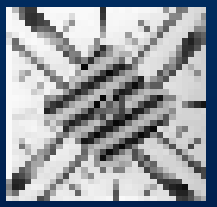
Process:	HP 1.2 um n-well CMOS
Pixel pitch:	24 um
No. pixels:	128 x 128
Pwr suppy:	5 volts
Saturation:	1200 mV
Conv. gain:	8 uV/e-
Noise:	116 uV rms 15 e- rms
Dynamic Range:	80 dB
FPN:	<3 mV p-p <2.5 %
Power:	< 5 mW at 30Hz



Full resolution image

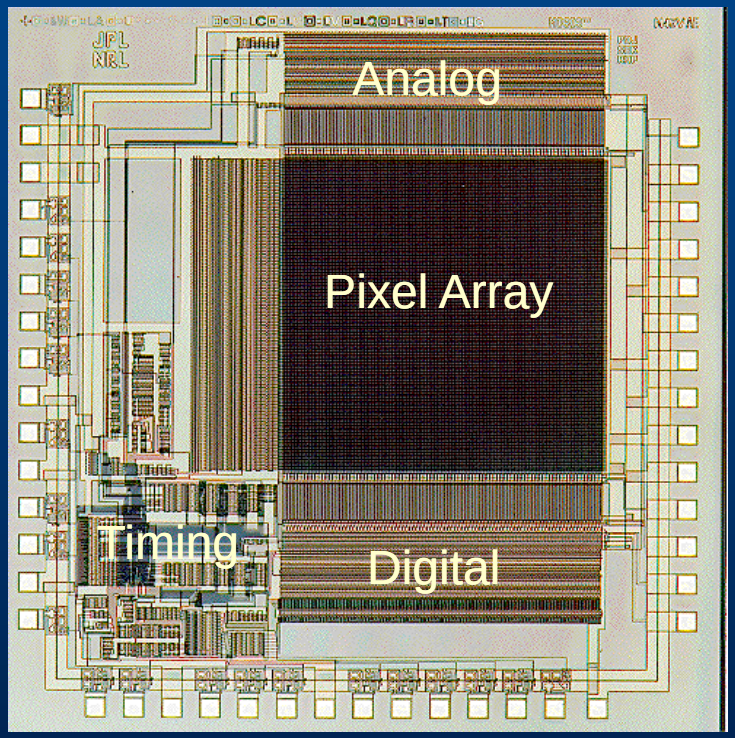
4x4 Averaged image (left)

1/4 Subsampled image (right)



Kemeny, Panicacci, Pain, Matthies, Fossum 1995

JPL HIGH SPEED CMOS APS



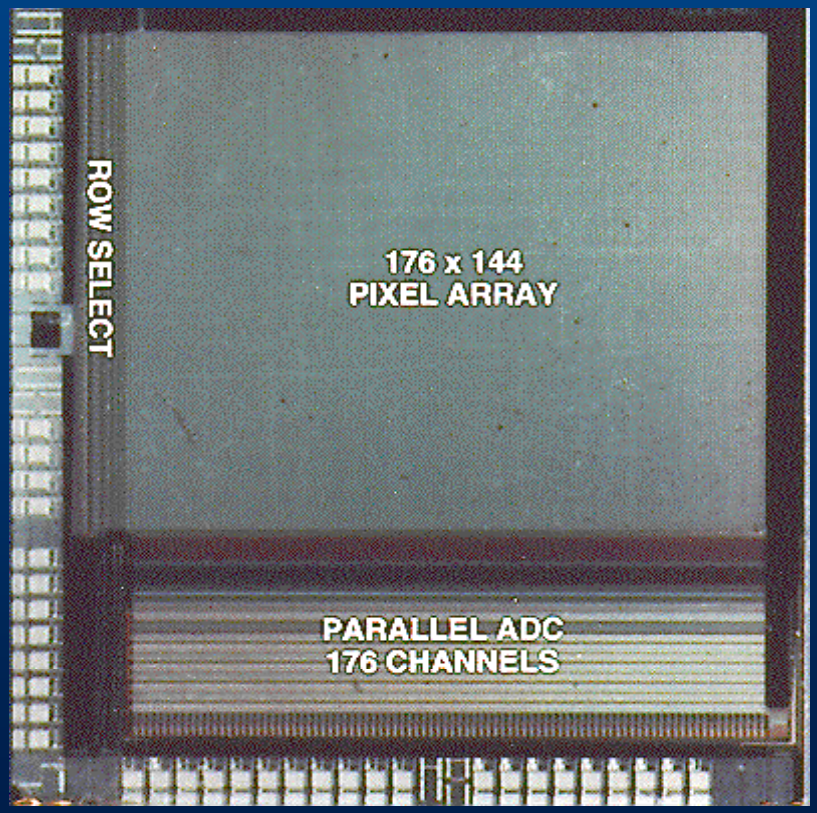
- 128x128 elements
- Photodiode active pixels
- 16 μm pixel pitch
- Analog output (top)
- 1-bit Digital output (bottom)
- 8,000 frames per second
- On-chip timing and control

Analog Output

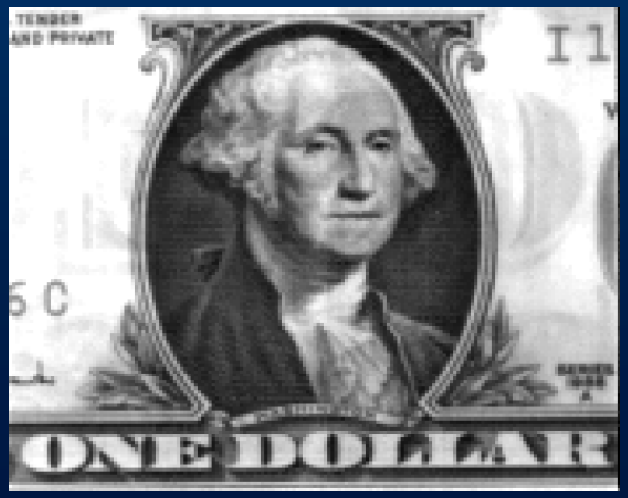
Digital Output

Panicacci, Jones, Fossum 1994

JPL/AT&T DIGITAL CMOS APS



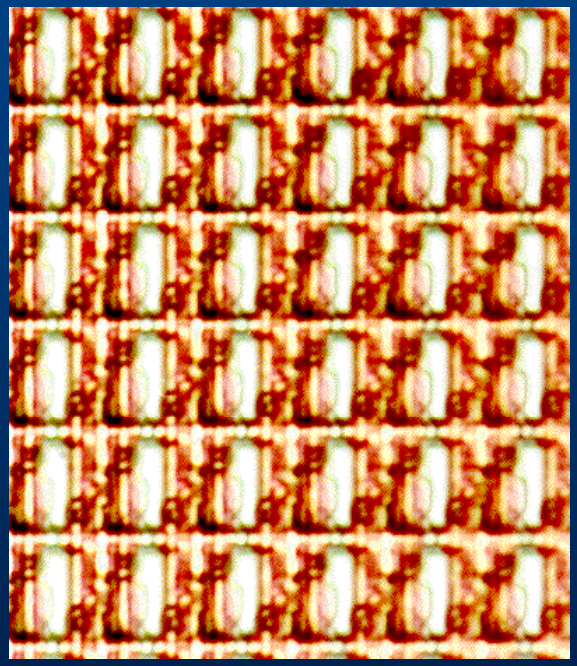
- 176x144 elements
- 20 μm pixel pitch
- Single-slope ADC per column
- 176 ADCs per chip
- 8 bit resolution
- 35 mW at 30 Hz
- 3.5 volt supply



Mendis, Inglis, Dickinson, and Fossum 1995

JPL/AT&T 1024 x 1024 CMOS APS

Chip

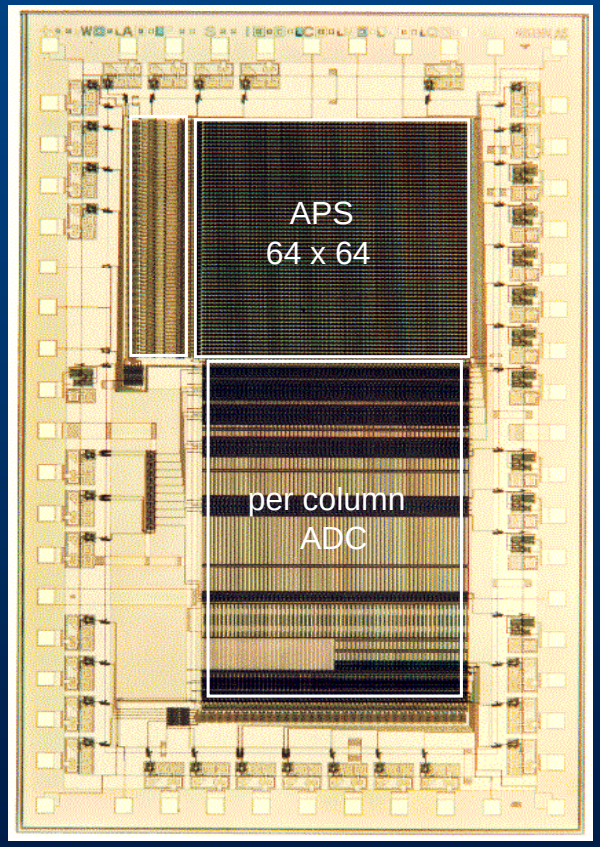


Closeup of pixels

Dickinson, Ackland, Azadet, Inglis, Mendis, Jones and Fossum 1995

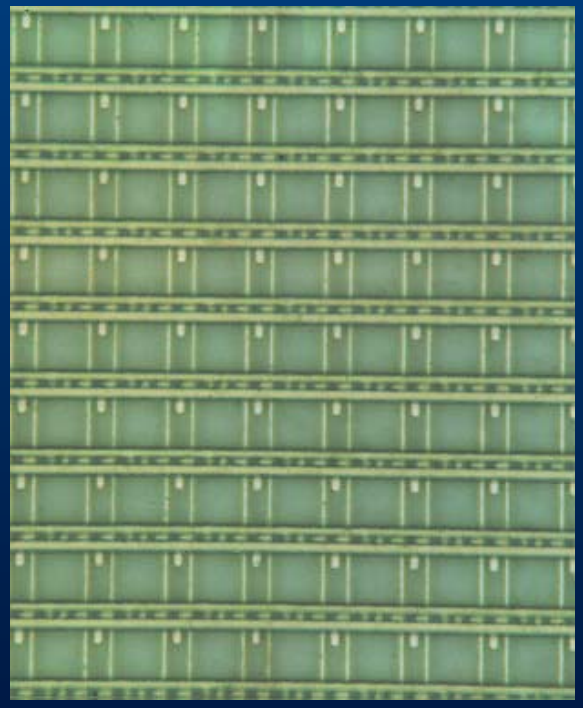
FIRST ON-CHIP SUCCESSIVE APPROXIMATION ADC

- 64x64 CMOS APS
  - 64 successive approximation on-chip ADCs
  - 0.1 μW/kHz/ADC
  - 8-bit resolution

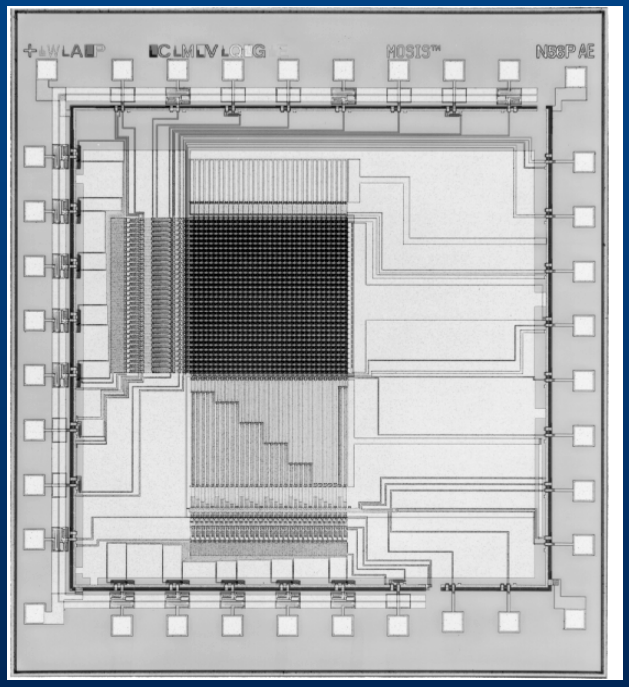


1024 x 1024 CMOS APS WITH 1024 ON-CHIP ADCS

- 1024x1024 CMOS APS
  - 1024 Single-slope on-chip ADCs
  - 24 μW/kHz/ADC
  - 8-bit resolution

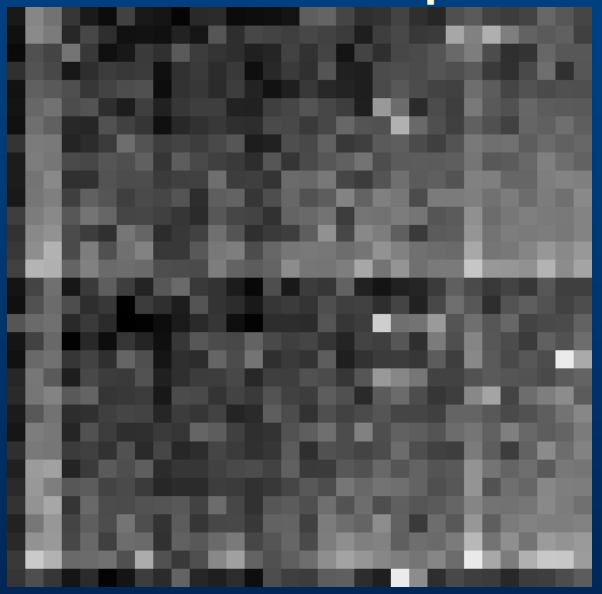


NOISE TEST CHIP



- Matrix of varying pixel and signal chain designs
- 32 x 32 elements PG APS
- 1.2 um n-well (HP)

Noise Map



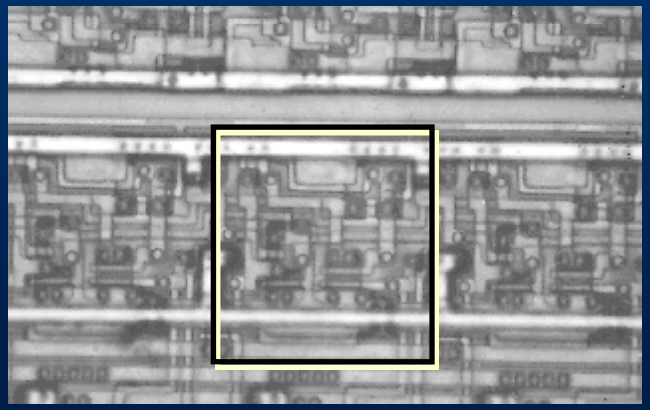
- Darker areas denote lower noise
- Noise is 7-20 e- rms
- Conversion gain is 4-10 uV/e-

Mansoorian and Fossum, 1995

PHOTOELECTRON COUNTING MUX

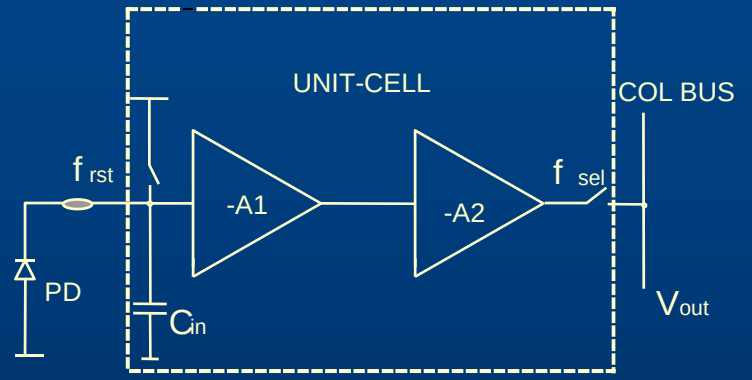
Single-Stage Design

- Cell size: 28x28 μm
- Technology: HP 1.2 μm
- Gain: 35 dB
- Variation: 3.2%
- Power: 35 μW/cell
- Max cnt rate: 300,000/sec
- Noise: 3 e- rms

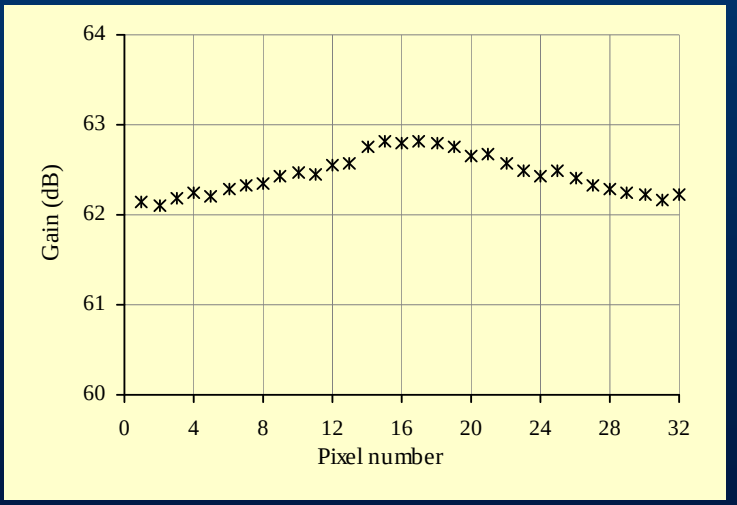


Single-stage unit cell microphotograph

Pain, Fossum 1996

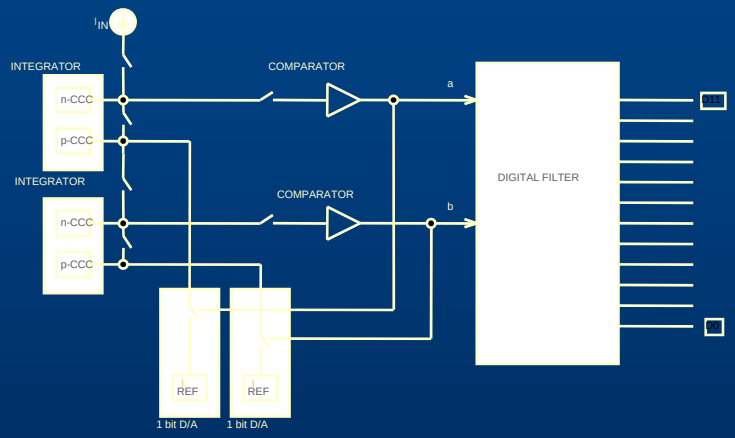


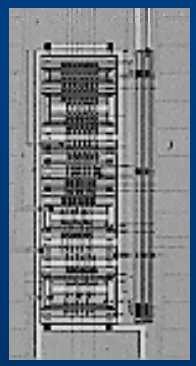
2-Stage circuit block diagram



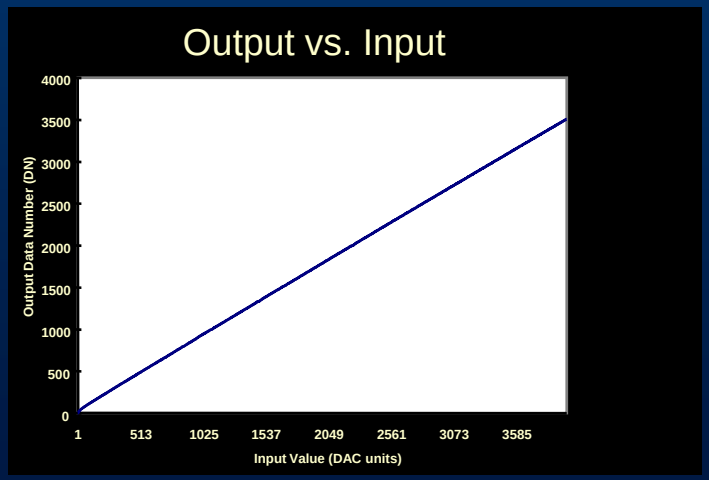
Excellent 2-stage gain uniformity

12 BIT Σ–Δ CURRENT MODE ADC





- 12 bit oversampled 2nd order ADC
- Current mode implementation
- 2 μm Olympus CMOS process
- 3 modulators in test chip
- ADC is 80 μm x 1.9 mm



Performance

- 5-10 kS/sec per channel
- <800 μW/channel
- 1 ADC per 8 columns
- INL < 30 LSBs
- DNL < 4 LSBs

Nakamura, Pain, Nomoto, and Fossum 11/95

JPL CMOS APS TEAM

Back Row: Panicacci, Mansoorian, Staller, Gee, Jones, Koulter
Front Row: Nixon, Kim, Fossum, Pain, Zhou, Yadid-Pecht