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## CMOS Image Sensors

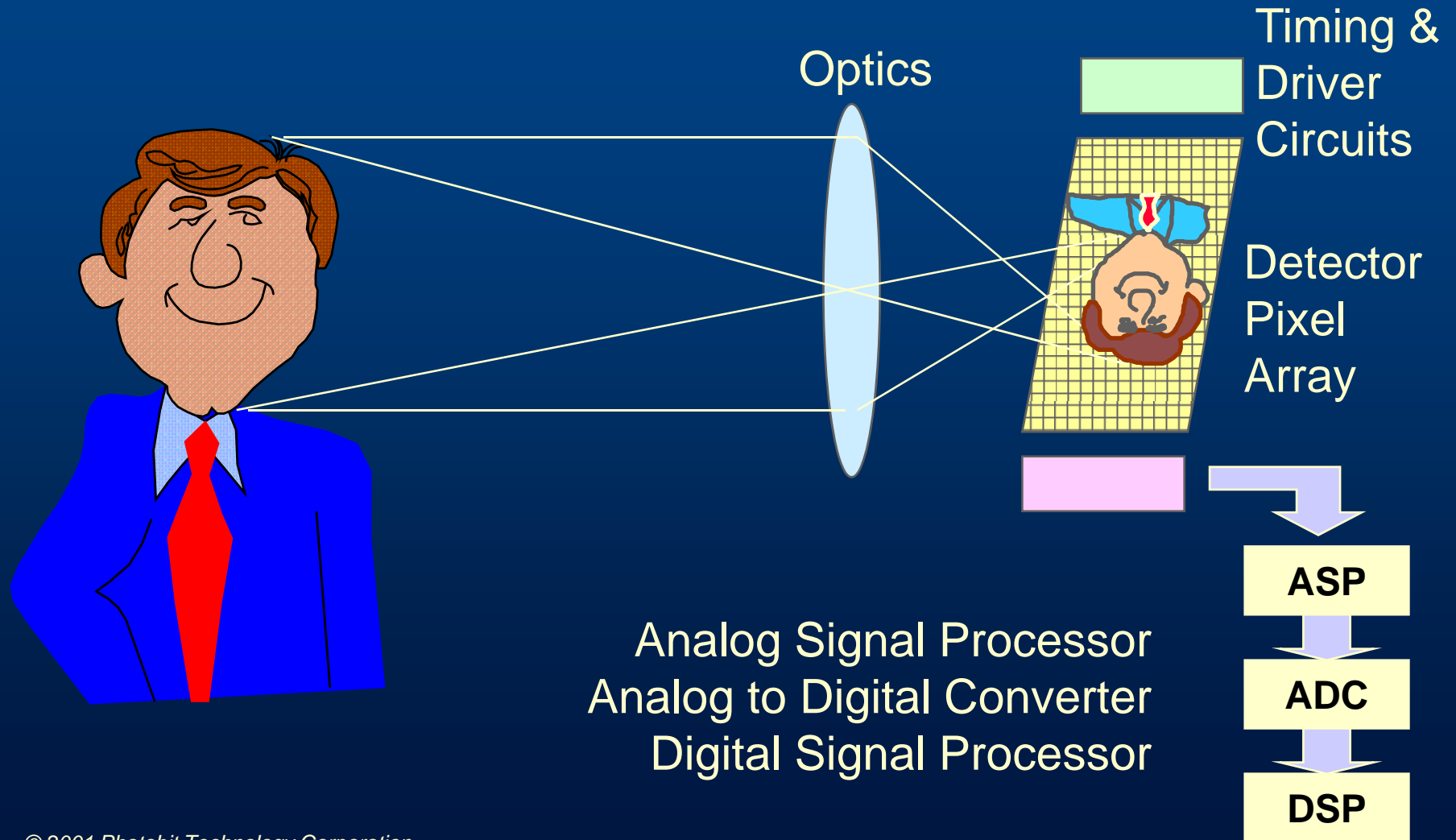
Dr. Eric R. Fossum  
Photobit Technology Corporation  
Pasadena, California

[fossum@photobit.com](mailto:fossum@photobit.com)



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## Imaging Systems





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## CMOS Image Sensor Camera-on-a-Chip

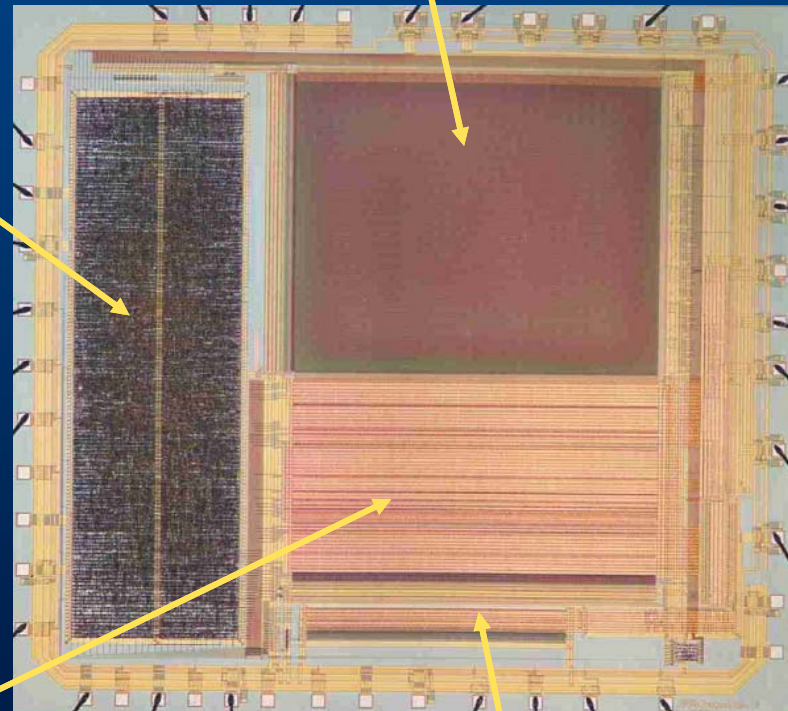
### Digital Logic for

- User Interface
- Sensor Setup
- Timing Generator
- Digital Signal Processing
  - Color Processing
  - White Balance
  - Image Enhancement
- Data Output Formatting

### Analog Signal Processing

- Data Sampling
- Noise Reduction
- Gain

### CMOS Active Pixel Color Imaging Array



### Analog-To-Digital Conversion



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## CMOS Image Sensor Functional Advantages over CCDs

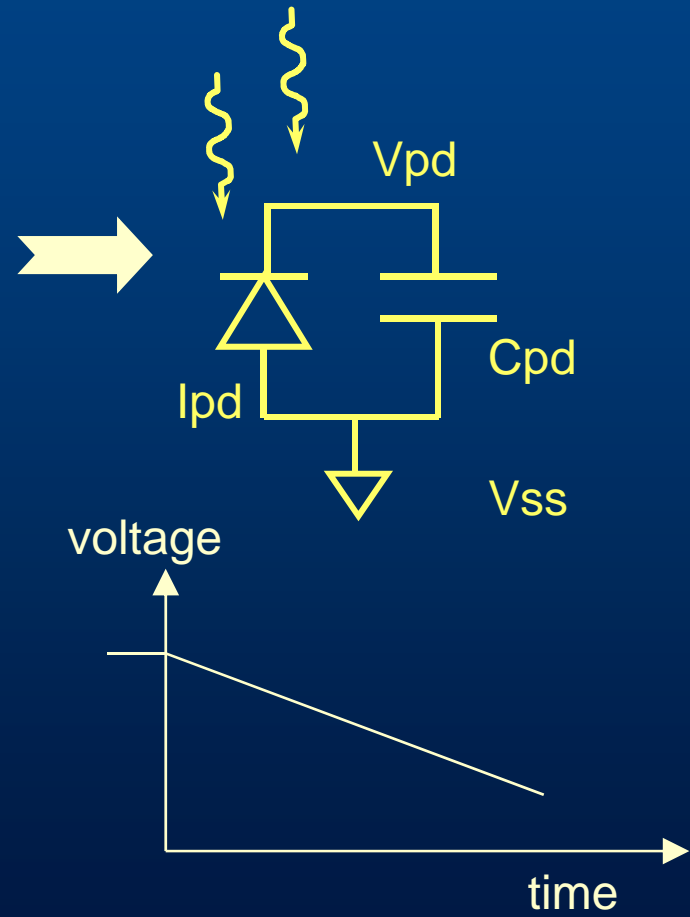
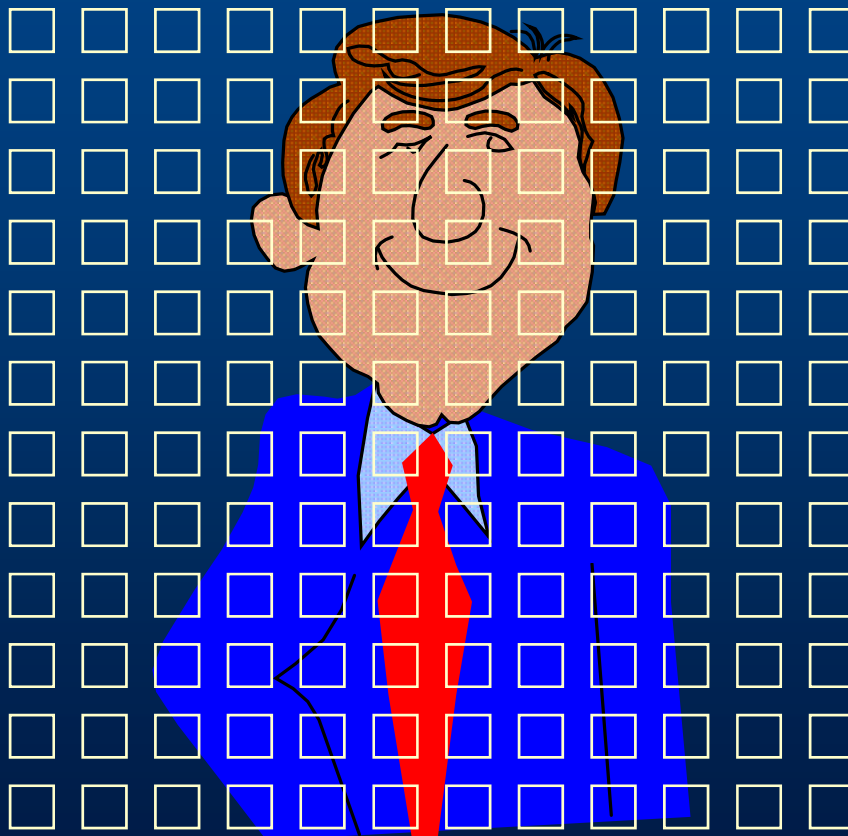
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- On-chip timing and control circuits
- On-chip analog signal processing
  - Correlated double sampling
  - Local neighborhood image processing
  - Multiresolution processing
  - Compression preprocessing
  - Pixel defect correction
- Ultra high dynamic range
- Window readout for electronic pan/tilt
- Skip-mode for low resolution readout
- On-chip analog-to-digital conversion
- High speed digital output
- On-chip DSP and digital sensor control
- Lower supply voltages and power (5V, 3.3V, 2.7V...)
- Easier interface, easier board design



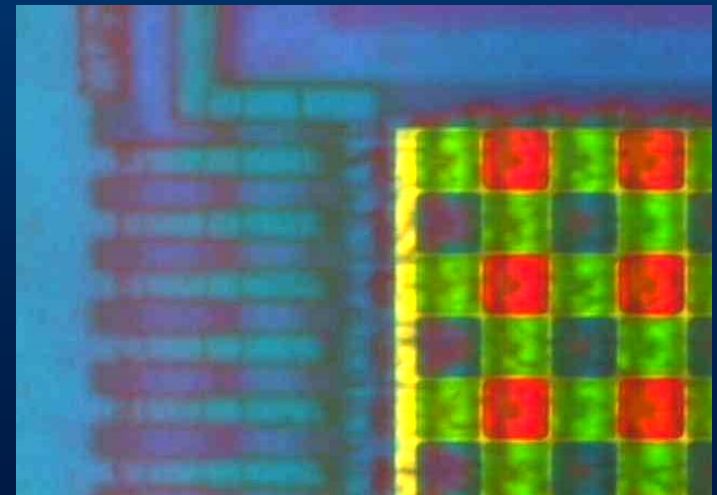
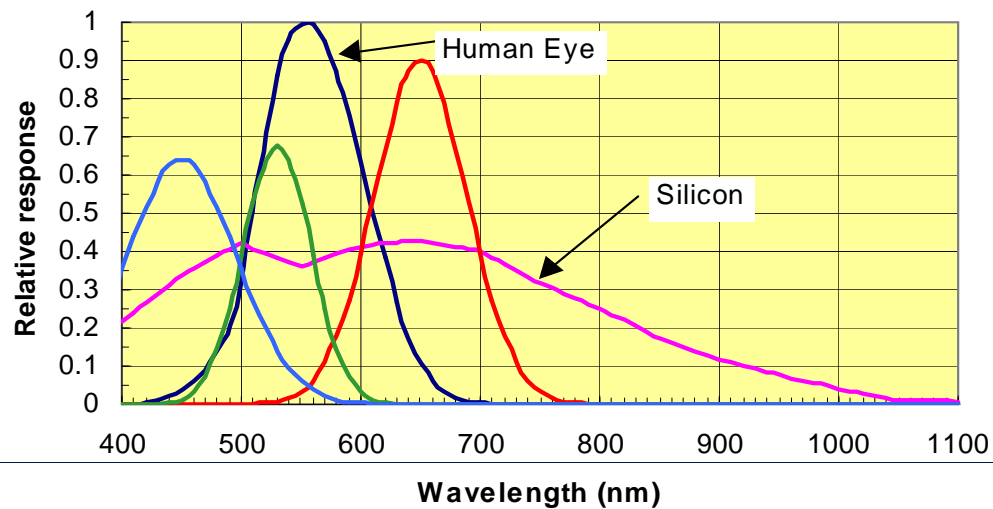
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## Pixels



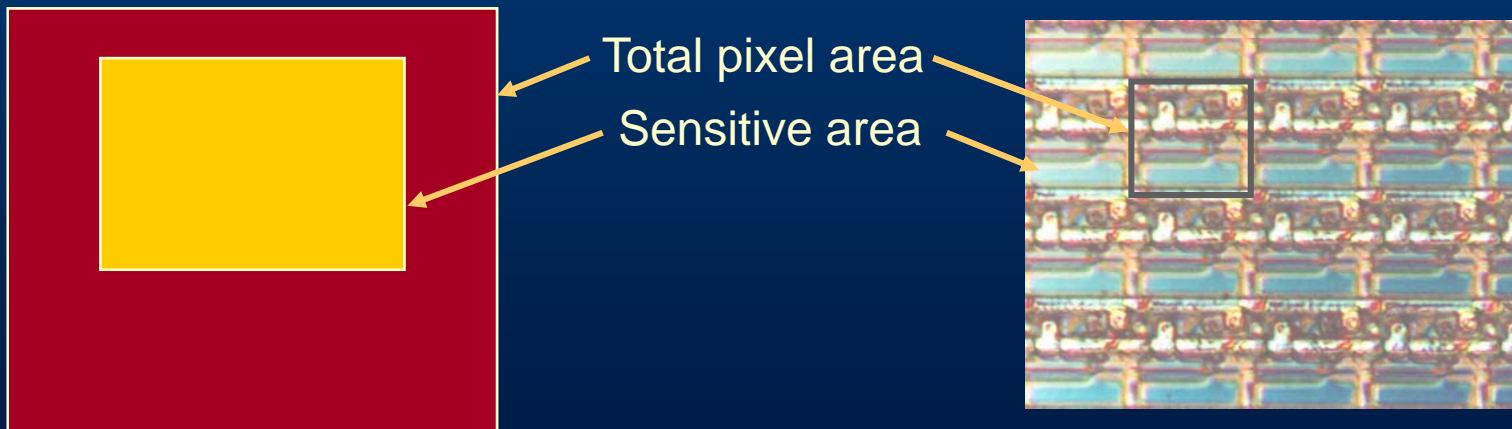


- Each pixel gets covered by a colored filter
  - We use red, green, blue (RGB) CFA - best match for RGB displays in “Bayer” pattern
  - Could use complementary colors (cyan, yellow, magenta)



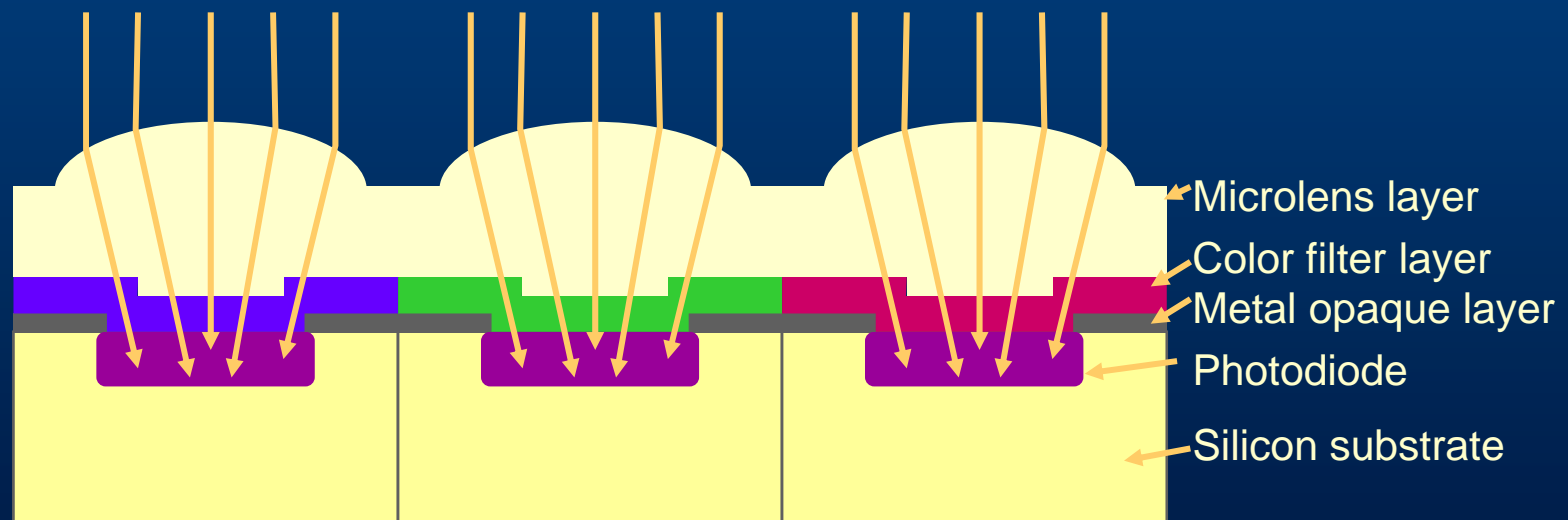


- A pixel is divided into a sensing portion and a readout portion
- Fill factor is the ratio of sensing area to total area and is typically about 20% for CCDs and CMOS APS



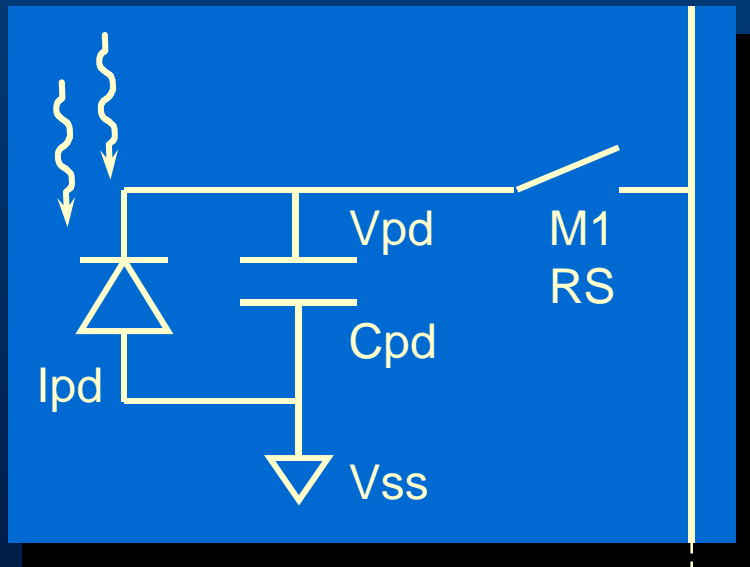


- Microlenses funnel light away from non-sensitive portions of pixel





- Key to Integrated Imaging System (camera on a chip) is making a good pixel in a CMOS platform process.
- Prior to CMOS active pixel was CMOS passive pixel.



- Simple and DRAM-like
- Not such a good pixel due to high read noise
- Gets worse with small pixels, large arrays and faster readout



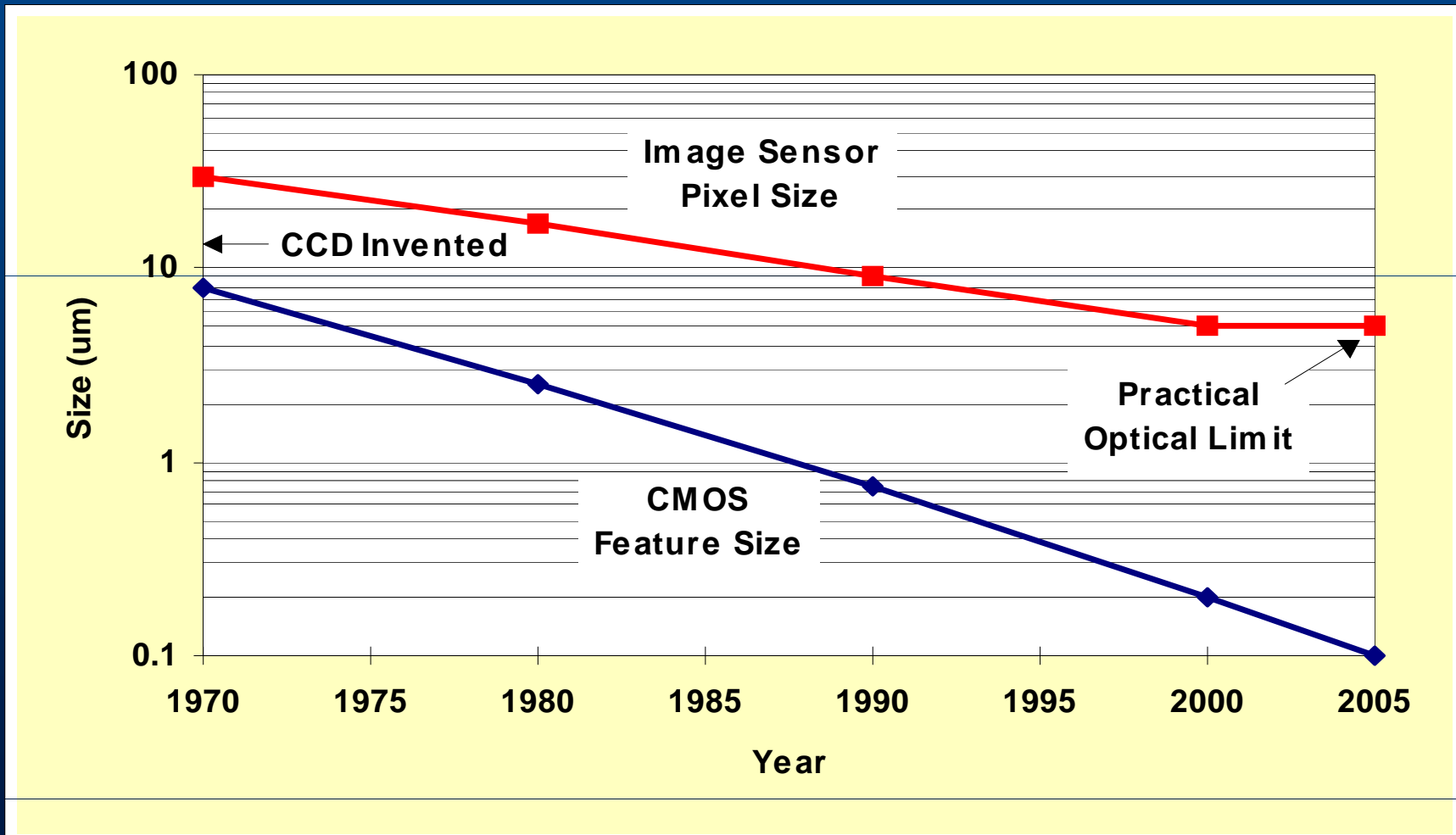
- Add an amplifier inside each pixel.
- Not so obvious:
  - Reduces fill factor due to 3 transistors
  - Adds fixed pattern noise due to offset variations in each amplifier
  - Was tried and discarded in the late 1960's and then CCDs were invented.
- Non-CMOS active pixel sensors were demonstrated by Olympus, Toshiba, Texas Instruments and others but suffer from requiring a unique semiconductor fabrication process

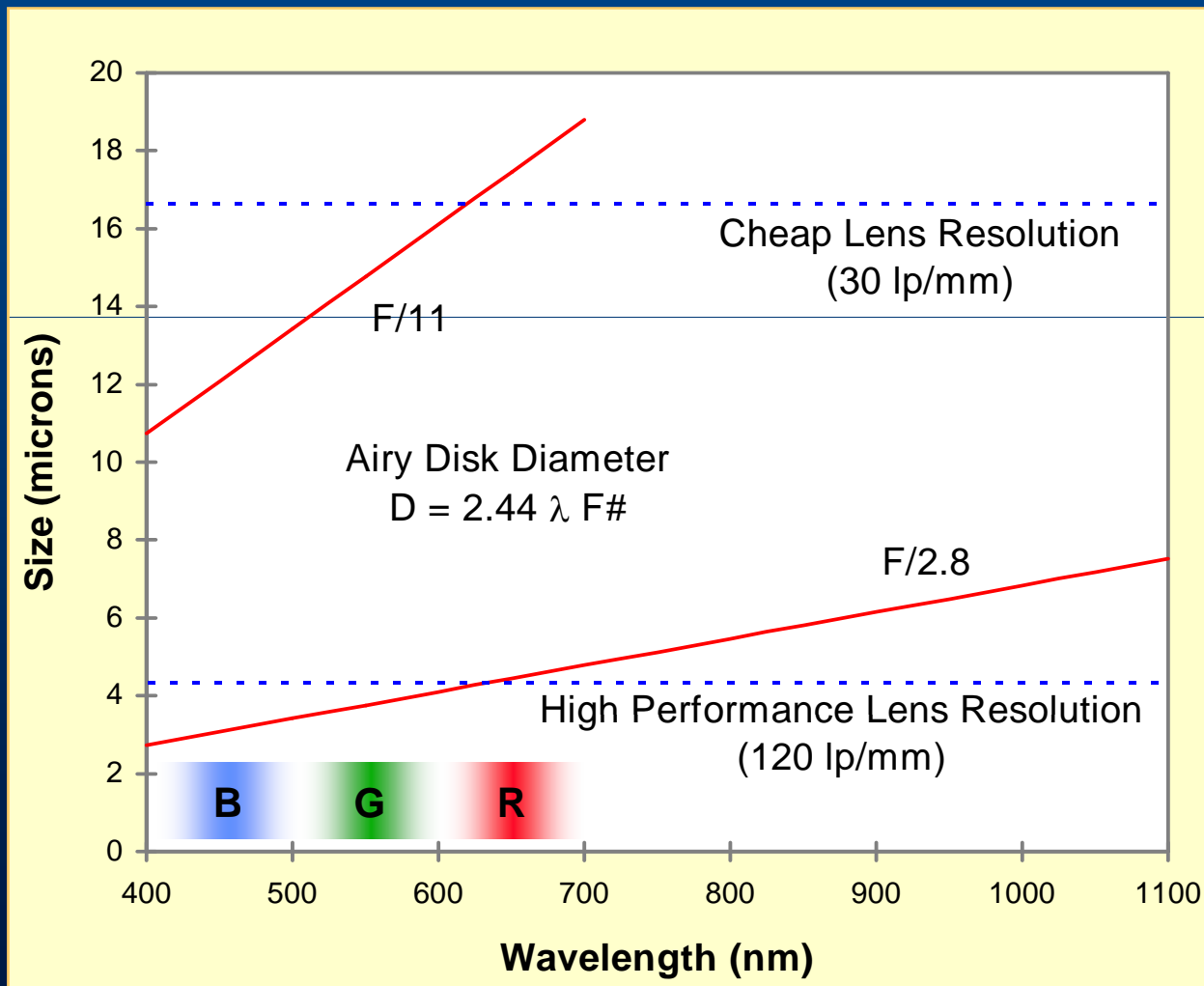


- CMOS state of the art is ripe for image sensors
  - Design rules permit competitive pixel sizes
  - Defects and contamination well controlled
  - Threshold voltages stable and fairly uniform
  - And now foundries offer specialized image sensor modules
- Customers demand low power, miniaturized systems-on-a-chip
- Circuit techniques developed for high performance
  - Active pixel provides gain in pixel and lower noise
  - Use of double-correlated sampling and double-delta sampling on-chip removes temporal & fixed pattern noise
  - Column parallel architecture permits low analog bandwidths to reduce noise and artifacts and maintain high frame rate.
  - Low power imaging circuit techniques reduce power to mW levels



## Evolution of Feature Size

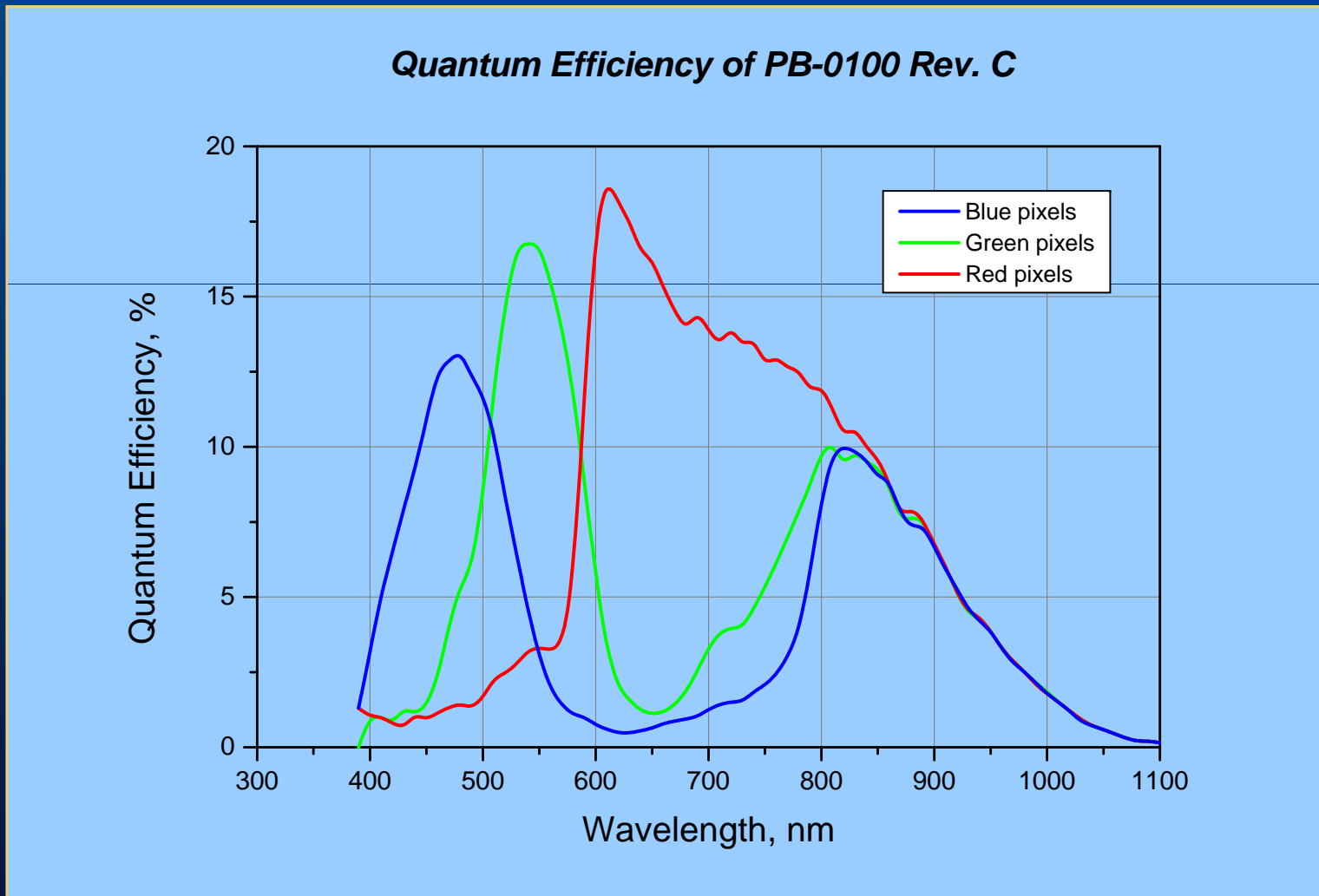






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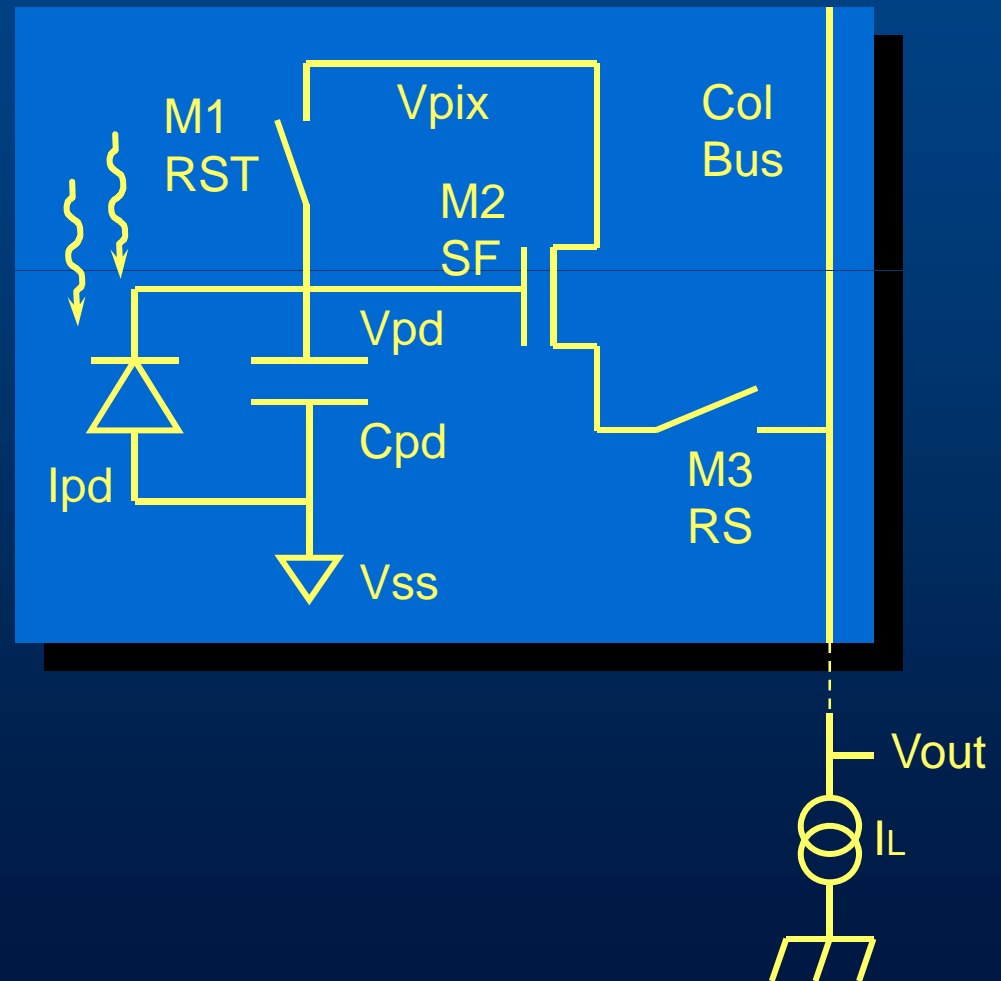
## QUANTUM EFFICIENCY WITH CFA





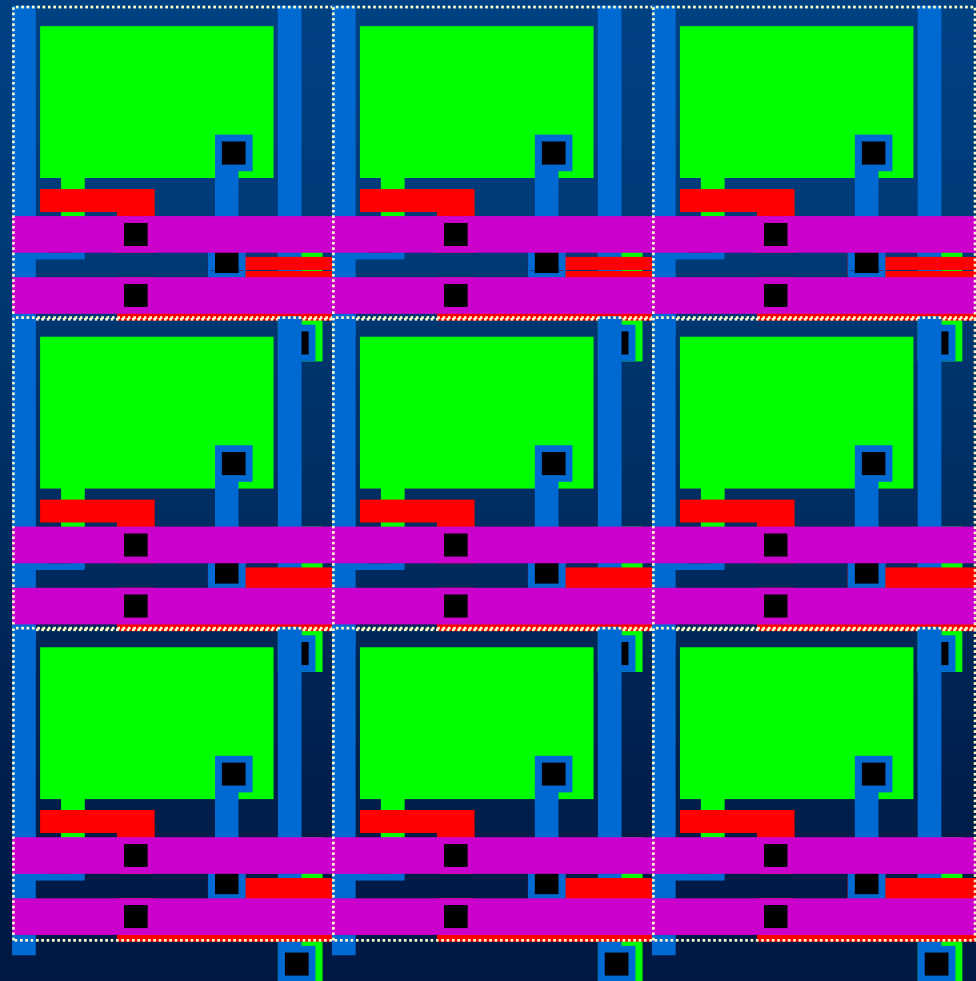
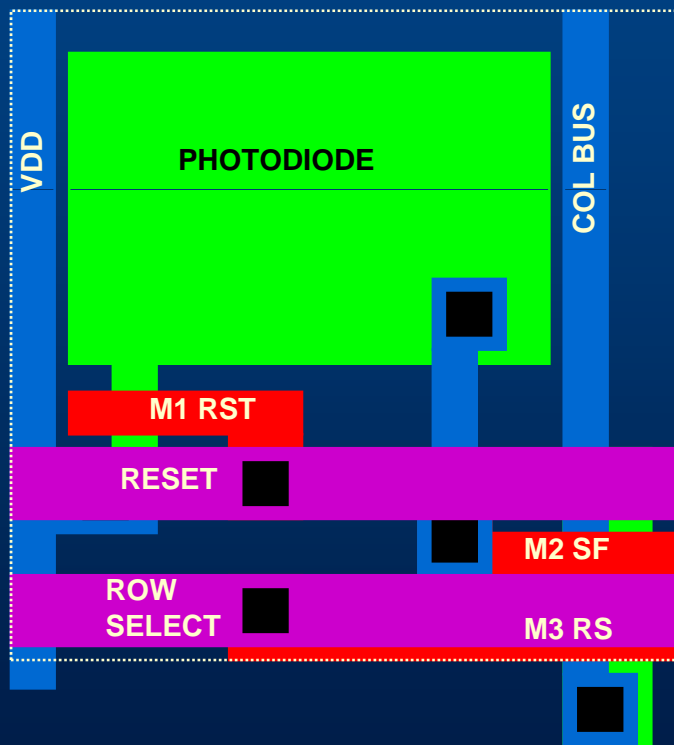
## CMOS Active Pixel

- PN junction photodiode (PD)
- RST switch M1 charges PD to  $V_{pix}$
- Light-generated current  $I_{pd}$  discharges PD
- Voltage  $V_{pd}$  on PD is gate voltage of in-pixel source-follower transistor M1.
- Row Select (RS) switch M3 connects pixel transistor to column bus and charges bus to same voltage as PD.
- Voltage  $V_{out}$  picked off at bottom of column.





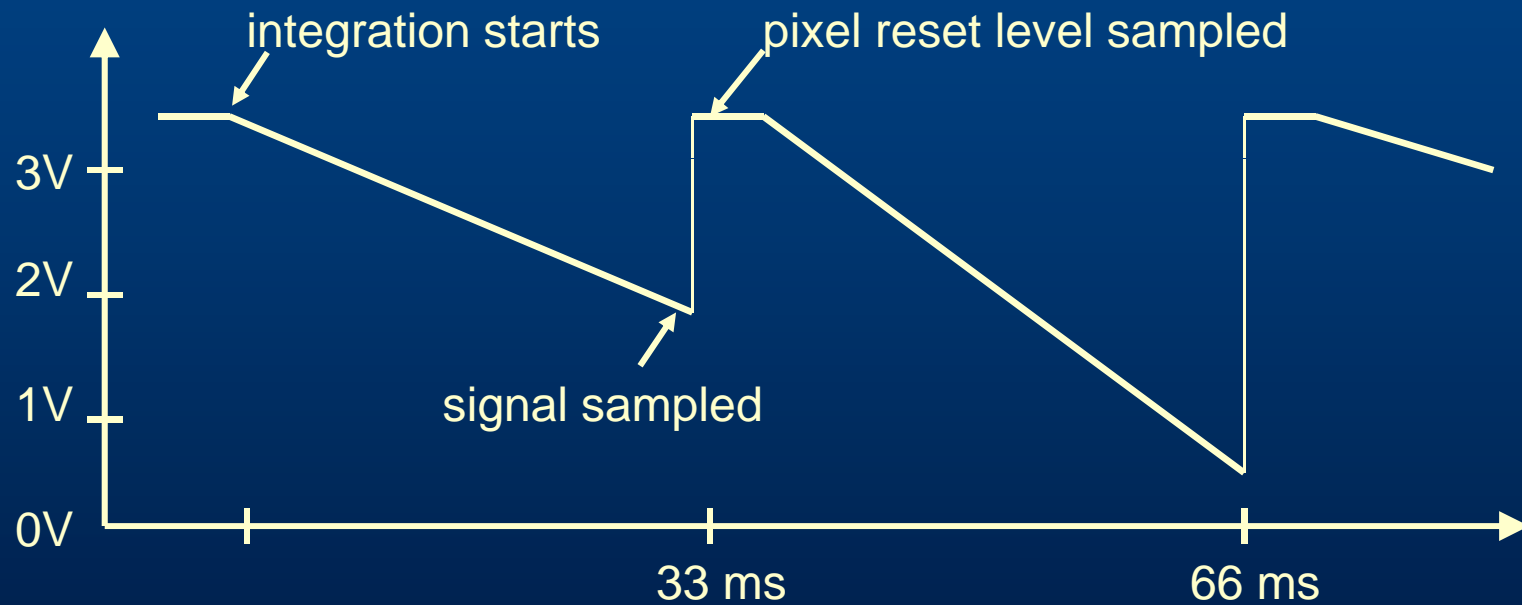
# Physical Layout of a CMOS Active Pixel





## “Correlated” Double Sampling

Photodiode Voltage

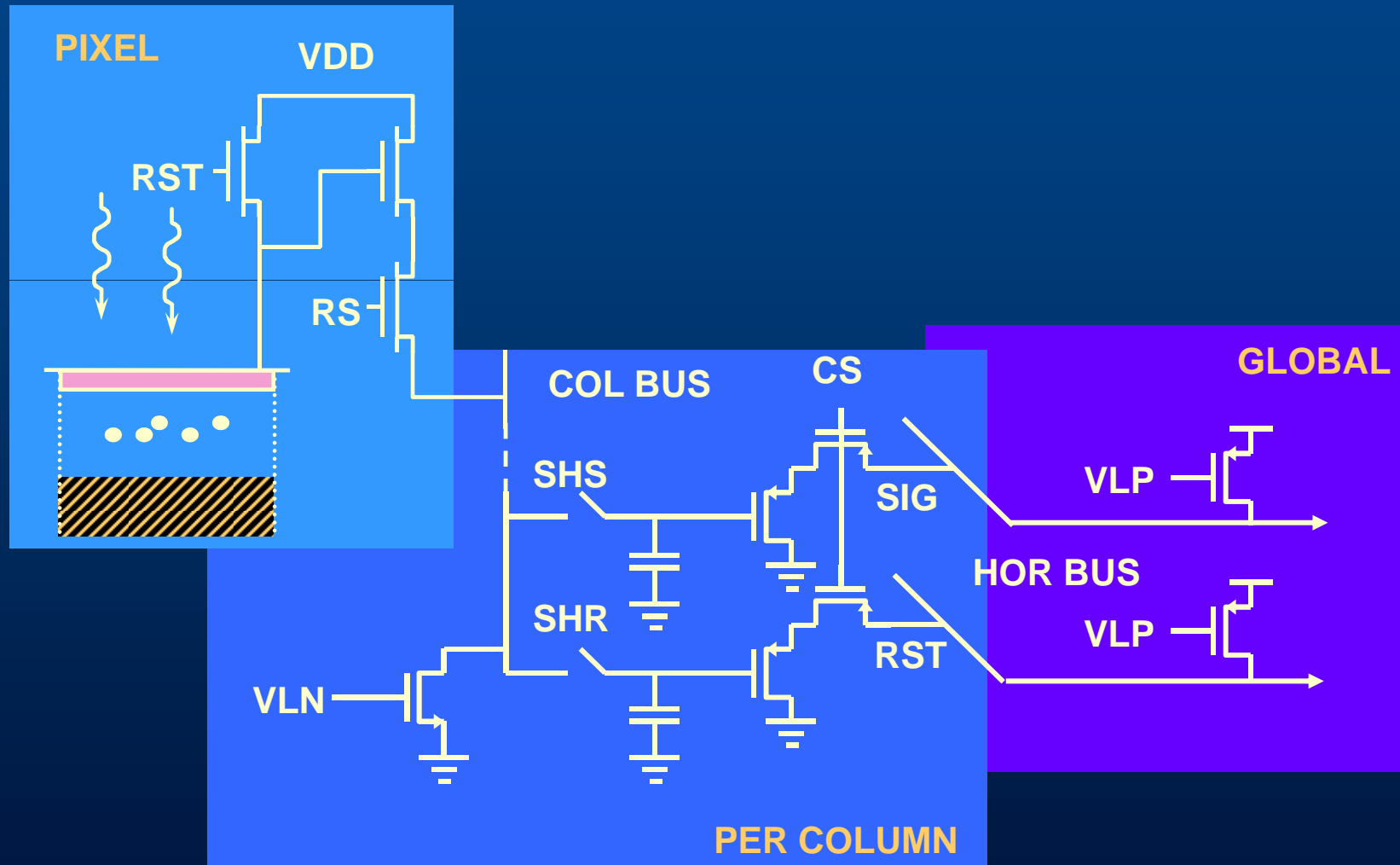


Pixel sampled twice to remove variations in threshold voltage of pixel source follower and reset level.



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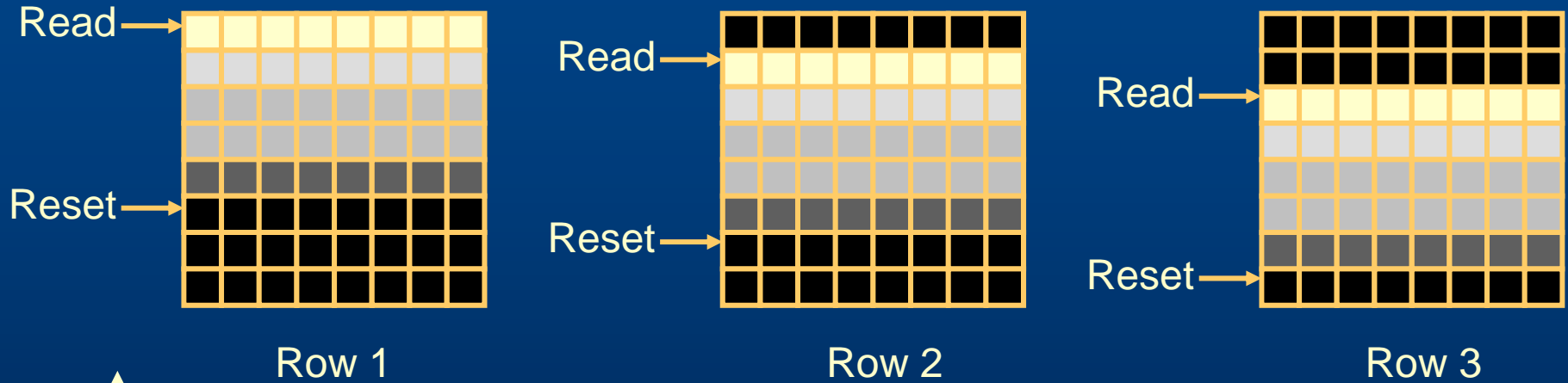
## Simplified Signal Chain





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## Electronic Rolling Shutter

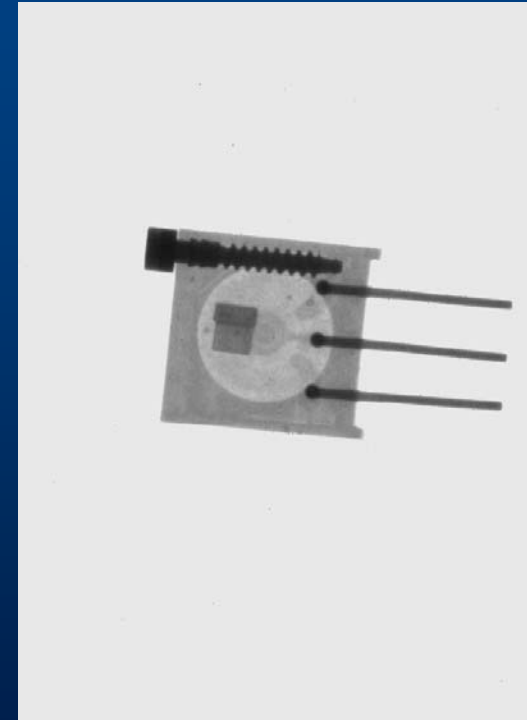
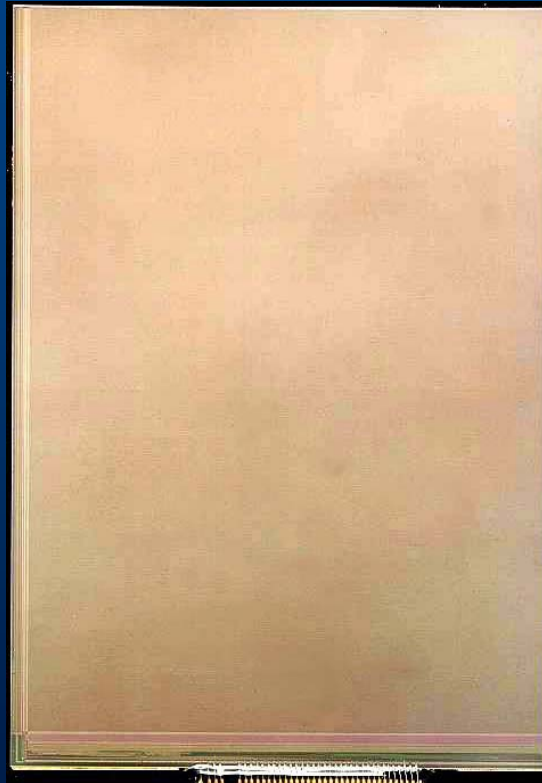




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## X-ray Sensor for Dental and Osteoporosis Applications

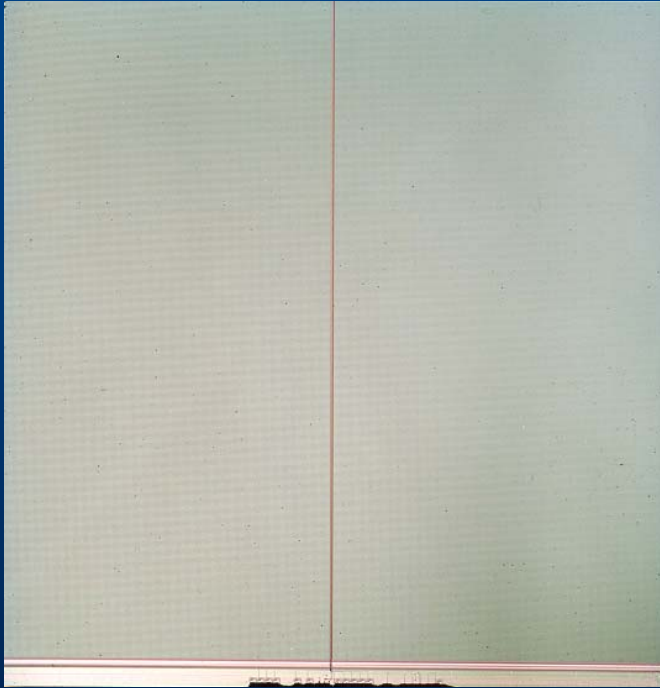
- Total chip size: 37 x 27 mm
- 900 (V) x 675 (H) elements
- 40  $\mu\text{m}$  pixel pitch
- 2  $\mu\text{m}$  CMOS process
- Differential analog output
- On-chip timing and control
- Perhaps world's largest CMOS chip in production





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## Mammography Sensor (3-Sides Buttable)



- 466 x 466 elements
- 30  $\mu\text{m}$  pixel pitch
- 0.8  $\mu\text{m}$  process
- 2 column loss



- 3-sides buttable
- P-channel PD-type pixel
- Differential analog output
- Some on-chip circuits

Xue 1997

© 2001 Photobit Technology Corporation

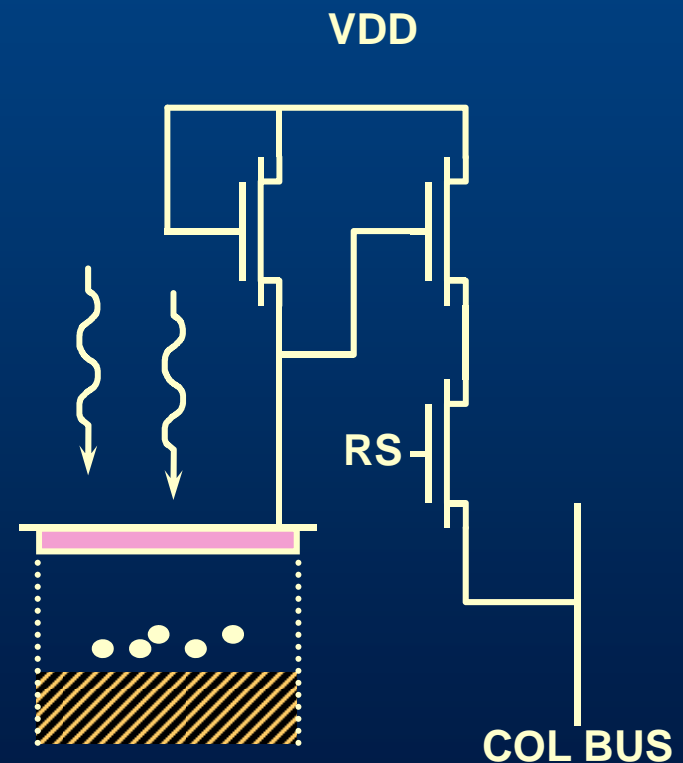


- Passive Pixel Sensor (PPS)
  - Photodiode
  - Charge injection
- Active Pixel Sensor (APS)
  - Photodiode (dates to 1968)
  - Photogate (invented at JPL)
  - Pinned Photodiode (invented by JPL/Kodak)
  - Floating gate (invented at JPL)
  - Logarithmic (high dynamic range - low contrast)
  - Freeze-Frame (Photobit)
  - More complex amplifiers (from DoD infrared imagers)



## Logarithmic Pixel

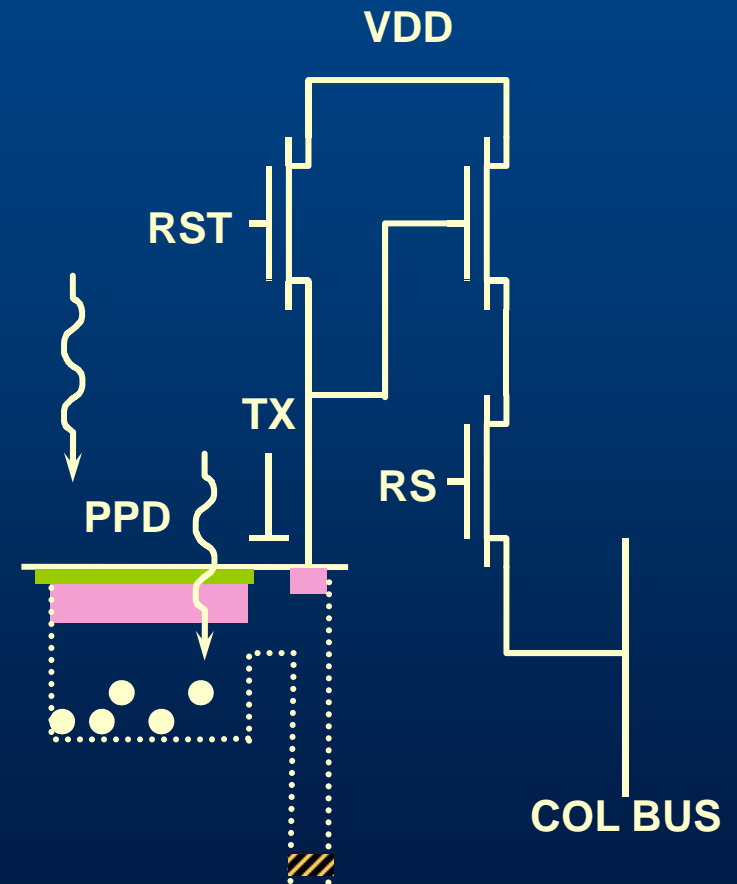
- 3 transistors per pixel
- Slightly larger pixel
- Great QE
- Logarithmic response -- good for large intrascene dynamic range
- Poor contrast under flat lighting
- Log-response makes color processing extremely complex
- Susceptible to FPN
- Slow response under low light





## Pinned Photodiode Active Pixel

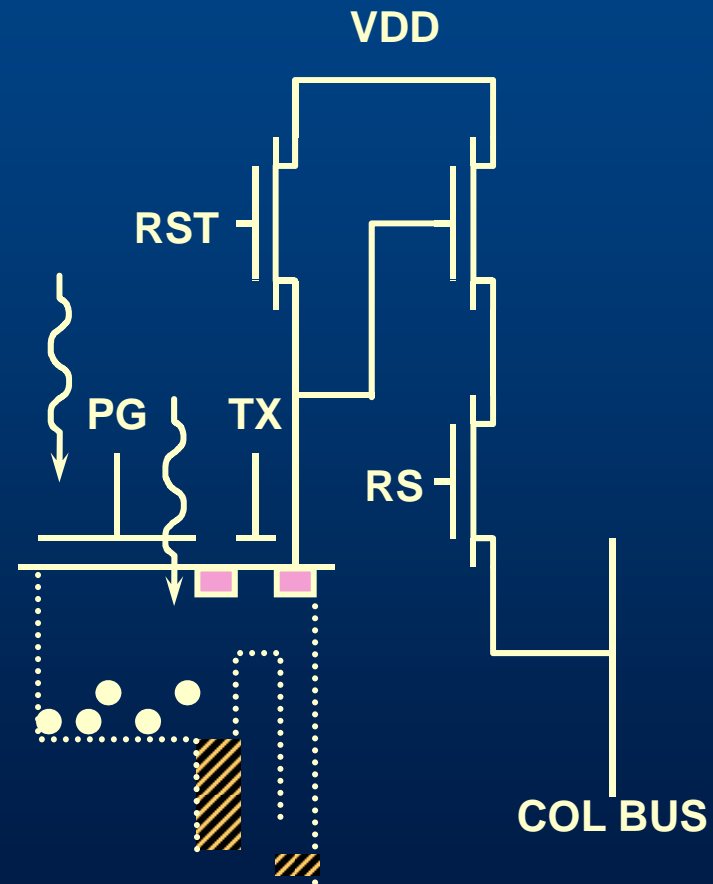
- 4 transistor pixel
- More complex fabrication
- Susceptible to lag
- Great QE
- Low noise
- Good scaling for large arrays
- Good scaling for fast arrays
- First demonstrated by JPL/Kodak





## Photogate Active Pixel

- 5 transistor pixel
- Larger pixel
- QE loss due to poly gate
- Lowest noise
  - 5 e- rms
- Good scaling for large arrays
- Good scaling for fast arrays
- US patent no. 5,471,515 (Pb)



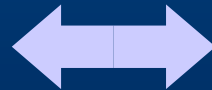


- Permits full digital interface
- Permits on-chip DSP for camera control, color interpolation, etc.
- Suppresses noise pick up from EMI, crosstalk
- Simplifies interface
- Permits faster readout
- Can reduce overall chip and/or system power



## On-Chip ADC Choices

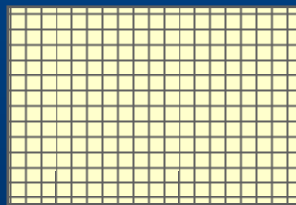
- One (or two or three) ADCs per chip
  - High data rate requirement (5-60 Mconv/s)
  - Local high power dissipation
- One ADC per pixel
  - Large pixels and low fill factor
- One ADC per column (column-parallel)
  - Tall, skinny ADCs



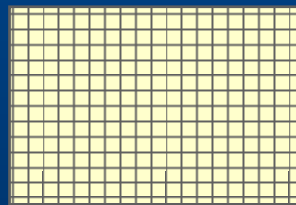
- Single-slope
  - slow
- Successive approximation
  - 8-10 b max
- Algorithmic
  - needs good op-amp
- Oversampled
  - Filter takes lots of area
- Flash and Folding
  - More power



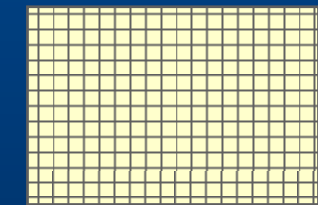
## On-Chip ADC Architectures



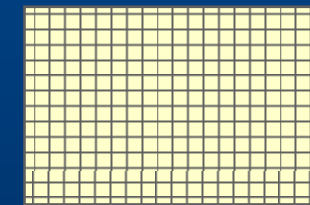
Digitized  
in pixel



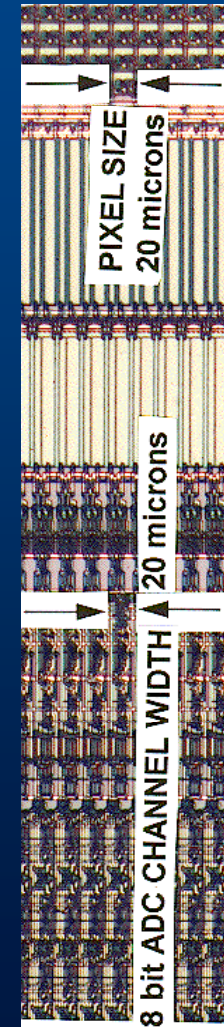
Serial ADC(s)  
at data rate



Column  
parallel  
ADCs  
Multiplexed  
output



Column  
parallel  
ADCs  
Parallel  
output ports

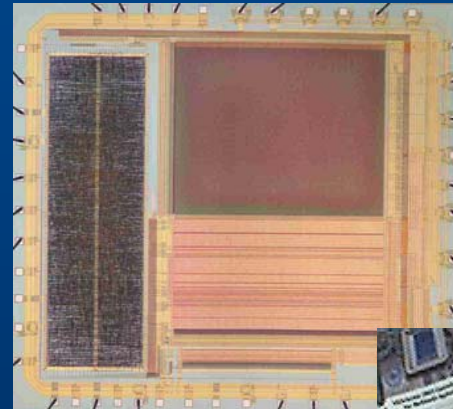




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## Example: CIF-Resolution Sensor

- Internet cameras, games
- 360x304 (352x288 effective) pixels
- 8b flash ADC
- 7.9  $\mu\text{m}$  x 7.9  $\mu\text{m}$  (1/5" optical format)
- Progressive scan, window readout
- 15,000 gate on-chip logic
- >30 frames per sec (adj.)
- 3.3 V operation
- <100 mW total power
- Built-in autoexposure control
- On-chip biasing
- On-chip CFA
- >20 dB SNR @ 1 lux, 30 fps



Van Blerkom, Huang, Chan 1999

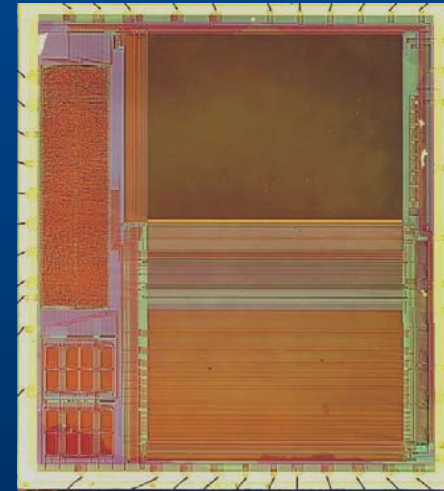
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## Example: VGA-Resolution Sensor

- Dual mode cameras, internet cameras
- 640x487 (640x480 effective) pixels
- 320 column-parallel 8b ADCs
- 7.9  $\mu\text{m}$  x 7.9  $\mu\text{m}$  (1/3" optical format)
- Progressive scan, window readout
- 15,000+ gate on-chip logic
- >30 frames per sec (adj.)
- 5 V operation
- <300 mW total power
- Built-in autoexposure control
- On-chip biasing
- On-chip CFA
- >20 dB SNR @ 1 lux, 30 fps



*Panicacci, Cho 1999*

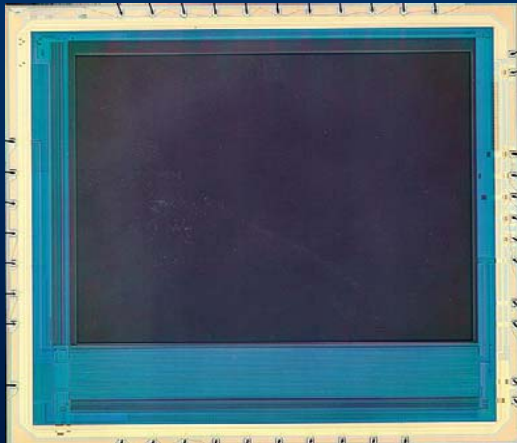
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## Example: 2Mpixel Digital Still Camera

- Digital still cameras
- 2 Mpixels
- 3.9  $\mu\text{m}$  pixel pitch
- Microlenses





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## Major Advantages of CMOS Image Sensors over CCDs

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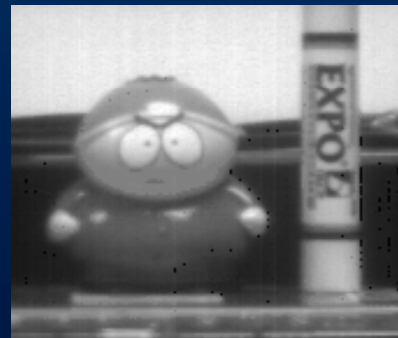
- Lower power
  - Lower supply voltages (5, 3.3, 2.7, ....)
  - Integration reduces parasitics
  - Clever mixed signal design and digital signal processing
- Increased functionality
  - Increased integration on chip and smaller form factor
  - Higher dynamic range, better image quality
  - Smart digital signal processing and local sensor control
- Higher speed imaging
  - High throughput with on-chip ADC and digital output
- Lower system cost
  - Fewer system components, lower wafer costs



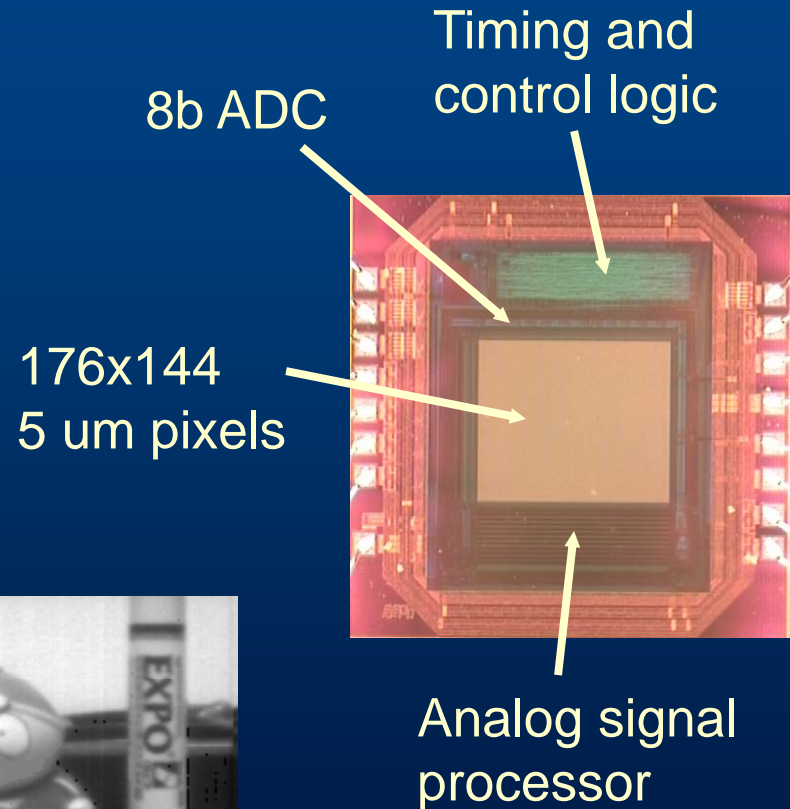
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## 3-Pin Self-Clocked Micropower Camera on a Chip

- World's lowest power camera-on-a-chip
- Portable electronics such as PDAs, cell phones, games
- QCIF format
- 0.35  $\mu\text{m}$  process technology
- 2mm x 2mm die size
- 550  $\mu\text{W}$  total power
- Watch battery operation
- On-chip clock
- On-chip 8b ADC
- 1.5 volt operation
- Serial digital data output



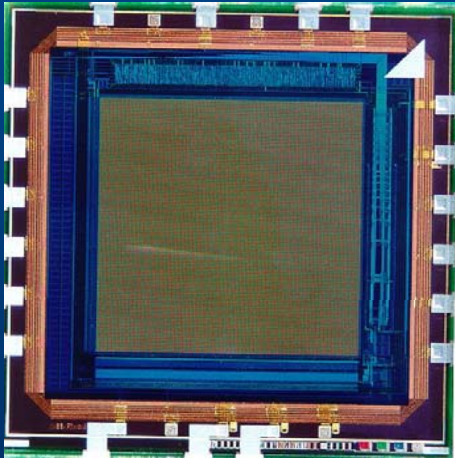
30 fps output



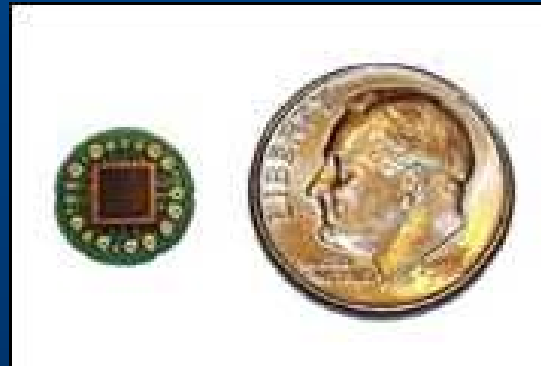


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## Pill Camera



Chip



Sensor and US\$0.10



Pill Camera and US\$0.25

View inside small intestine



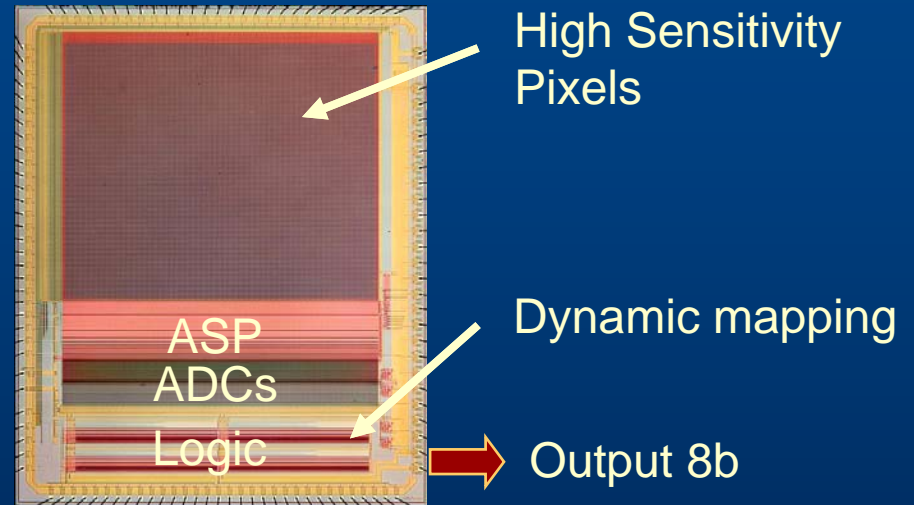
- Pixel Format: 256 X 256
- Pixel Size: 10  $\mu\text{m}$  X 10  $\mu\text{m}$
- Frame Rate: 2 fps
- ADC: On-Chip, 8 bits
- Power Supply: 2.8 V
- Power: 3 mW



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## Ultra-High Intrascene Dynamic Range Sensor for Automotive

Any one 8b image does not cover full intrascene dynamic range:



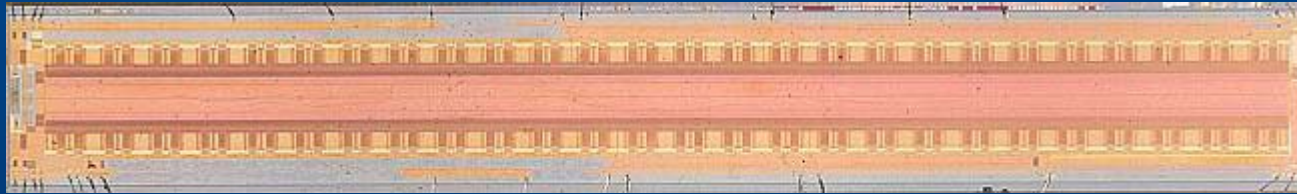
- Proprietary pixel design allows very high dynamic range  $>100$  dB image capture
- Preserves contrast unlike logarithmic sensors
- Low susceptibility to FPN compared to logarithmic sensors





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## High Speed Linear Sensor for Inspection



- 4096 x 1 linear array
- 7 um pixel pitch (28 mm long)
- Curtain-style readout
- 4 analog output ports, each 40 MHz
- 160 Mpix/sec total output rate
- 35,000 lines/sec
- 5 V operation
- Subwindowing allowed, from center



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## Linear Sensor for Fingerprint Scan



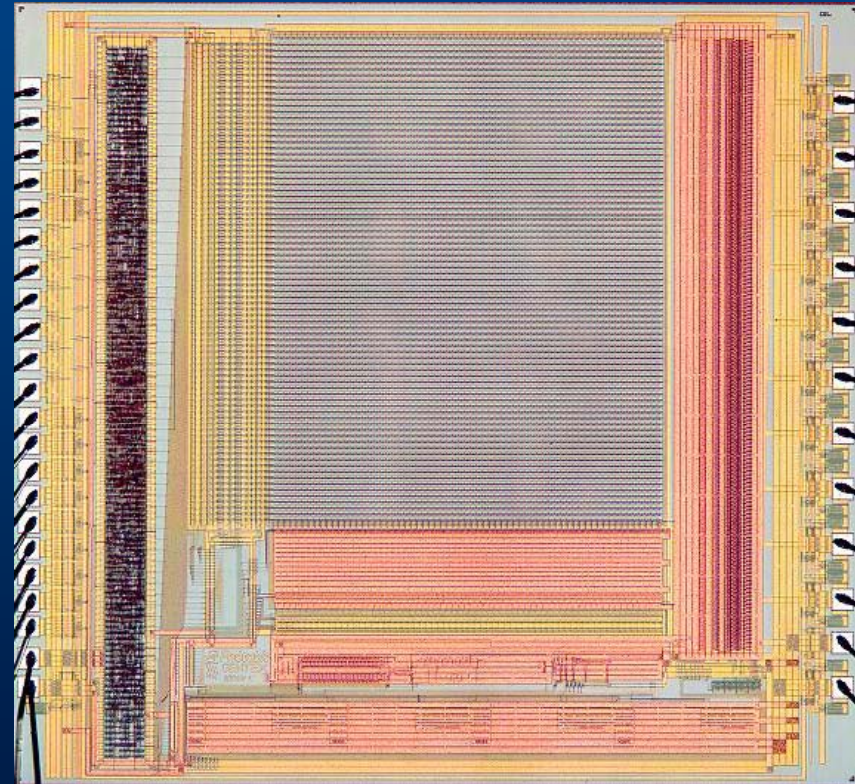
- 900 element linear sensor
- 1000 dpi scan density
- $> 9 \text{ V} / \text{lux-sec}$
- 10b ADC
- $< 150 \text{ mW}$  operation
- on-chip FIFO buffer
- 40 Mbytes/s readout rate
- SPI compatible serial interface



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## SmartBeam™ Headlight Dimmer Sensor

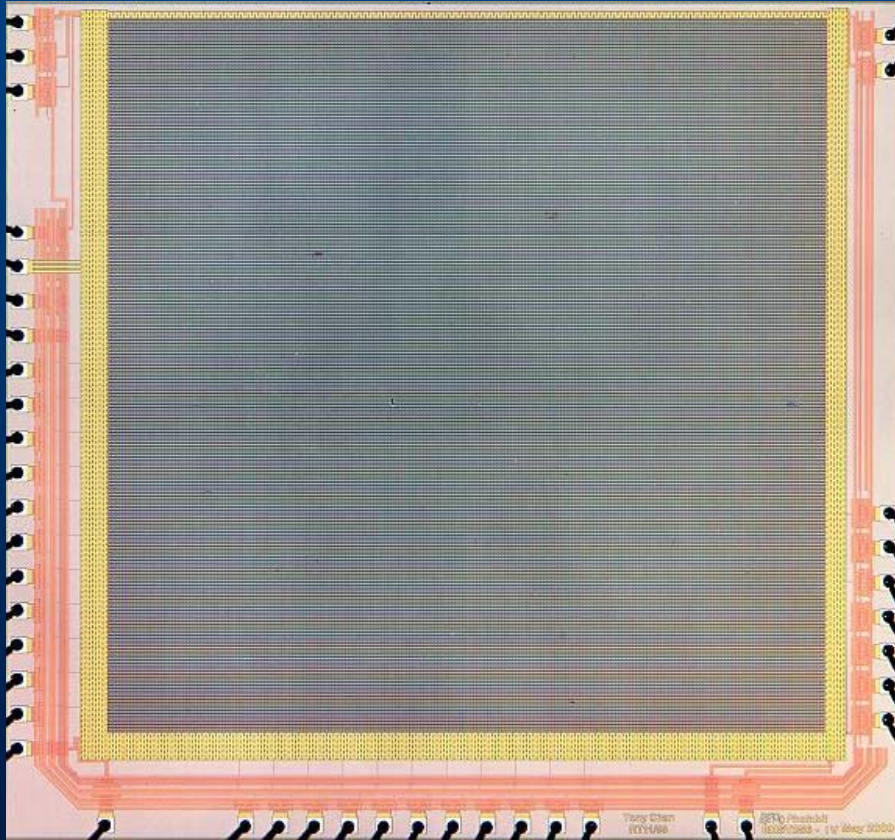
- Pseudo-random access readout
- High sensitivity photogate pixels
- 8b ADC
- SPI interface





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## Radiation Hard Star Tracker



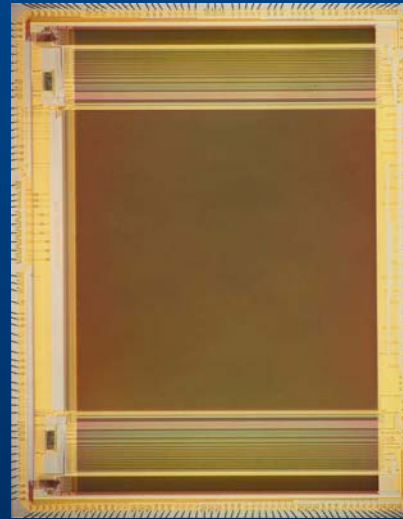
- 512x512 array
- Photodiode-type pixel with radiation tolerant readout circuitry
- 1 MHz analog output
- Individual pixel reset circuitry for ultra high dynamic range management
- Initial results shows sensor still working after 30Mrads



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## 1024x1024 (1.0 Mpix), 500 fps ERS

- 1024x1024 elements
- 10  $\mu\text{m}$  x 10  $\mu\text{m}$  pixel pitch
- 0.5  $\mu\text{m}$  CMOS
- 1024 on-chip 8b ADCs
- 8x8b digital output (64 pins)
- Open architecture
- 3.3 volt operation
- Power: 95 mW @ 60 fps
- Power: 450 mW @ 500 fps
- 500 bits/lx-s



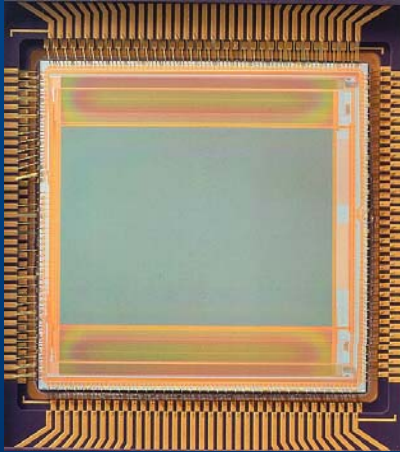
*Krymski, Van Blerkom, Bock, Anderson 1998*

© 2001 Photobit Technology Corporation

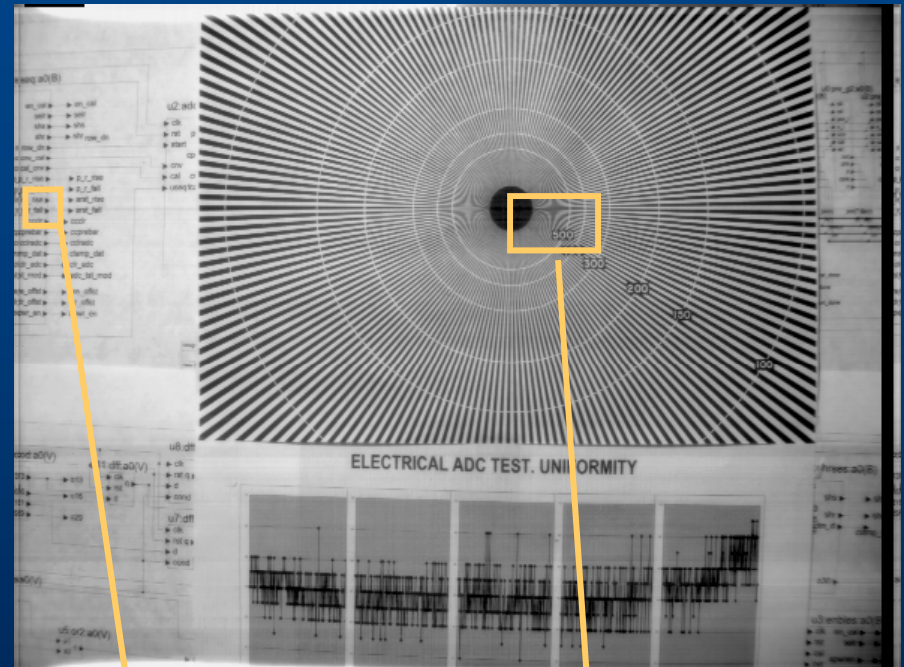


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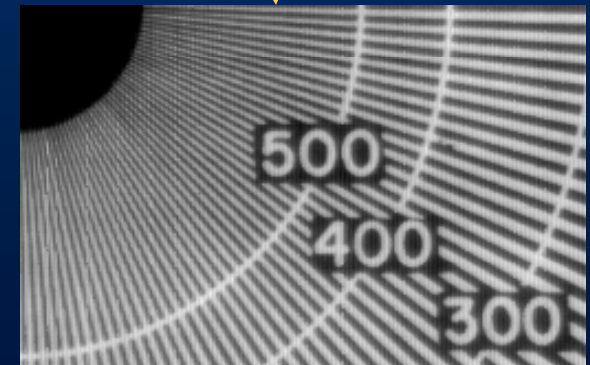
## PBMV40 (in development) 2352x1728 (4.1Mpix) 240fps ERS



- 4.1 Mpixel sensor
- 7  $\mu\text{m}$  x 7  $\mu\text{m}$  pixel pitch
- 16x10b digital output
- 240 fps ERS
- 960 Mbytes/sec at 66 MHz
- 4000 bits/lx-sec
- 3.3 volt operation



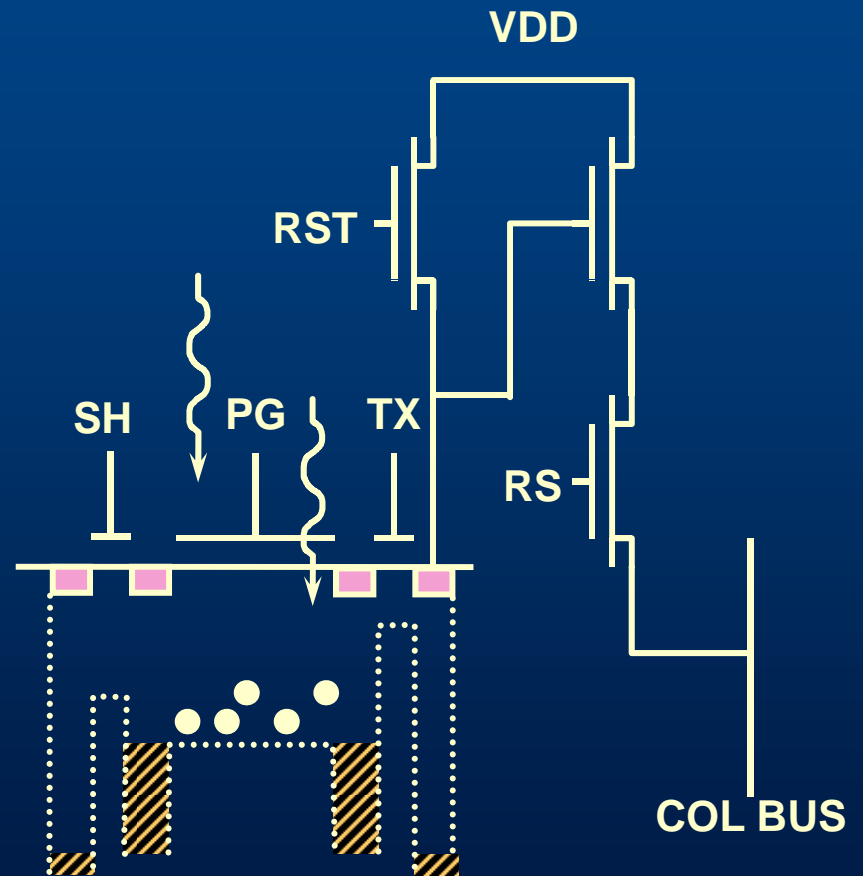
▶ p\_r\_rise  
▶ p\_r\_fall  
▶ arst\_rise  
▶ arst\_fall





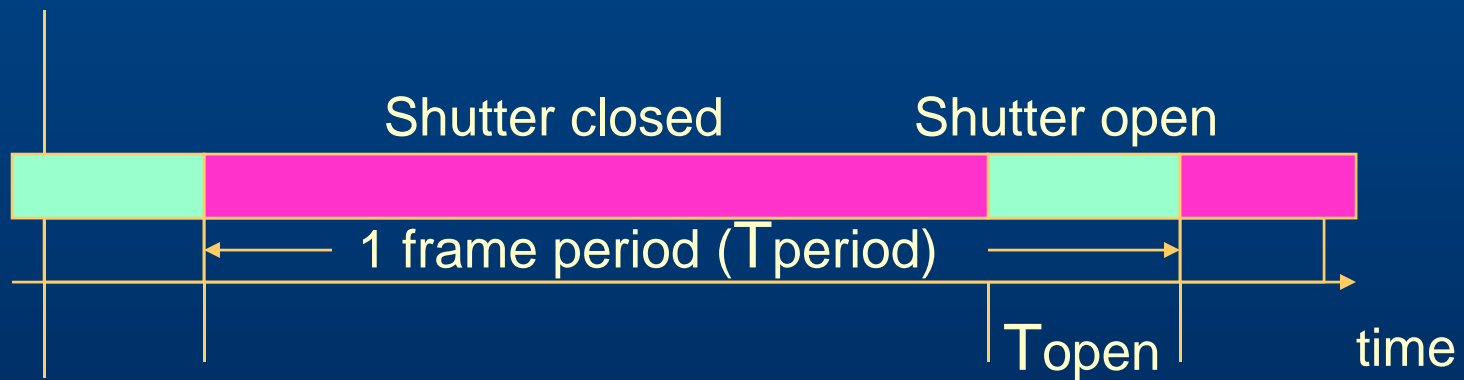
## Shuttered Node Active Pixel (SNAP)

- 6 transistor pixel
- Larger pixel
- QE loss due to poly gate
- Allows simultaneous integration across all pixels (freeze-motion)
- Shutter efficiency issue





## Shutter Efficiency

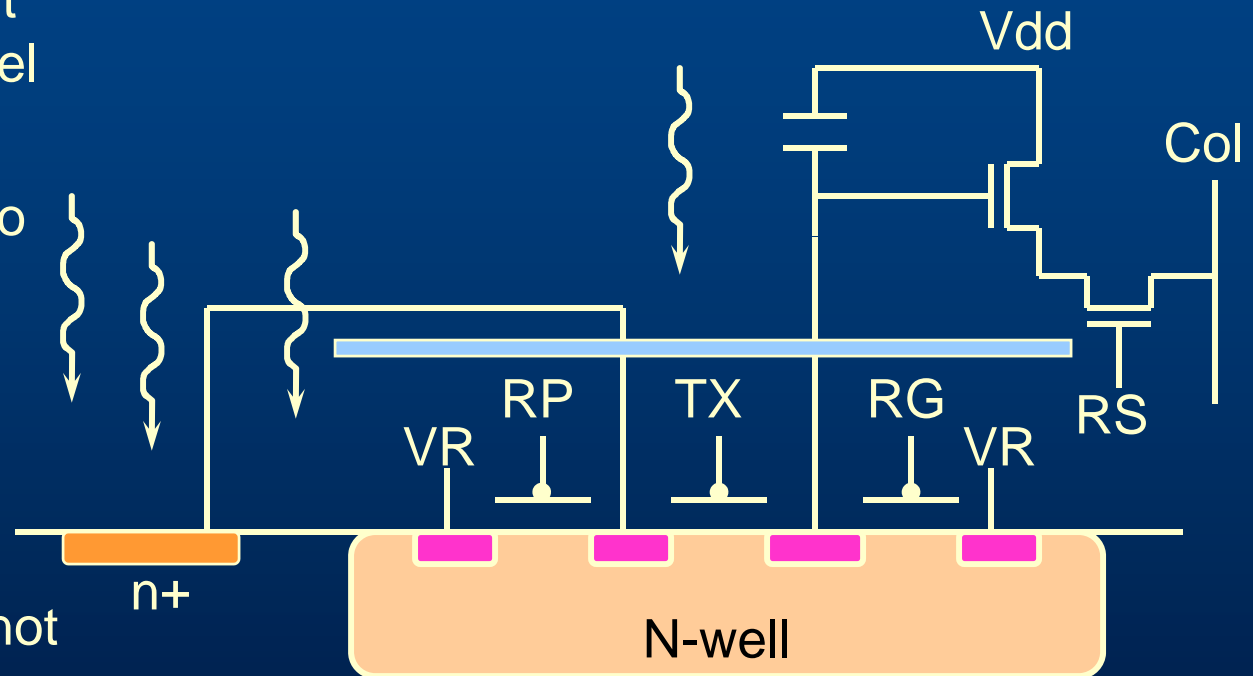


Ideal:  $\text{Signal} = T_{\text{open}} / T_{\text{period}} \text{Signal}_0$

Actual:  $\text{Signal} = T_{\text{open}} / T_{\text{period}} \text{Signal}_0 + (1-\varepsilon) \text{Signal}_0$   
where  $\varepsilon$  is the shutter efficiency



- Proprietary Photobit technology, 5-T pixel
- Normal photodiode
- Signal transferred to storage node in N-well
- Storage node read out in usual way
- Diffusing photoelectrons do not affect storage
- Very high shutter efficiency >99.9%

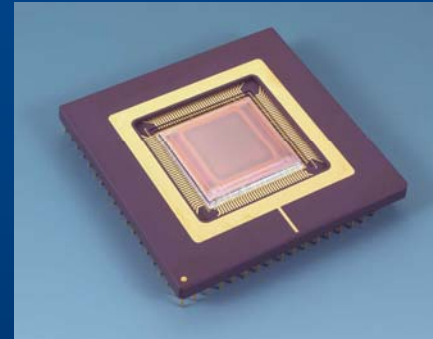




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TECHNOLOGY

**1280x1024 (1.3Mpix) 600fps**

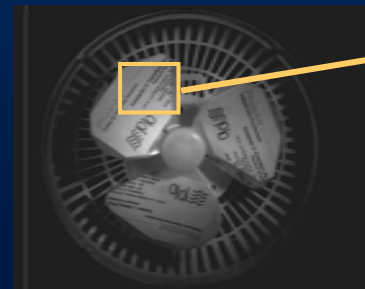
- 1.3 Mpixel sensor
- 12  $\mu\text{m}$  x 12  $\mu\text{m}$  pixel pitch
- 0.35  $\mu\text{m}$  CMOS
- High efficiency (>99.9%) freeze frame shutter
- Shutter speeds from 1/30th to 1/100,000th sec
- 10x10b digital output (100 pins)
- Open architecture
- 3.3 volt operation
- Power: <500 mW @500 fps
- 1000 bits/lx-s
- Color or monochrome



Color image with rotating fan



1/605 sec=1652 usec  
Rolling shutter



1/33,000 sec = 30 usec  
Freeze frame shutter

