CMOS ACTIVE PIXEL SENSOR (APS)
FY'95 TECHNICAL PROGRESS REPORT

presented to

Gordon Johnston, NASA Code X

and CSMT Review Board

by

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Imaging and Spectrometry Systems Technology Section

November 29, 1995

OUTLINE

1. Brief Overview
2. Program Objectives
3. Progress in FY'95
4. Publications, Inventions, etc.
5. Commercialization
6. Flight Applications
7. Costing, Schedule
8. Plans for FY'96

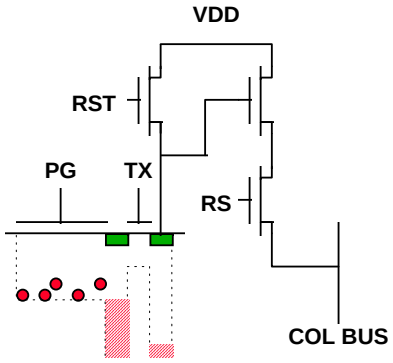
OVERVIEW

CMOS APS OVERVIEW

- Second generation solid-state image sensor technology invented at JPL in 1992 by Fossum, Mendis and Kemeny.
- Retains nearly all the performance of a CCD
- Uses mainstream microelectronics technology (CMOS)
- Unique advantages of CMOS APS:
  - Ultra low power system, >100x less than CCD system
  - Highly integrated on-chip electronics enables miniaturization
  - Commercial CMOS technology leverage
  - Don’t need a dedicated CCD fab line to make sensors ($$)
  - Random access and window-of-interest pixel readout
  - Standard 5 volt (or 3.3 volt) operation
  - Fast, digital readout
  - More radiation hard than CCDs
- Strong commercial, biomedical, defense, and space applications

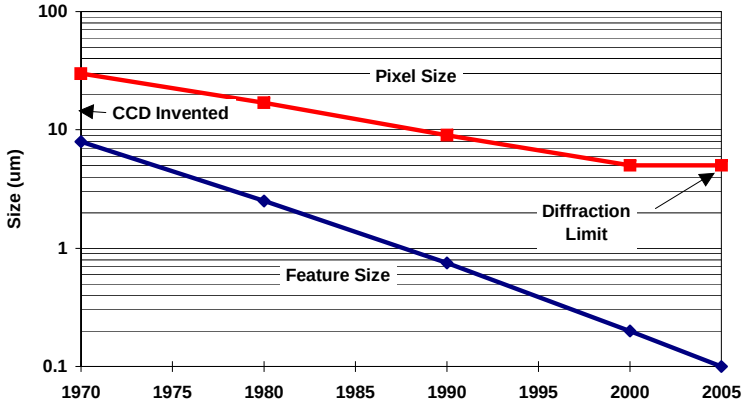
TECHNOLOGY OVERVIEW

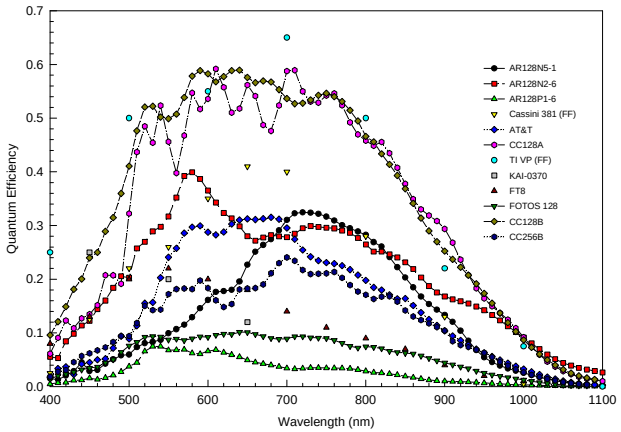
- ***APS exploits best of CCD and CMOS X-Y readout technology.***
- ***CCD detector structure***
- ***Low noise CCD amplifier***
- ***Random access X-Y readout wiring***



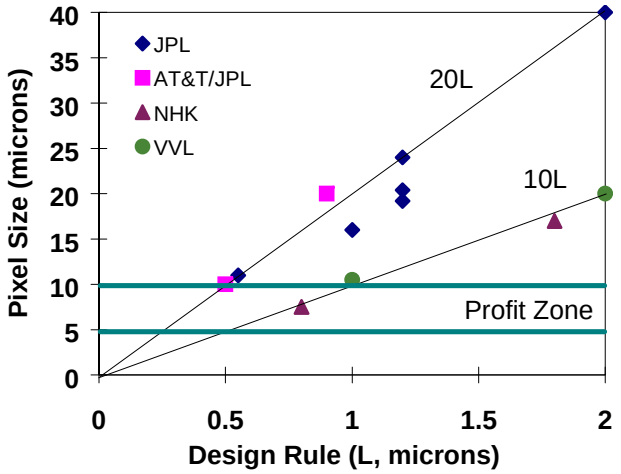
MICRO-CCD PIXEL CIRCUIT

- ***Amplifiers can be put into pixels.***





- ***APS has quantum efficiency competitive with CCDs***



- ***APS benefits from mainstream CMOS technology trend***

FLIGHT APPLICATIONS*

STRV2, STRV1c - Space Technology Research Vehicle

- Imaging and energetic particle detection/analysis

Champollian - CIRCLE

- Selected for Rosetta mission. APS major reason for success.

Mars98 - Dust and Volatile Element Sensor Camera

- Declined for Mars98. Waiting for next opportunity.

MISR II - Multi-angle Imaging Spectrometer/Radiometer II

- Lightweighting/miniaturization of Mission to Planet Earth instr.

PICS

- Slated to replace CCDs in New Millennium flight TBD.

**Discussed in detail in separate briefing*

PROGRAM OBJECTIVES

- Enable the miniaturization of future imaging systems for planetary spacecraft and satellites.
- Increase the scientific performance of CMOS active pixel sensors (noise, dynamic range, quantum efficiency, etc.)
- Increase the performance of on-chip analog-to-digital converters (resolution, accuracy, power, speed)
- Demonstrate highly integrated imaging systems using camera-on-a-chip technology.
- Transfer technology to US industry to increase National competitiveness.

1995 APS R&D TEAM

JPL:
Mr. John Alphonse-Gibbs
Mr. Christopher Clark
Dr. Thomas Cunningham
Mr. Nick Doudoumopoulos
Dr. Eric Fossum
Mr. Russell Gee
Dr. Bruce Hancock
Mr. Peter Jones
Dr. Sabrina Kemeny
Dr. Quiesup Kim
Mr. John Koehler
Mr. Junichi Nakamura
Dr. Barmak Mansoorian
Mr. Ken McCarty
Mr. Robert Nixon
Dr. Bedabrata Pain
Mr. Roger Panicacci
Mr. Peter Ringold
Mr. George Soli
Mr. Craig Staller
Dr. Orly Yadid-Pecht
Mr. Zhimin Zhou

AT&T:
Dr. Bryan Ackland
Dr. Alex Dickinson
Dr. Kamran Azadet
Mr. Dave Inglis
Dr. Sunetra Mendis
Dr. David Gibbons

Kodak Research Labs
Dr. Paul Lee
Dr. Tom Lee

UCLA:
Dr. Jason Woo

IBM:
Dr. Philip Wong

EG&G Reticon
Mr. Gene Weckler

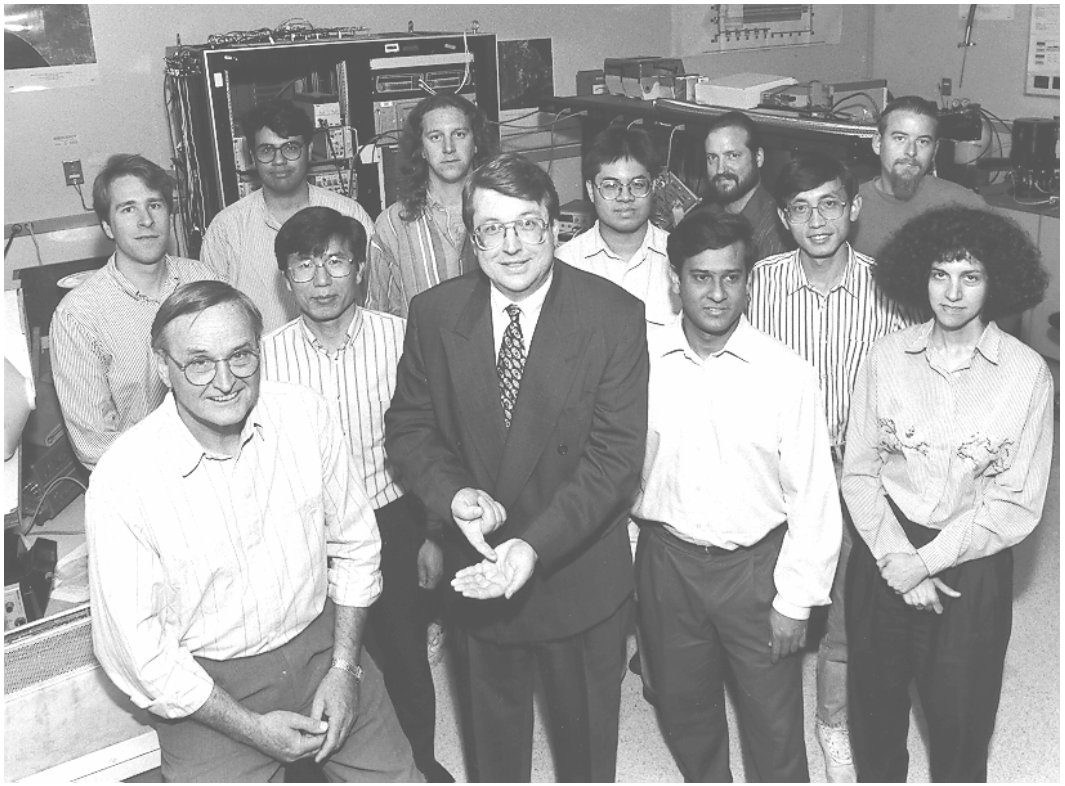
ITT
Mr. Richard Floryan
Mr. Chip Hambro

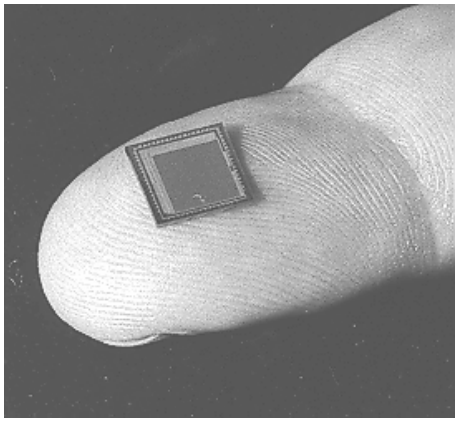
Polaroid:
Dr. Dan McGrath

Schick Technologies
Mr. David Schick
Mr. Dan Neugroschel
Mr. John Singer

National Semiconductor:
Mr. Kevin Brehmer
Mr. Dick Merrill

JPL APS TEAM





FY'95 PROGRAM ELEMENTS

• NASA Code X R&D	$250K
• NASA Code X New Millennium	$250K
• NASA Code X Tech. Transfer	$225K
• NASA Code SZ UV sensor	$150K
• NASA Code S PIDDP	$100K
• Defense Acceleration	$420K
• ARPA Wireless Camera	$285K
• DDF - Rad Hard APS Study	$ 70K
• PF - UCLA Collaboration	$ 35K
• Technology Affiliates Program	$ 50K
	=====
	$1835K

PROGRESS

256 x 256 CMOS APS
ANALOG CAMERA-ON-A-CHIP

Objective:

Demonstrate a 256x256 CMOS APS with on-chip timing and control and analog signal chain.

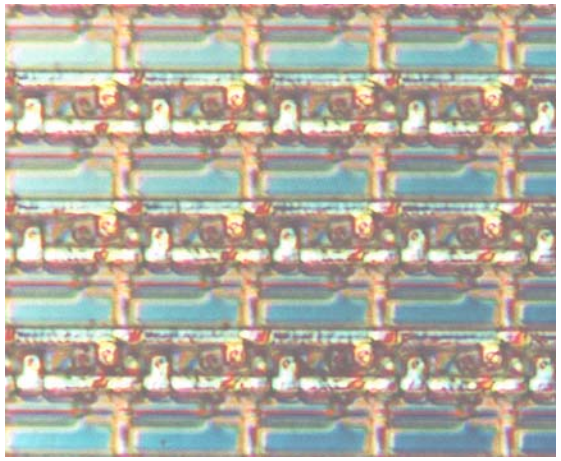
Status:

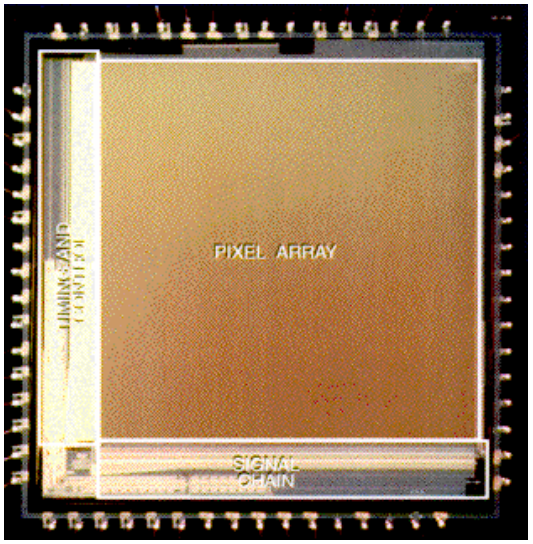
Chip worked on first silicon. Excellent performance. Some excess power dissipation due to design error. Corrected design in fabrication.

Sponsor:

NASA Code X APS R&D, Defense Acceleration

256x256 CMOS APS
With on-Chip Timing and Control Circuits





Pixel size:	20.4 μm
Pixel type:	photogate
Fill factor:	21%
Technology:	HP 1.2 μm n-well
Supply:	5 V

Array size: 256x256
Timing, control, CDS
FPN suppression
Motion detection
Window readout
Program. integration time

Conv. Gain:	10.6 μV/e-
Saturation:	800 mV
Noise:	13 e- rms
FPN:	0.15% sat
Dyn. range:	76 dB

REGIONAL ELECTRONIC SHUTTER

Objective:

Demonstrate an APS sensor that permits different exposures in different regions of the sensor, simultaneously, for star tracker applications. Enables simultaneous capture of guide stars, each independently optimized for centroiding exposure.

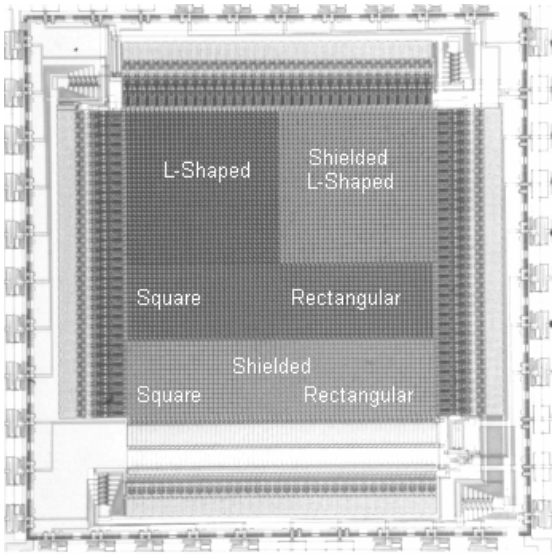
Status:

First chip fabricated and tested. Very good performance obtained.

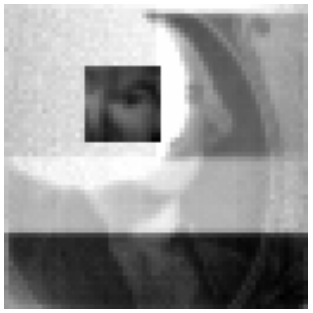
Sponsor:

NASA Code X APS R&D

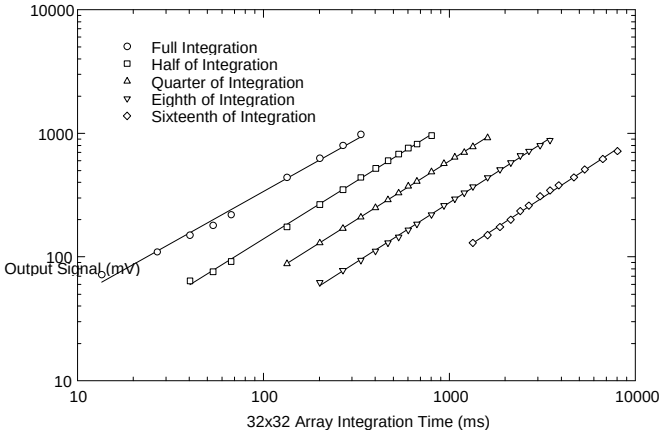
REGIONAL ELECTRONIC SHUTTER



Fabricated Sensor



Regional Shutter Gives Non-Saturated Image of Eye



- New individual pixel reset (IPR) circuitry in pixel
- Permits local reset and regional electronic shutter
- 64x64 element test chip fabricated and tested
- Six (6) different pixel geometries tested.
- Regional shutter works well
- Electronic IPR shutter adds more than 40 dB dynamic range.

STAR TRACKER

Objective:

Deliver APS to Star Tracker Group for independent verification of APS performance and assessment of usefulness in star tracker applications.

Status:

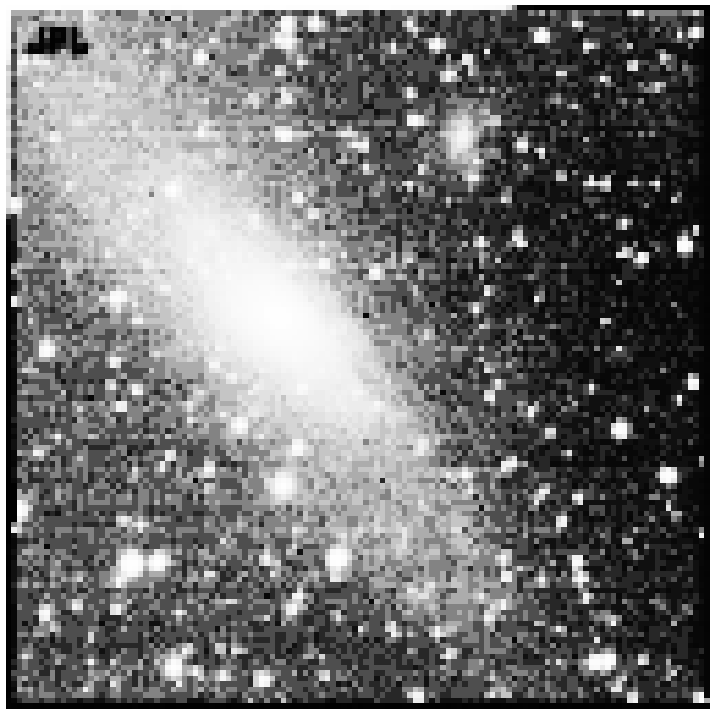
Camera built and tested at Table Mountain Observatory. Better-than-expected results obtained for centroiding. Residual noise in camera system limits performance of sensor.

Sponsor:

NASA Code X APS R&D + Star Tracker Group's Program

STAR TRACKER

- **Star tracker camera built and tested**
- **Uses JPL CC128A APS**
  - -128x128 elements, PD APS
  - -On-chip timing and control
- **Tested at Table Mtn. Obs.**
- **Results:**
  - - “Extremely low dark current, like MPP CCD”
  - - “Very large pixel capacity (full well)”
  - - “Well-managed blooming control”
  - - “Excellent spectral sensitivity to stars”
  - - “Centroiding appears to be well behaved” (<1/20 pixel)
- **Independent verification of APS performance**



Andromeda Galaxy

E. Dennison, C. Clark, and G. Udomkesmalee 10/95

ANALOG TO DIGITAL CONVERTERS

Objective:

Develop on-chip ADC technology for CMOS APS applications. Requires low power, very compact layout and good performance at reasonable speeds.

Status:

Several test chips completed. Single slope ADCs slow but good for 10 bit resolution. Successive approximation ADCs need improvement, but adequate for many commercial applications. Oversampled ADC achieves 12 bit resolution but 8-9 bit absolute accuracy. Research continuing.

Sponsors:

JPL DDF, NASA Code X APS R&D, Defense Acceleration, ARPA

LARGE FORMAT APS

Objective:

Develop a 1024x1024 element sensor with on-chip ADC.

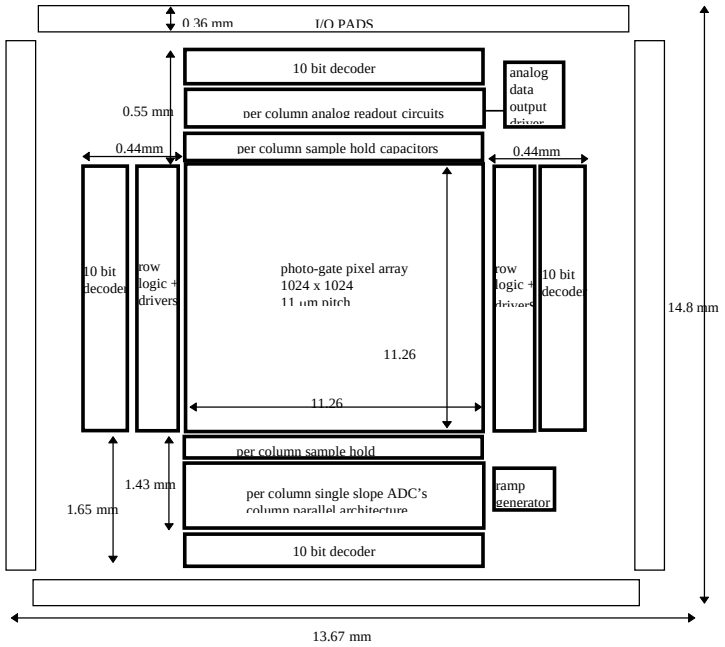
Status:

Using a technology cooperation agreement with National Semiconductor, a 1Kx1K sensor has been designed at JPL and is in fabrication at National. Chip is expected 12/21/96. Several smaller chips are also in fabrication.

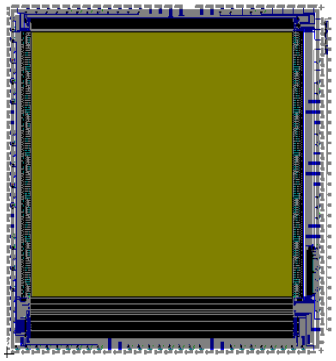
Sponsor:

NASA Code X APS R&D, Defense Acceleration, PIDDP

LARGE FORMAT APS



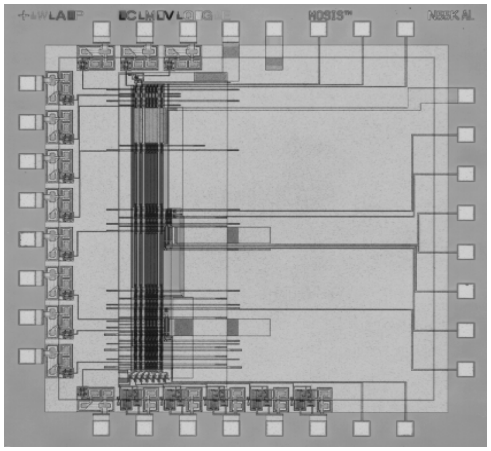
1K x 1K APS block diagram and chip dimensions for NSC 0.55 μm N-well process



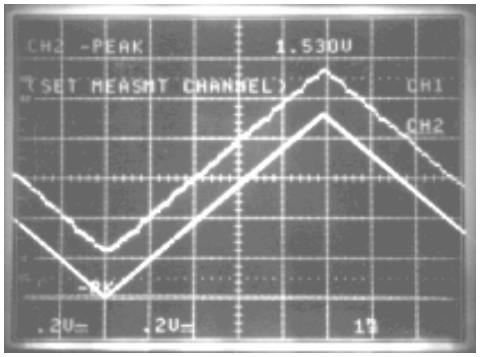
NSC 1Kx1K with on-chip ADC layout

- 1024 x 1024 Active Pixel Sensor with on-chip analog to digital conversion developed for PIDDP
- 0.55 μm N-well CMOS technology - National Semiconductor Corp.
- 10 bit single slope ADC
- On-chip ramp generator
- Analog readout port
- 3-5 Hz frame rate
- 50 mW power @ 3.3V operation
- photogate, photodiode versions
- Fabrication started 9/21, target delivery date 12/21
- 352 x 288 design started - for 0.8 μm process in collaboration w/ NSC

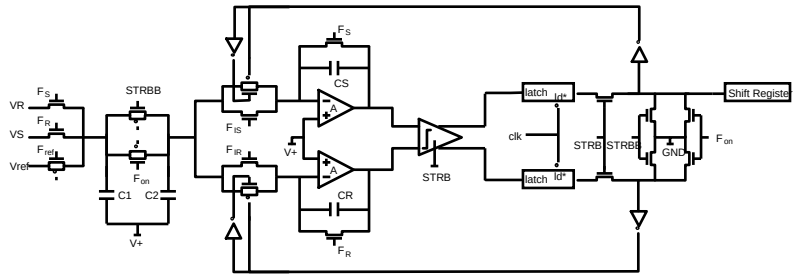
SUCCESSIVE-APPROXIMATION ADC
(SWITCHED CAPACITOR INTEGRATOR)



Photograph of Successive Approximation ADC test chip (2.77 mm x 2.81 mm)



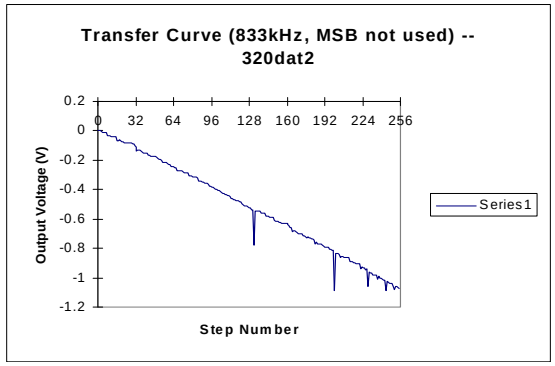
ADC response (top trace) to a 1V triangle wave input (bottom trace) at 20 usec conversion rate.



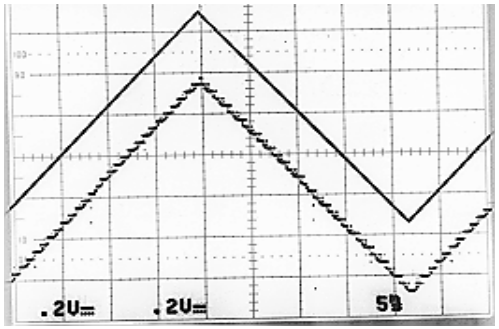
SA-ADC circuit using switched capacitor integrator approach

- Successive-approximation ADC test chip with multiple ADCs and op amps fabricated for characterization
- 1.2 um N-well CMOS process
- 50 kHz conversion rate per channel (8-bits)
- 20.4 um x 1.94 mm ADC size (w/o shift register readout)
- High gain folded cascode amplifier results:
  Gain: 10,400 Power: 20 uW Size: 20.4 x 104 um

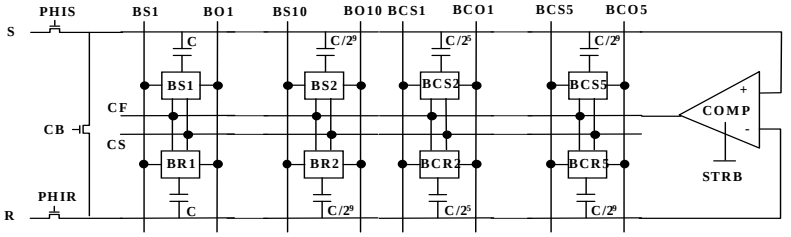
SUCCESSIVE-APPROXIMATION ADC
(CAPACITIVELY COUPLED)



Dual sided scaled capacitor SA-ADC output for a 256 step ramp input (x-axis is input step number, y-axis is response from a DAC using SA-ADC digital output).



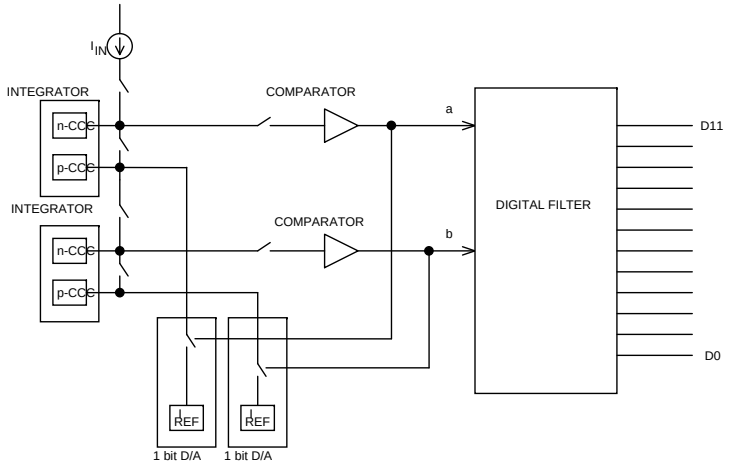
Single side scaled capacitor SA-ADC response (bottom trace) to a 1V triangle wave input (top trace).

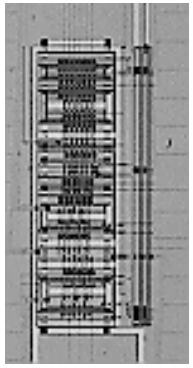


Dual sided capacitor scaled Successive approximation ADC circuit

- Capacitor Scaled Successive-Approximation ADC test chips with dual and single sided capacitor banks
- 830 KHz conversion rate for 8 bits
- 40 µm x 5.5 mm for dual sided version in 2 µm N-Well, Double Poly, Orbit CMOS (includes shift register readout)
- 24 µm x 3.2 mm for single sided version in 1.2 µm HP CMOS (includes shift register readout)
- 50 µW @ 5V supply (comparitor bias current)

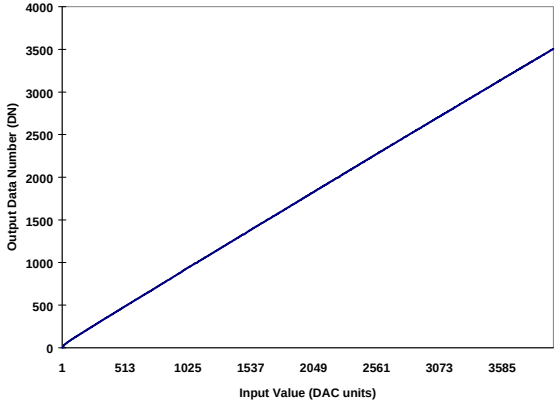
12 BIT Σ–Δ CURRENT MODE ADC





- 12 bit oversampled 2nd order ADC
- Current mode implementation
- 2 μm Olympus CMOS process
- 3 modulators in test chip
- ADC is 80 μm x 2.4 mm

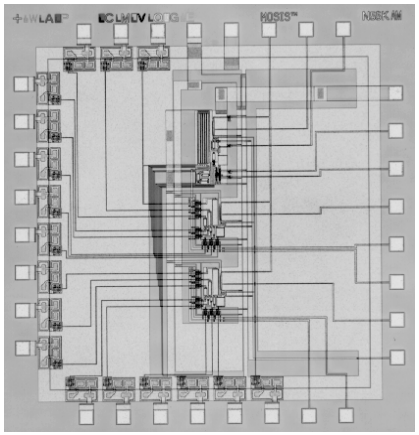
Output vs. Input



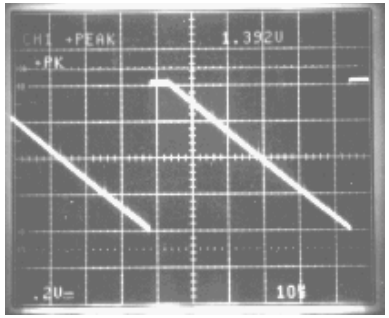
Performance

- 5-10 kS/sec per channel
- <800 μW/channel
- 1 ADC per 8 columns
- INL < 30 LSBs
- DNL < 4 LSBs

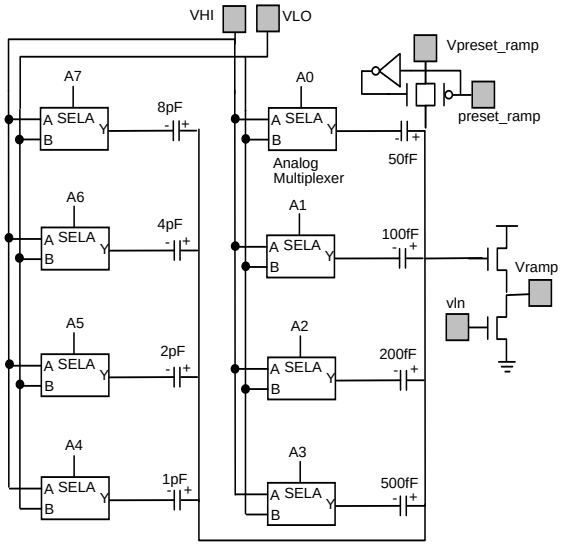
RAMP GENERATOR



Photograph of ramp generator test chip (2.77mm x 2.81 mm)



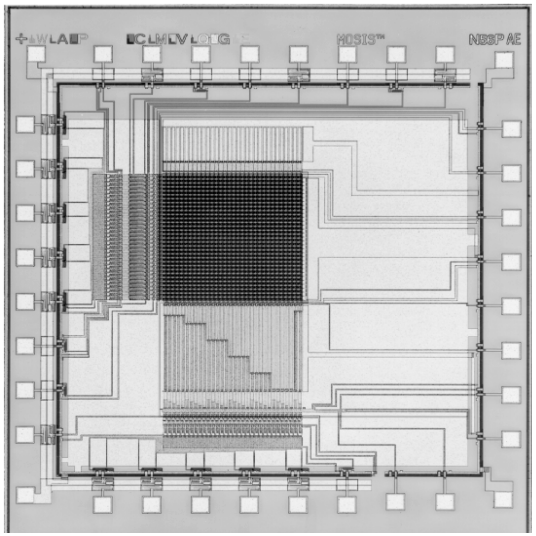
Output response of 8 bit ramp generator (256 steps). 1V ramp @ 4mV/step



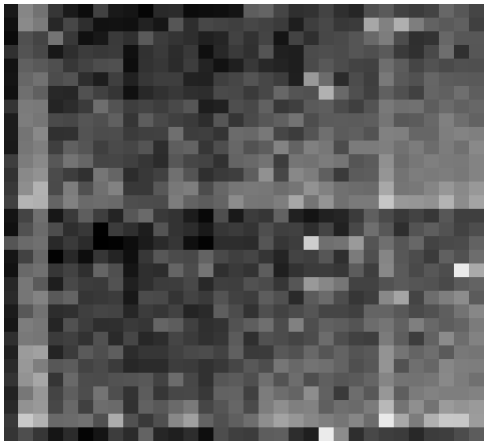
8-bit DAC ramp generator - scaled capacitor network circuit

- Ramp generator test chip with a scaled capacitor network design and integrator op-amp design approach
- Ramp generator used for single-slope ADCs
- 1.2 μm N-WELL CMOS
- 100-200 nsec / step (256 steps for 8 bit design)
- Adjustable ramp amplitude and shape

Noise Test Chip



Noise Map



Darker areas denote lower noise
Noise: 7-20 e^-
Conversion: 4-10 $\mu V/ e^-$

- 32 x 32 Element
- **Matrix of varying pixel and readout designs**
- 1.2 μm CMOS HP
- 20.4 μm pixel
- PG APS design

MULTIRESOLUTION IMAGING SENSOR

Objective:

Develop a multiresolution image sensor for rover vision applications that permits low resolution readout without aliasing effects, and windowed readout in selected regions.

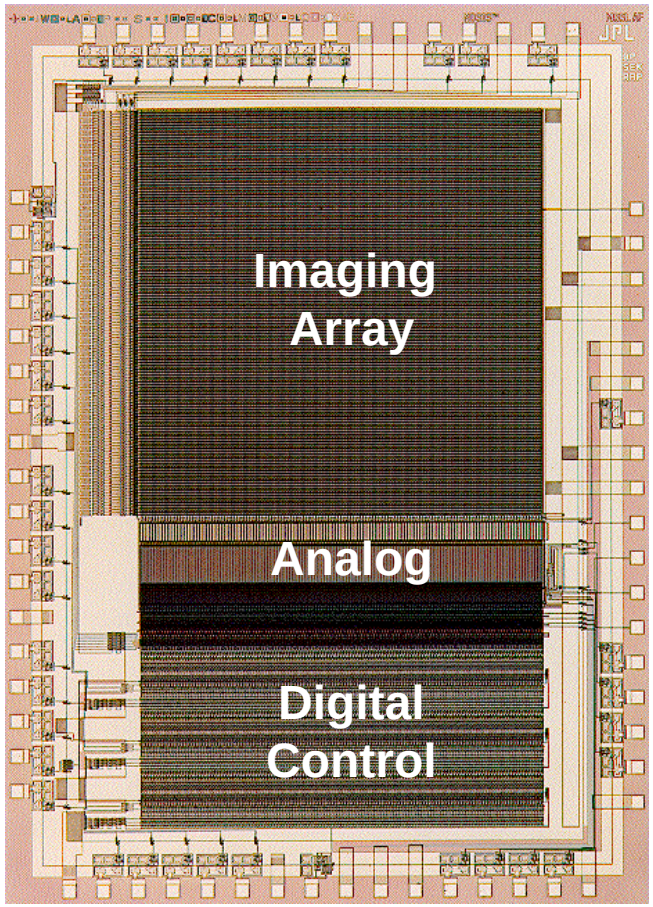
Status:

Chips fabricated and tested. Performance is excellent.

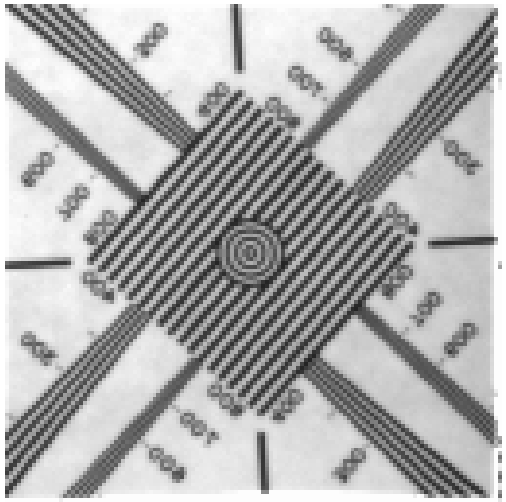
Sponsor:

JPL DDF

MULTIRESOLUTION IMAGING SENSOR



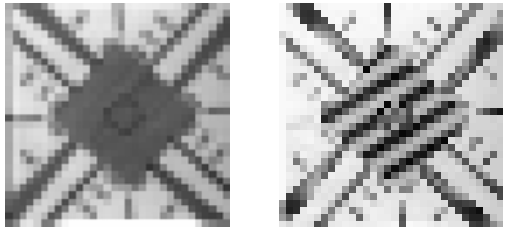
Process:	HP 1.2 um n-well CMOS
Pixel pitch:	24 um
No. pixels:	128 x 128
Pwr suppy:	5 volts
Saturation:	1200 mV
Conv. gain:	8 uV/e-
Noise:	116 uV rms 15 e- rms
Dynamic Range:	80 dB
FPN:	<3 mV p-p <2.5 %
Power: at 30Hz	< 5 mW



Full resolution image

4x4 Averaged image (left)

1/4 Subsampled image (right)



Kemeny, Panicacci, Pain, Matthies, Fossum 1995

UV PHOTOELECTRON COUNTING SENSOR

Objective:

Develop a hybrid sensor for UV photon counting. Develop a readout chip sensitive enough to sense individual photoelectrons coming from the detector material.

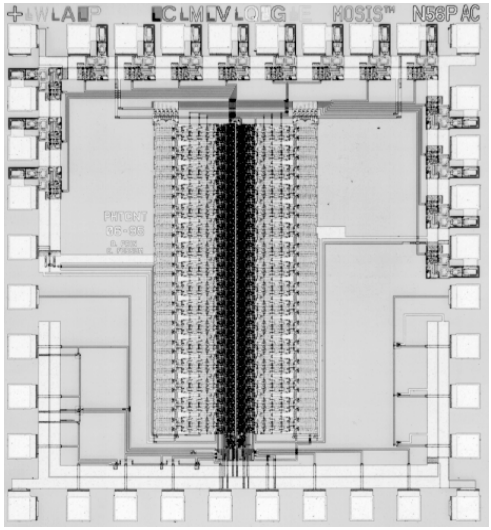
Status:

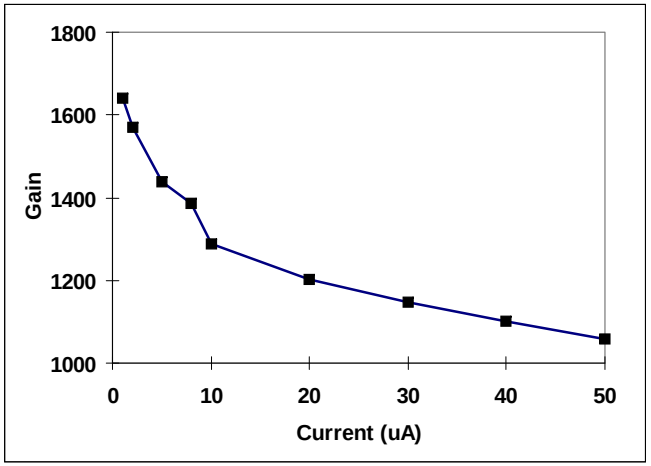
16x2 pixel readout amplifier chip designed, fabricated and tested. Amplifiers appear to have the required performance. A larger array with multiplexer is in progress.

Sponsor:

NASA Code SZB - Weiler

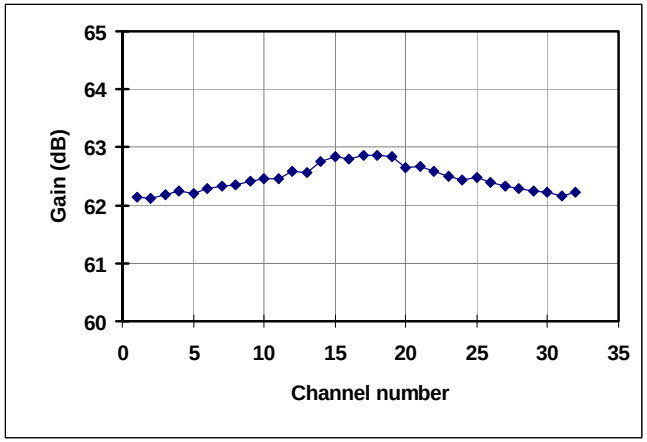
UV PHOTOELECTRON COUNTING SENSOR





Measured Amplifier characteristics

- Gain: > 63 dB
- Gain variation: < 8%
- Operating current range: 1- 50 μA
- Power: < 50 μW per amplifier
- Cut-off frequency: 2 MHz
- Typical Self-biasing time: 2 μs.
- Size: 5100 sq-μm^2



B.Pain 1995

NON-VISIBLE IMAGING APPLICATIONS

Objective:

Explore other applications of CMOS APS technology for imaging particles, x-rays, high energy photons, low energy ions, etc.

Applications:

Medical x-rays, solar physics, space radiation effects, mass spectroscopy, DNA sequencing, etc.

Progress:

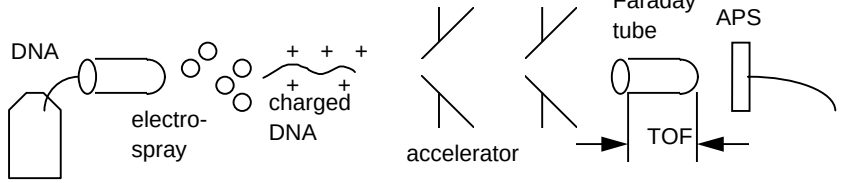
Initial measurements of APS in various environments encouraging. Fabricated several custom APS chips for low energy charged particle measurement and space physics.

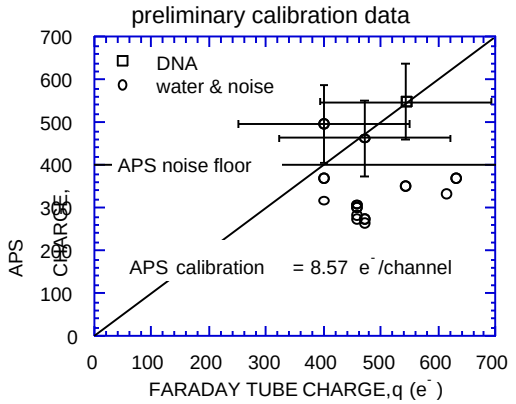
Sponsor:

NASA Code X APS R&D, misc. B&P

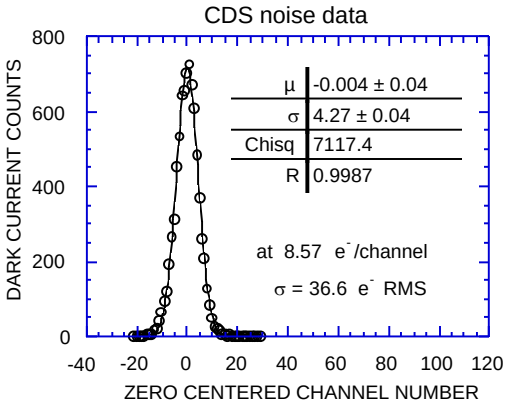
Human Genome Center
APS DNA CHARGE MEASUREMENTS

Electro Spray Ionization





- **APS enables order-of-magnitude increase in resolution**
  - **DNA mass sequence fine structure measurable**
  - **fast disease diagnosis by live virus mass measurement**
- **APS low cost and simple operation commercializes instrument**



Soli, Gee and Fossum 1995

COMMERCIALIZATION

COMMERCIALIZATION

Signed Technology Cooperation Agreements:

- AT&T - Videophone $75K
- Kodak - Pinned photodiode CMOS APS $75K
- Schick - Dental x-ray CMOS APS $75K
- National Semiconductor - Mixed Analog/Digital new

Technology Affiliates Program

- EG&G Reticon $50K
- ITT $50K

JPL Spin-off Company

- Photobit

Misc

- Polaroid, IBM, HP?

SCHICK TECHNOLOGIES
Overview

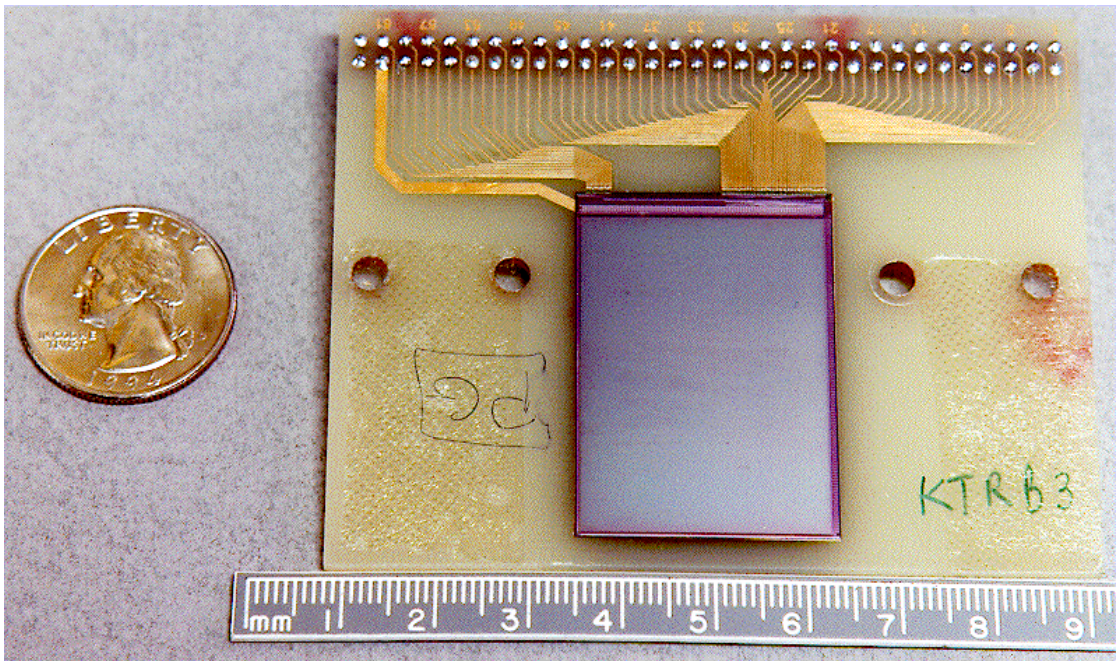
- Schick has pioneered computed dental radiography using large area CCD sensors.
- Product is complete system for dentist's office
  - Sensor heads (at least 3 sizes)
  - Computer hardware
  - Image processing software
  - Data archiving software
- Major market obstacle is cost of sensor heads
- Schick contacted JPL as 3-man company in early 1994
- JPL asked to design a large area CMOS APS for computed dental radiography.
- Schick Technologies is now a 40+ person company

SCHICK TECHNOLOGIES
Progress

- 6 sensors were designed at JPL
  - 375x550, 500x875, 675x900 elements
  - 40 micron pixel pitch, PG and PD-type pixels
  - On-chip timing, event trigger, auto dark frame readout.
- Masks were fabricated in USA
- Chips were fabricated overseas
- Initial screening performed by JPL indicated process basically OK using test chip, but chips had problems
- JPL, using ion milling and deposition, identified several design modifications that were required
- JPL performed redesign of sensors
- New chips currently in fabrication

SCHICK TECHNOLOGIES

675x900 Element CDR APS



PROPRIETARY - For Official Use Only

KODAK
Overview

- Kodak has major investment in electronic imaging using charge-coupled devices (CCDs)
- Collaboration began with call to Kodak to collaborate on active pixel sensor technology (before invention of CMOS APS)
- Kodak cautious but agrees to fund its half of collaboration
- Kodak has 2 micron CMOS process running (1985 technology) as captive process with 1.2 micron CCD process.
- Kodak has license from NEC and understanding of pinned photodiode structure
- TCA formed to investigate CMOS APS using pinned photodiode pixel element

KODAK
Progress

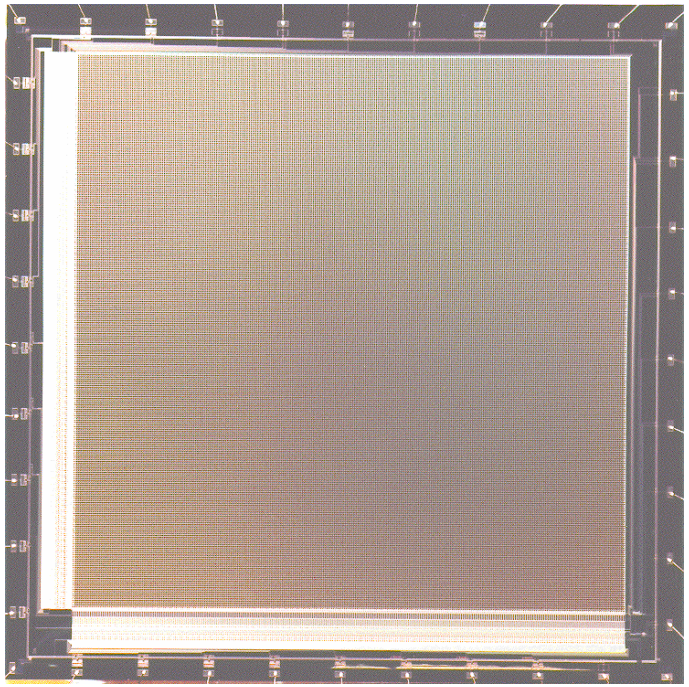
- CMOS/PPD process developed by KRL in collaboration with JPL. Patent filed by KRL.
- 256x256 element CMOS APS chip with PPD pixels designed at KRL and at JPL. NTR submitted to JPL.
- Chip fabricated at KRL (>6 months elapsed time)
- Obvious design flaws found with mysterious origins probably related to electronic data transfer process.
- Capability to design chips at JPL developed
- Capability to verify designs at JPL developed
- New sensor to be fabricated by KRL

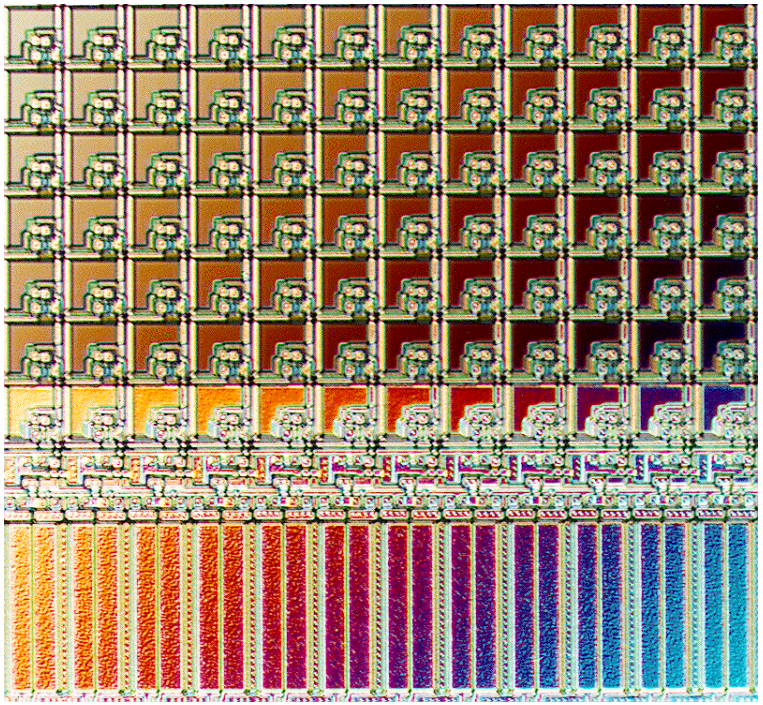
JPL

KODAK

CSMT

256 x256 CMOS APS with Pinned Photodiode Pixels





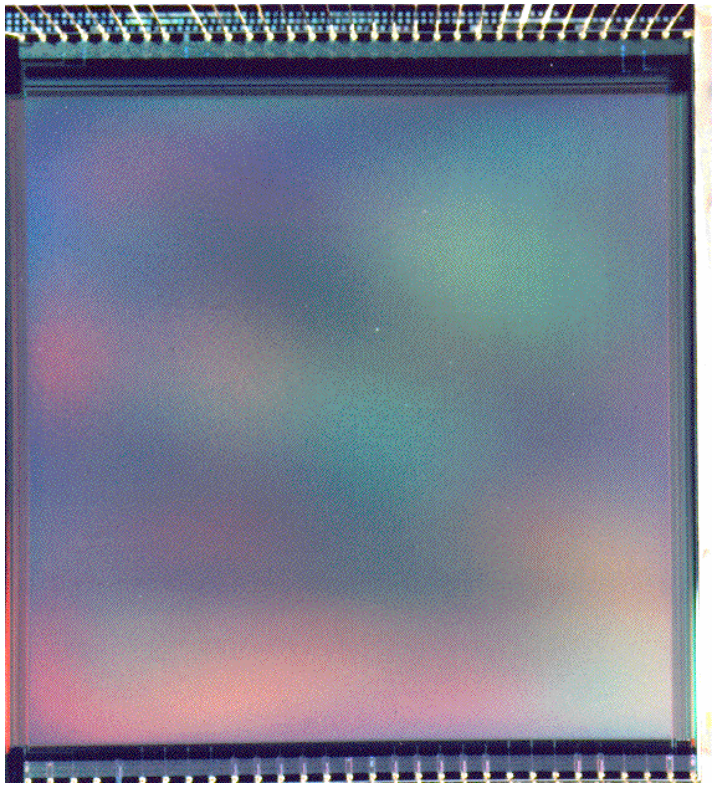
AT&T Bell Laboratories Overview

- AT&T wants to sell bandwidth over their network. Video phones and PC video conferencing cameras use a lot of bandwidth.
- AT&T approached JPL for help in making CMOS image sensors for video phones.
- AT&T has captive foundry for making chips with 0.9 micron, 0.5 micron and 0.35 micron design rules.
- AT&T Bell Laboratories must market technology to AT&T operating companies such as AT&T Microelectronics and AT&T Consumer Products.

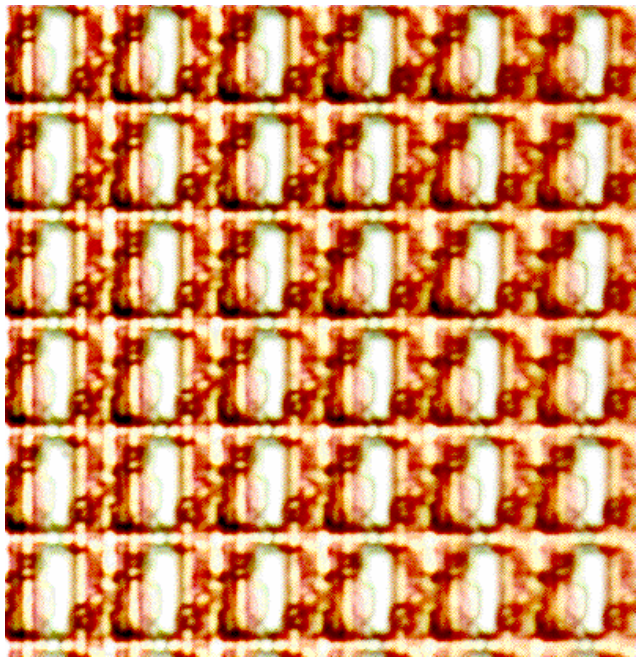
AT&T Bell Laboratories
Progress

- Demonstrated 176x144 element sensor (QCIF format)
- Demonstrated 256x256 element sensor
- JPL built first demo camera using 256x256 sensor
- Demonstrated 176x144 element sensor with on-chip 8b ADC
- Demonstrated 1024x1024 element sensor (oxide leakage problem discovered on 0.5 micron fab line)
- AT&T nearly autonomous and tech transfer nearly completed.

AT&T/JPL 1024x1024 Element Array with 10 um Pixels



Chip



Closeup of pixels

PUBLICATIONS, INVENTIONS AND NOTABLE EVENTS

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J. Nakamura, S.E. Kemeny and E.R. Fossum, A CMOS active pixel image sensor with simple floating gate pixels, IEEE Trans. Electron Devices, vol. ED-42(9) pp. 1693-1694 (1995).

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A. Dickinson, B. Ackland, E-S. Eid, D. Inglis and E.R. Fossum, A 256x256 CMOS active pixel image sensor with motion detection, pp. 226-227, 1995 IEEE International Solid State Circuits Conference, Digest of Technical Papers, San Francisco CA, February 1995.

A. Dickinson, B. Ackland, El-Sayed Eid, D. Inglis and E.R. Fossum, Standard CMOS Active Pixel Image Sensors for Multimedia Applications, Proc. 16th Conference on Advanced Research in VLSI, UNC-Chapel Hill, March 26-29, 1995.

E.R. Fossum, Overview of CMOS Image Sensor Technology, Proc. of Optoelectronics Industry Development Association (OIDA) Technology Workshop on Optoelectronic Sensors, Albuquerque New Mexico, March 7-8, 1995.

P.P.K. Lee, R.C. Gee, R.M. Guidash, T-H. Lee, and E.R. Fossum, An Active Pixel Sensor Fabricated Using CMOS/CCD Process Technology, in Program of 1995 IEEE Workshop on CCDs and Advanced Image Sensors, Dana Point, CA, April 20-22 1995.

Z. Zhou, S.E. Kemeny, B. Pain, R.C. Gee, and E.R. Fossum, A CMOS Active Pixel Sensor with Amplification and Reduced Fixed Pattern Noise, in Program of 1995 IEEE Workshop on CCDs and Advanced Image Sensors, Dana Point, CA, April 20-22 1995.

S. E. Kemeny, B. Pain, R. Panicacci, L. Matthies, and E.R. Fossum, CMOS Active Pixel Sensor Array with Programmable Multiresolution Readout, in Program of 1995 IEEE Workshop on CCDs and Advanced Image Sensors, Dana Point, CA, April 20-22 1995.

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R. Panicacci, S. E. Kemeny, P.D. Jones, C. Staller, and E.R. Fossum, High Speed CMOS Binary Active Pixel Image Sensor, in Program of 1995 IEEE Workshop on CCDs and Advanced Image Sensors, Dana Point, CA, April 20-22 1995.

PUBLICATIONS (cont.)

E. R. Fossum and Philip H-S. Wong, Future Prospects for CMOS Active Pixel Image Sensors, in Program of 1995 IEEE Workshop on CCDs and Advanced Image Sensors, Dana Point, CA, April 20-22 1995.

E.R.Fossum, T.J. Cunningham, T.N. Krabach, and C.O. Staller, Monolithic Active Pixel Infrared Sensors, NASA Tech Briefs, pg. 24a, vol. 19(6), 1995.

E.R. Fossum, S. Mendis, B. Pain, and R. Nixon, Active-pixel image sensor with analog-to-digital converters, NASA Tech Briefs, pp. 37-38, vol. 19(7), 1995.

E.R. Fossum, Low power camera-on-a-chip using CMOS active pixel sensor technology, Proc. 1995 Symposium on Low Power Electronics, San Jose, CA, Oct. 9-10, 1995.

G.A. Soli, H.B. Garrett, E.R. Fossum, CMOS charged particle spectrometers, Proc. IEEE 1995 Nuclear Science Symposium and Medical Imaging Conference, October 25, 1995.

INVENTIONS

E.R. Fossum, J. Nakamura, and S.E. Kemeny, *Simple floating gate active pixel sensor,* JPL New Technology Report NPO-19621/9229 (1995).

H. Langenbacher, S.E. Kemeny, E.R. Fossum*, CMOS active pixel sensor array with intensity driven readout,* JPL New Technology Report NPO-19539/9145 (1995).

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E.R. Fossum, R.C. Gee, P.K. Lee, T-H. Lee, and R.M. Guidash, *A CMOS active pixel sensor using a pinned photodiode,* JPL New Technology Report NPO-19648/9258 (1995).

O. Yadid-Pecht and E.R. Fossum, *Method of Operating an Image Sensor with Ultra High Dynamic Range,* JPL New Technology Report NPO-19705/9318 (1995).

Other Notable Events

- Invited for Plenary talk at IEEE Int'l Electron Devices Mtg Dec. '95 (>3000 persons).
- AT&T invited for Plenary talk at IEEE Int'l Solid State Circuits Conference Feb. '95 on CMOS APS transferred from JPL.
- JPL/CSMT organized and hosted 1995 IEEE Int'l Workshop on CCDs & Advanced Image Sensors. Limited to 100 attendees.
- CMOS APS Image Sensors chosen as featured special workshop topic for 1996 ISSCC.
- APS featured in Mar. 6, 1995 Business Week (2 pages).
- Numerous other articles, interviews, incl. BBC radio.
- Recipient of 1995 NASA Space Act Award.

FY’96

Anticipated APS Program Funding FY'96

	FY'95	FY'96	
• NASA Code X R&D	$250K	$250K	
• NASA Code X New Millennium	$250K	$ 50K	need help
• NASA Code X Tech. Transfer	$225K	$225K	
• NASA Code S PIDDP carryover	$ 50K	$ 50K	
• NASA Code SZ UV sensor	$150K	$150K	
• Defense Acceleration	$420K	$420K	
• ARPA Wireless Camera	$285K	$550K	
• DDF - Rad Hard APS Study carryover	$ 20K	$ 50K	
• PF - UCLA Collaboration carryover	$ 20K	$ 15K	
• Technology Affiliates Program carryover	$ 5K	$110K	
• NASA Code Q Rad Effects		$100K	
• BMDO - Large Area Sensor		$200K	maybe
• AF Philips Lab - Rad Hard APS		$200K	maybe
	=====	=====	
	$1675K	$2370K	

MAJOR MILESTONES END FY'96

- Demonstrate 256x256 element sensor digital camera-on-a-chip.
- Demonstrate 1024x1024 element sensor with on-chip ADC
- Complete 2nd generation demonstration camera
- Develop CMOS APS time-delay and integration (TDI) technology
- Demonstrate camera operating over wireless link
- Complete tech transfer to AT&T, Schick and Kodak.

Other milestones dependent on actual FY'96 funding and customer goals.

SUMMARY

- JPL CMOS APS has changed the course of image sensor development world-wide, and is widely acknowledged.
- Significant progress made in FY'95 (it took more than 15 yrs to develop 1Kx1K CCD)
- Significant technology transfer and commercialization activity
- Growing acceptance in scientific community.
- Enabled the multi-eyed CIRCLE camera and selection for Rosetta/Champollian (lander) comet mission.

- Need more funding for baseline R&D (currently $250K).
- Progress limited by funds for fabricating silicon.
- Need to demonstrate microlens technology.