CMOS Image Sensors: Electronic Camera-on-a-Chip

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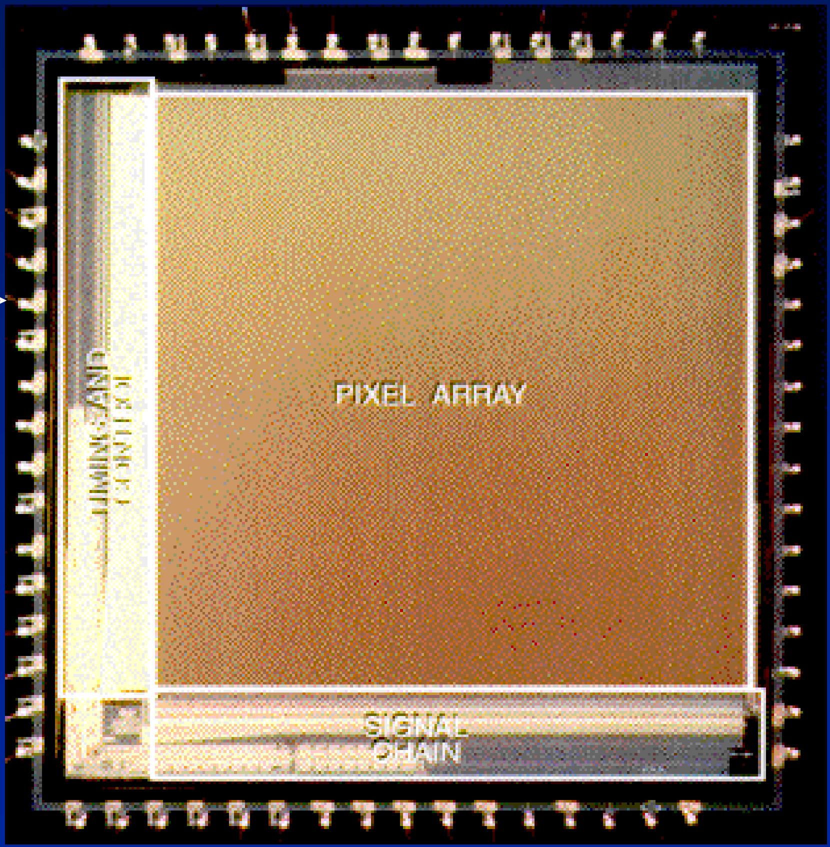
OUTLINE

- Quick look at state of the art
- Application drivers
- Historical perspective
- Modern CMOS image sensor pixels
- Integration of electronics
- Camera-on-a-chip and smart sensors

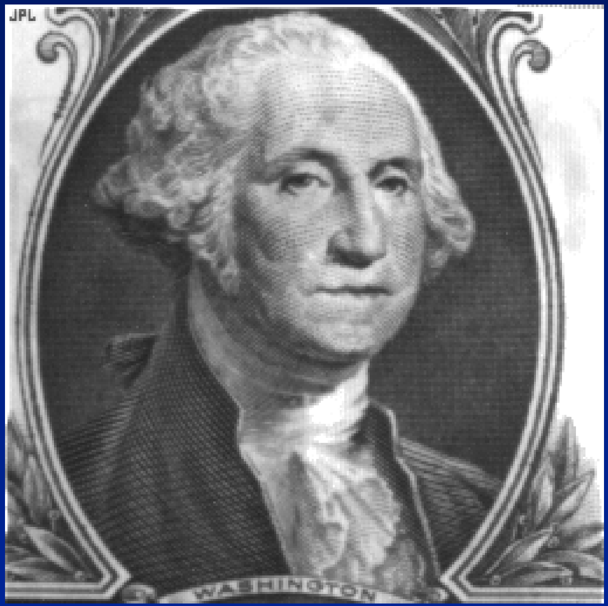
256x256 CMOS APS
With on-Chip Timing and Control Circuits

Clock

+5V

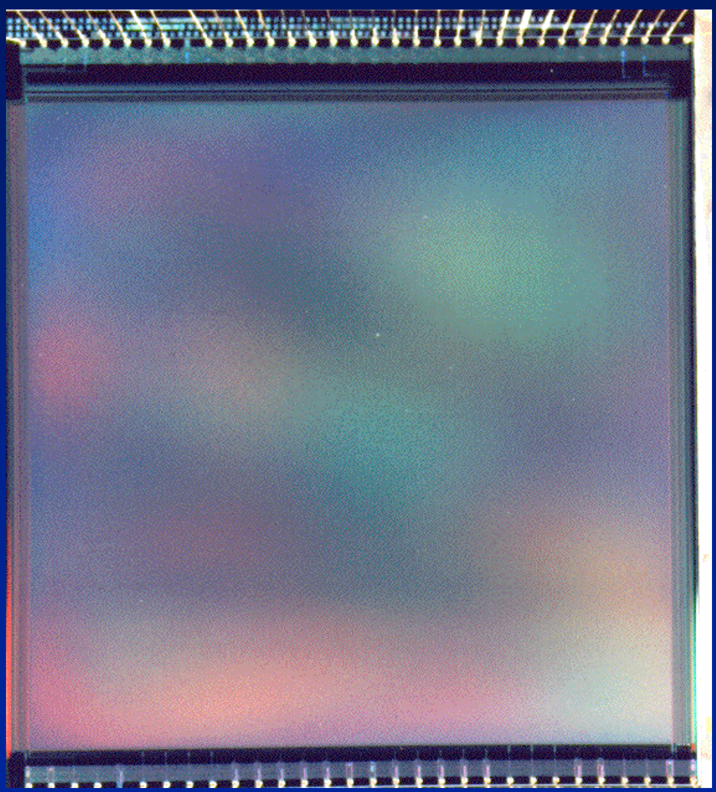


Analog

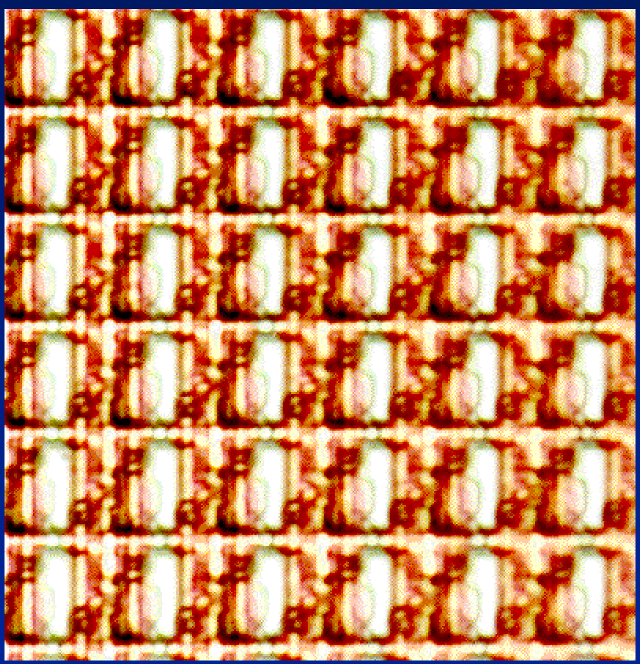


Nixon and Fossum, 1995

AT&T/JPL 1024 x 1024 CMOS APS



Chip



Closeup of pixels

Dickinson, Ackland, Azadet, Inglis, Mendis, Jones and Fossum 1995

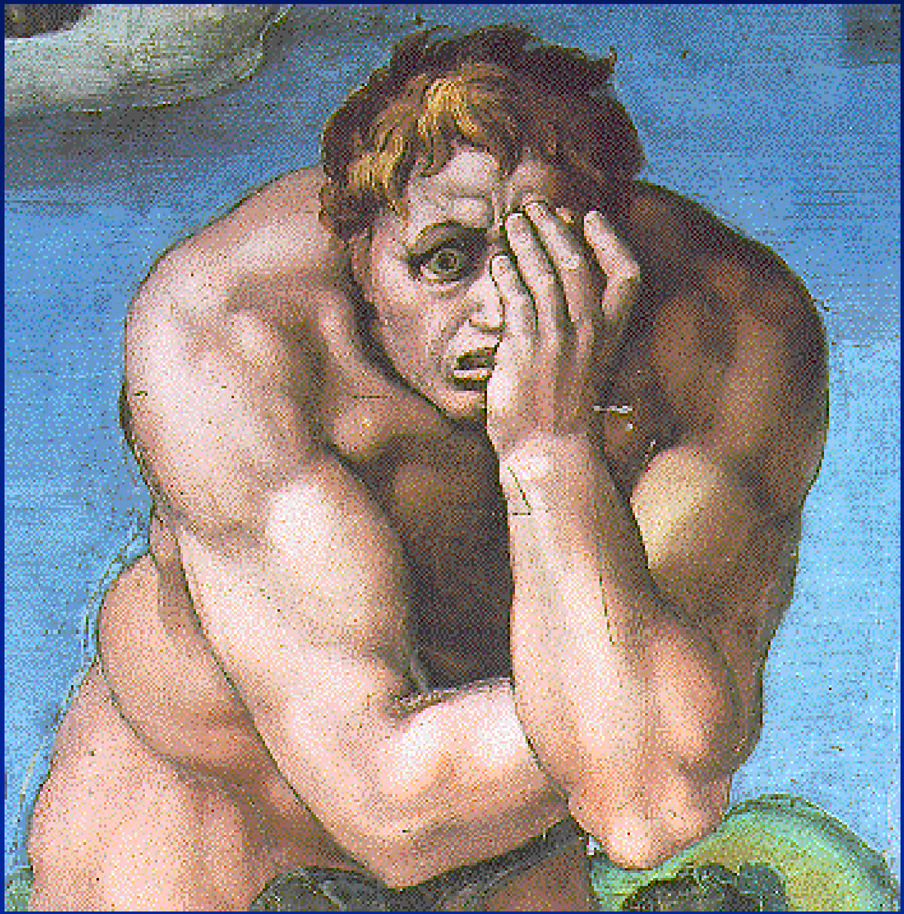
Historical Perspective on Image Capture

A long long time ago. . .

- Cave painting from 12,000 years ago

A few hundred years ago. . .

- Capturing images with paint
- Tormented soul from Michelangelo’s Last Judgment (1541)



Film Photography

1960’s Solid-State Image Capture

- 1963 Morrison - Honeywell
  - » Light spot position “computational” sensor
- 1964 Horton, et al. - IBM
  - » The “scanistor”
- 1966 Schuster & Strull - Westinghouse
  - » 50 x 50 element phototransistor array
- 1967 Weckler - Fairchild
  - » Charge integration on a floating pn junction

1960's Solid-State Image Capture

- 1967 Weimer, et al. - RCA
  - » 180x180 TFT element self-scanned sensor
  - » Battery powered, wireless camera
- 1968 Dyck & Weckler - Fairchild
  - » "Passive pixel" photodiode array ("reticon")
  - » 100 x 100 element array

1960’s Solid-State Image Capture

- 1968 Noble - Plessey
  - » Passive pixel photodiode array
  - » On-chip charge integrating amplifier
  - » Buried photodiode structure
  - » Source-follower buffer in pixel
- Birth of active pixel photodiode array

JPL

1970's Solid-State Image Capture

- 1970 Boyle, Smith, Amelio, Tompsett
  AT&T Bell Labs
  - » Charge-coupled semiconductor devices
- Birth of the CCD
- Almost the end of MOS image sensors

CCDs Were Better

- Smaller pixel sizes (3 electrodes/pixel)
- Lower readout noise
- No fixed pattern noise
- Low on-chip power dissipation
- Interesting device physics

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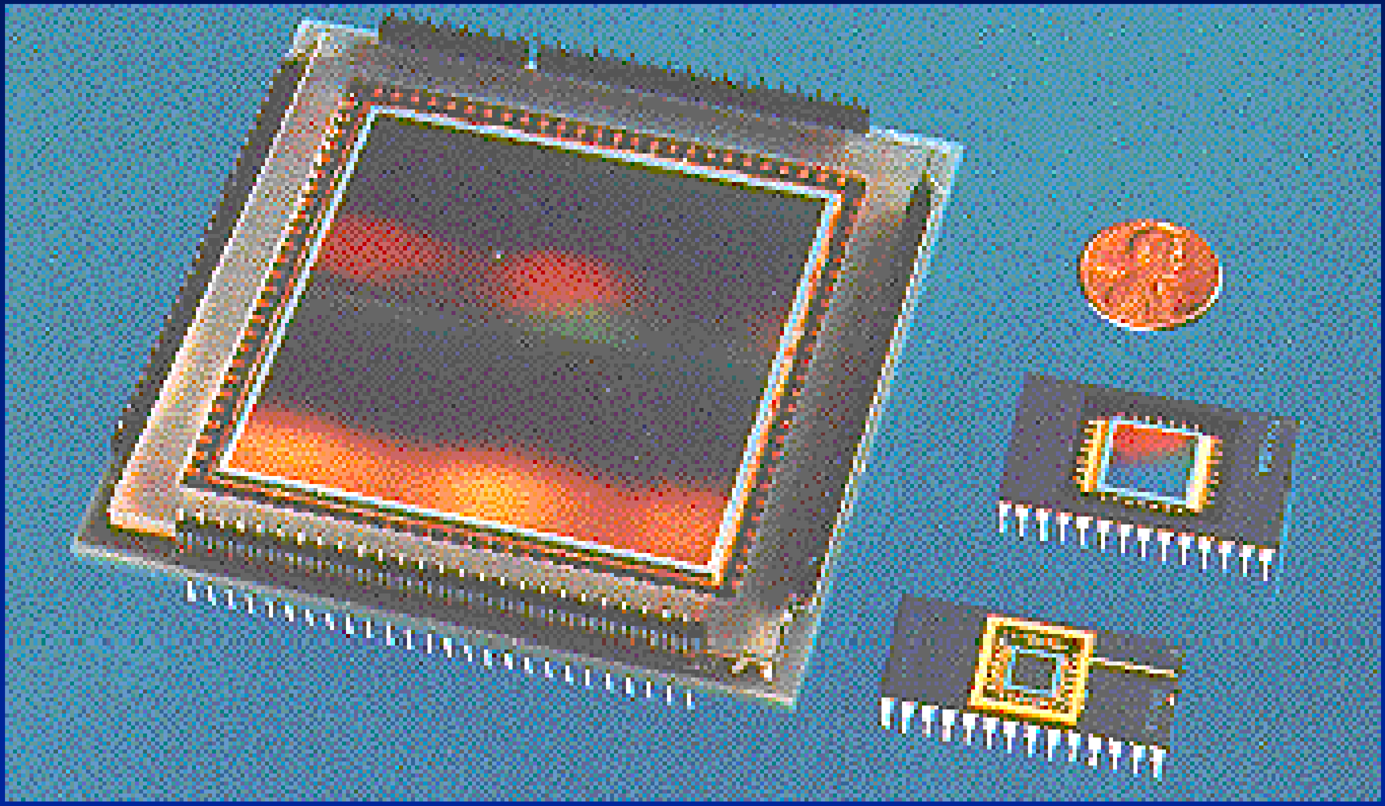
CCDs Are a Mature Technology



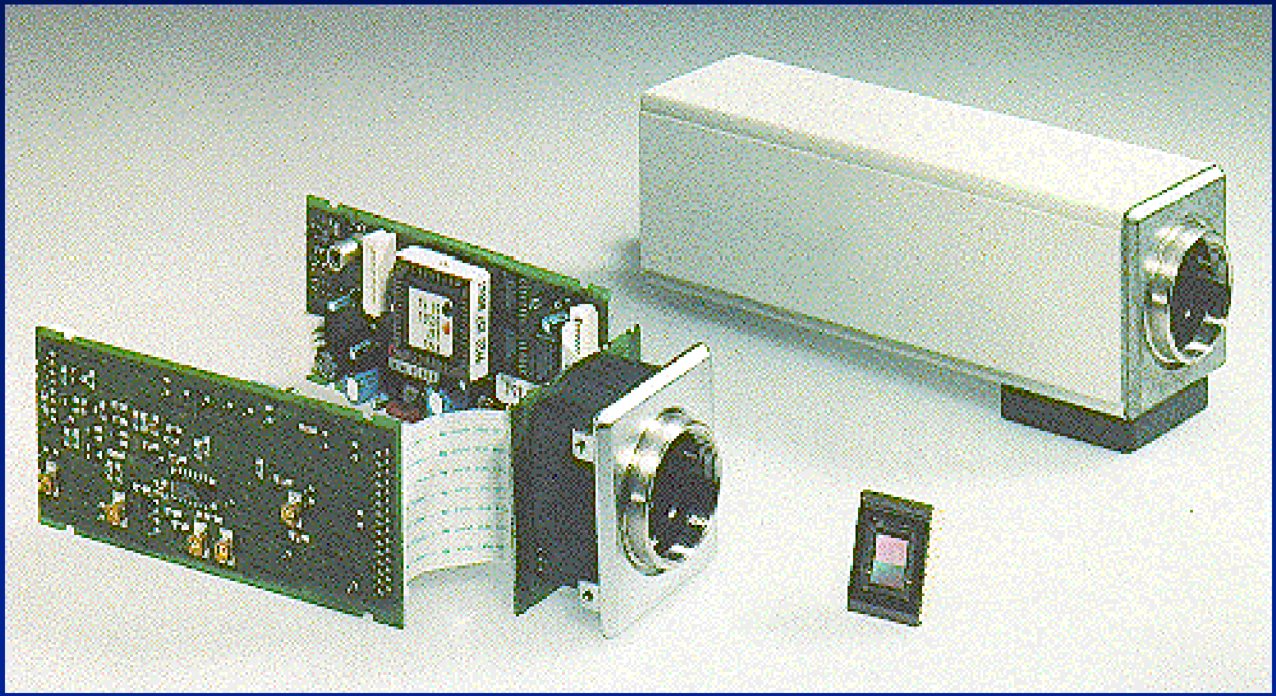
- DALSA 25 Mpixel sensor

- HDTV image
- HST image

CCDs Have Limitations

- Requires high charge transfer efficiency
  - » Special fabrication process
  - » Large voltage swings, different voltage levels
  - » Radiation "soft" in space environment
- Difficult to integrate on-chip timing, control, drive and signal chain electronics
- Serial access to image data
- System power in 1-10 Watt range

Total CCD Camera Power is High



- CCD imaging systems require many off-chip components

- Connectrix camera
- Connectrix boards

1970’s and 1980’s

- Very little published activity on MOS imagers
- Hitachi, Matsushita, Reticon continued development of passive pixel MOS imager
- NHK/Olympus developed photodiode type APS
- Caltech develops retina-like sensors

CMOS Image Sensors

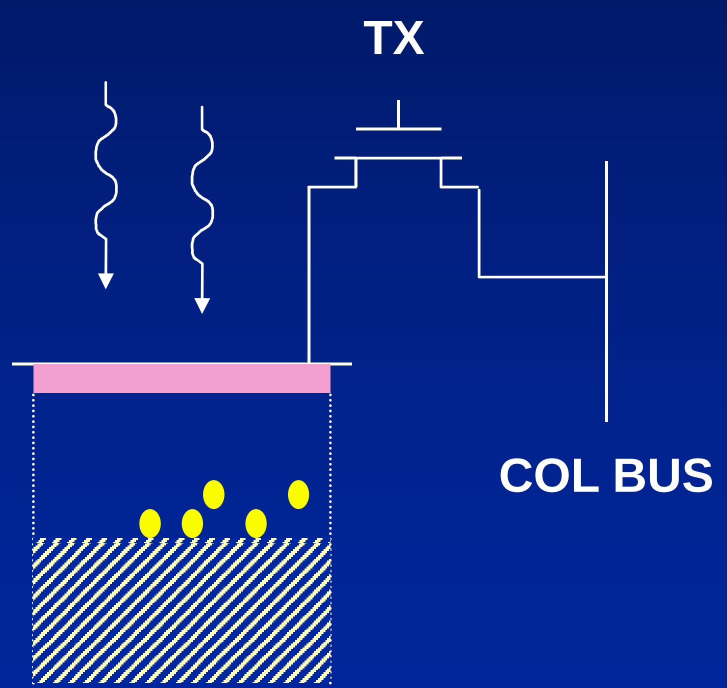
How Do They Work?

CMOS Image Sensors

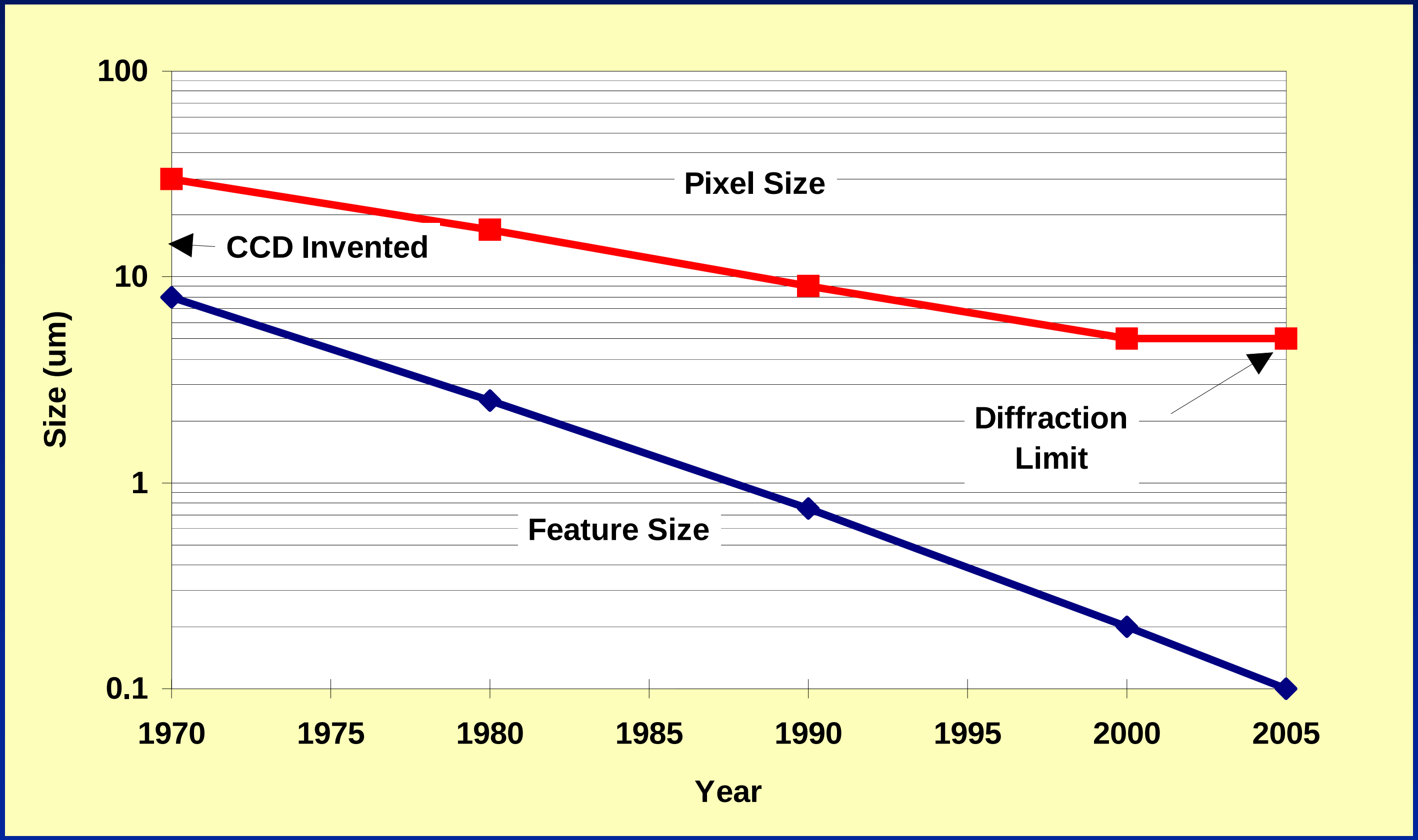
- Charge Integrating Sensors
  - » Passive Pixel Sensors
  - » Active Pixel Sensors
- Non-Integrating Sensors
  - » Retina-like Sensors
  - » Other functions

Passive Pixels

- 1 transistor per pixel
- 10 L scaling - small pixels (10 μm pixel needs 1.0 μm process)
- Great QE
- Poor noise (250 e- rms)
- Poor scaling for large formats
- Poor scaling for fast readout



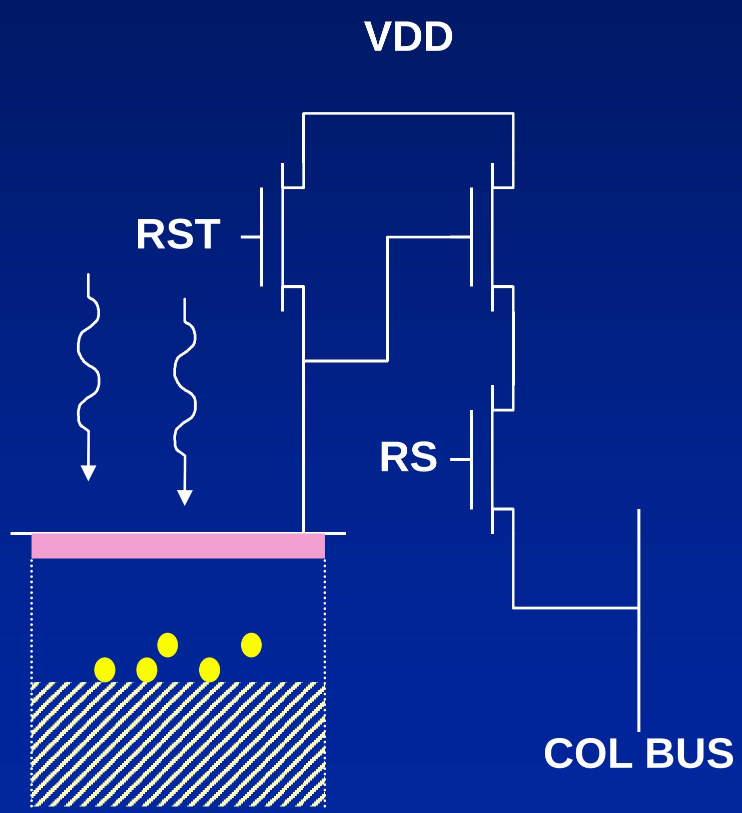
Evolution of Feature Size



- Enough space to put amplifier into each pixel.

Photodiode Active Pixel

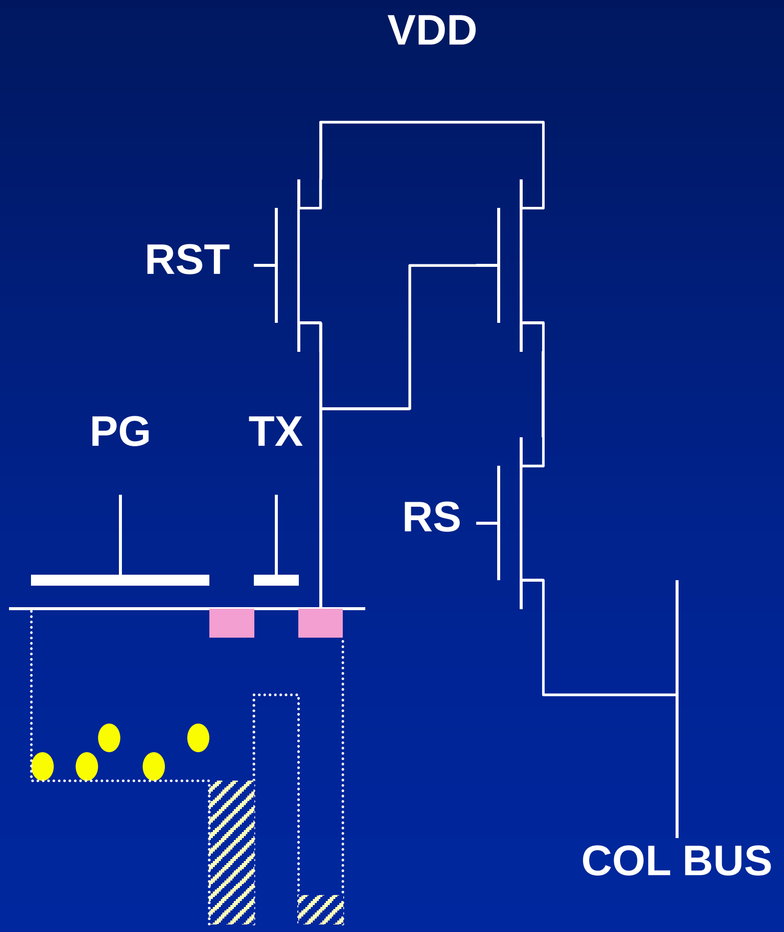
- 3 transistors per pixel
- 15 L scaling (10 μm pixel needs 0.7 μm process)
- Great QE
- OK noise (50-100 e- rms)
- Good scaling for large arrays
- Good scaling for fast arrays



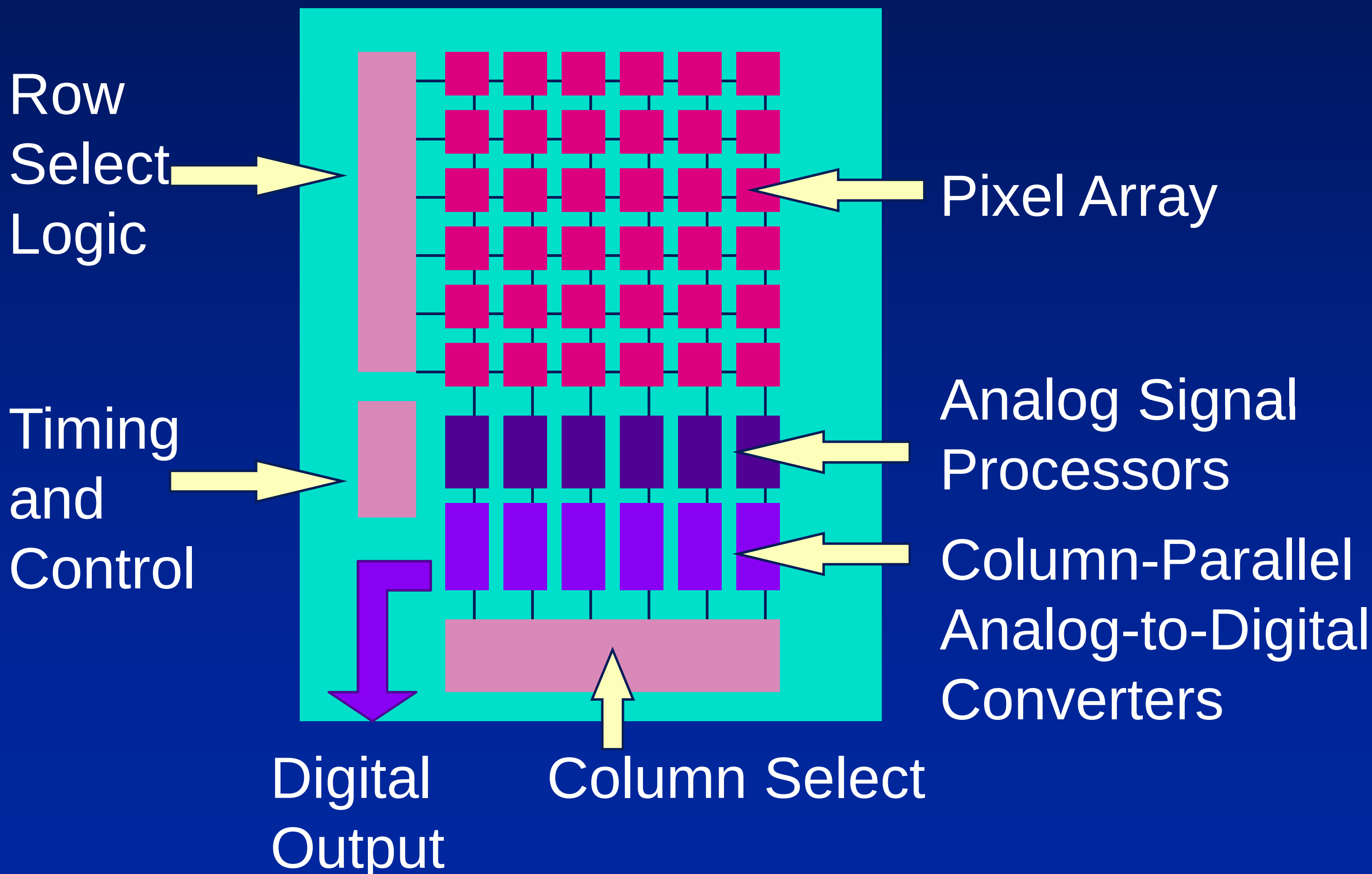
- NHK chip / closeup
- NHK cross section
- NHK high speed images

Photogate Active Pixel

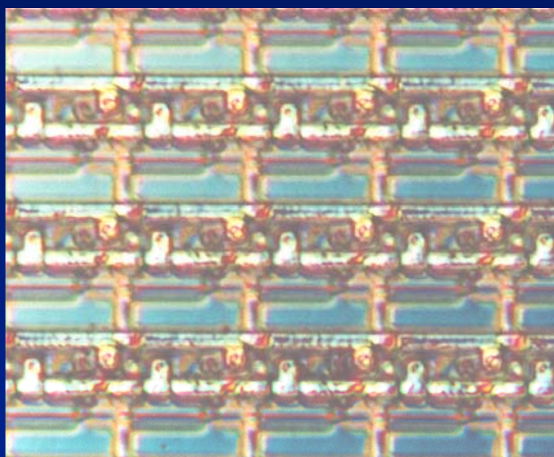
- 5 transistor pixel
- 20 L scaling (10 μm pixel needs 0.5 μm process)
- QE loss due to poly gate
- Great noise (10 e- rms)
- Good scaling for large arrays
- Good scaling for fast arrays

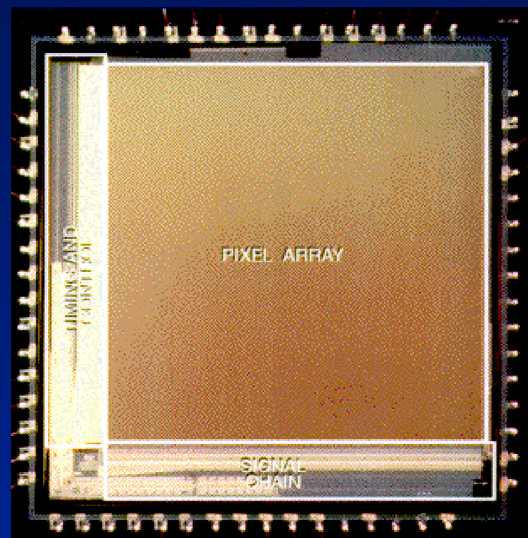


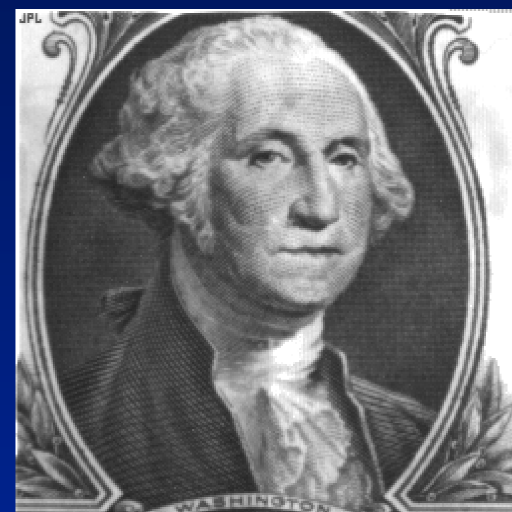
CMOS APS Architecture



JPL 256x256 CMOS APS







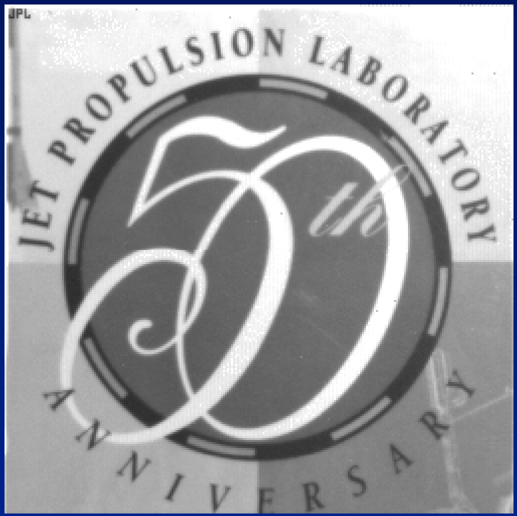
Pixel size:	20.4 μm
Pixel type:	photogate
Fill factor:	21%
Technology:	HP 1.2 μm n-well

Array size: 256x256
Timing, control, CDS
FPN suppression
Motion detection
Window readout
Program. integration time

Conv. Gain:	10.6 μV/e-
Saturation:	800 mV
Noise:	13 e- rms
FPN:	0.15% sat
Dyn. range:	76 dB
Power:	3 mW

Motion Detection

Motion to left

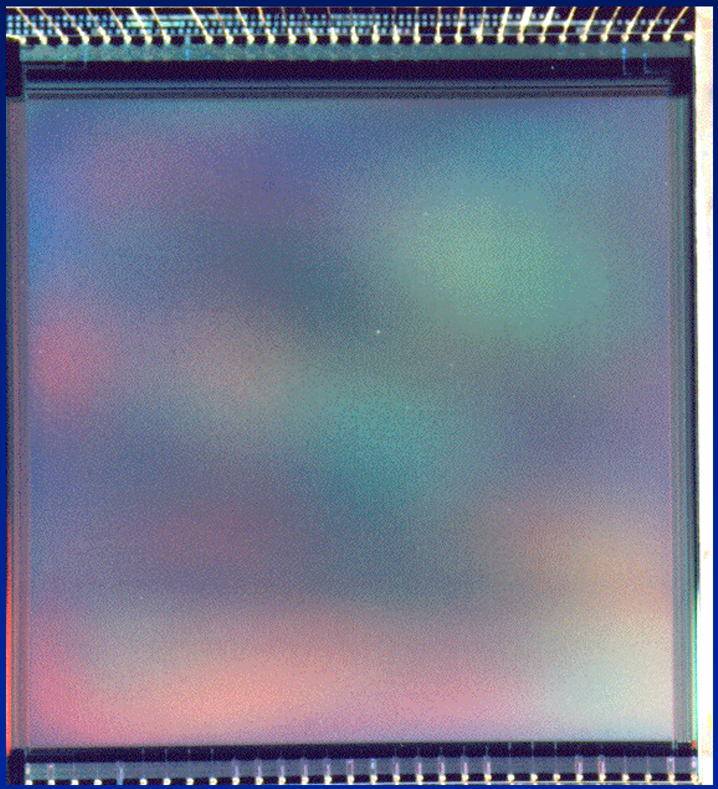


Normal image

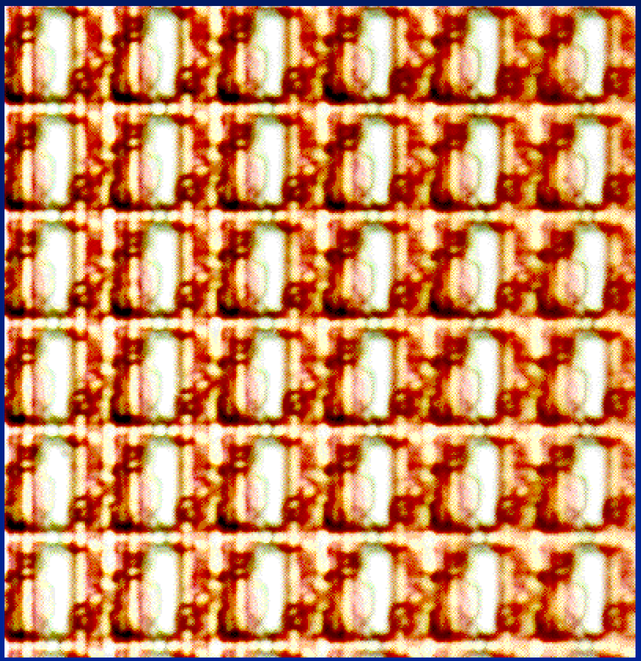
Motion to right

- Use floating diffusion as analog frame memory
- No change to pixel design, just timing

AT&T/JPL 1024 x 1024 CMOS APS



Chip

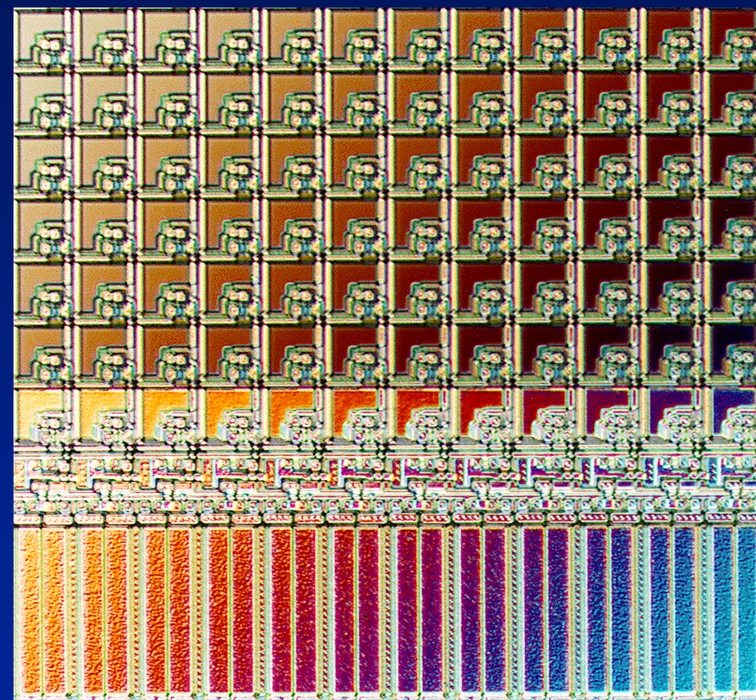


Closeup of pixels

Dickinson, Ackland, Azadet, Inglis, Mendis, Jones and Fossum 1995

Kodak/JPL PPD CMOS APS

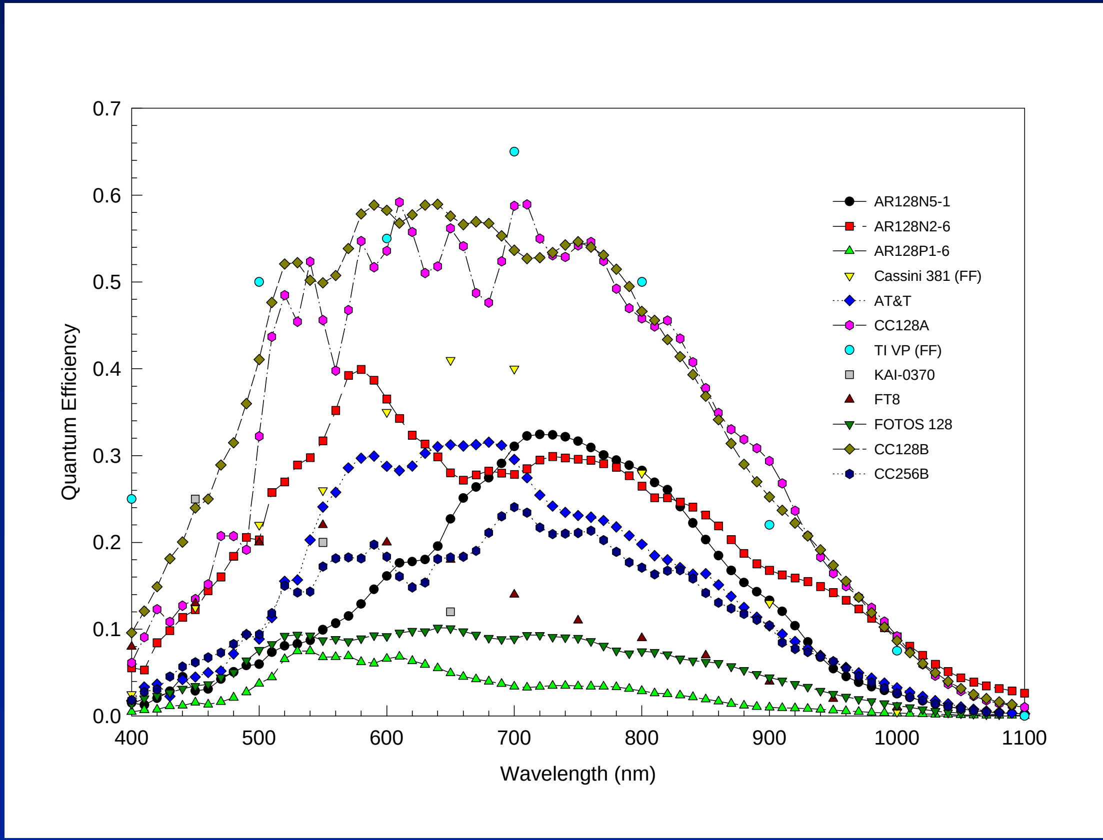
- Pinned photodiode CMOS APS
- No poly obscuration
- Good blue response
- Lower dark current
- 256 x256 element sensor



Pinned photodiode (PPD) APS pixels

P. Lee, R. Gee, M. Guidash, T. Lee, and E. Fossum, 1995

Quantum Efficiency



- QE competitive with CCDs

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CMOS APS Low Power Advantage

- Single 5V supply operation (or 3.3 V)
- Low capacitance on-chip loads
- Pixel amplifier activated only for readout
- Column-parallel signal chains operate at low frequency and low current bias (<10 μA)
- Digital output simplifies off-chip drivers
- Total chip power 10-50 mW

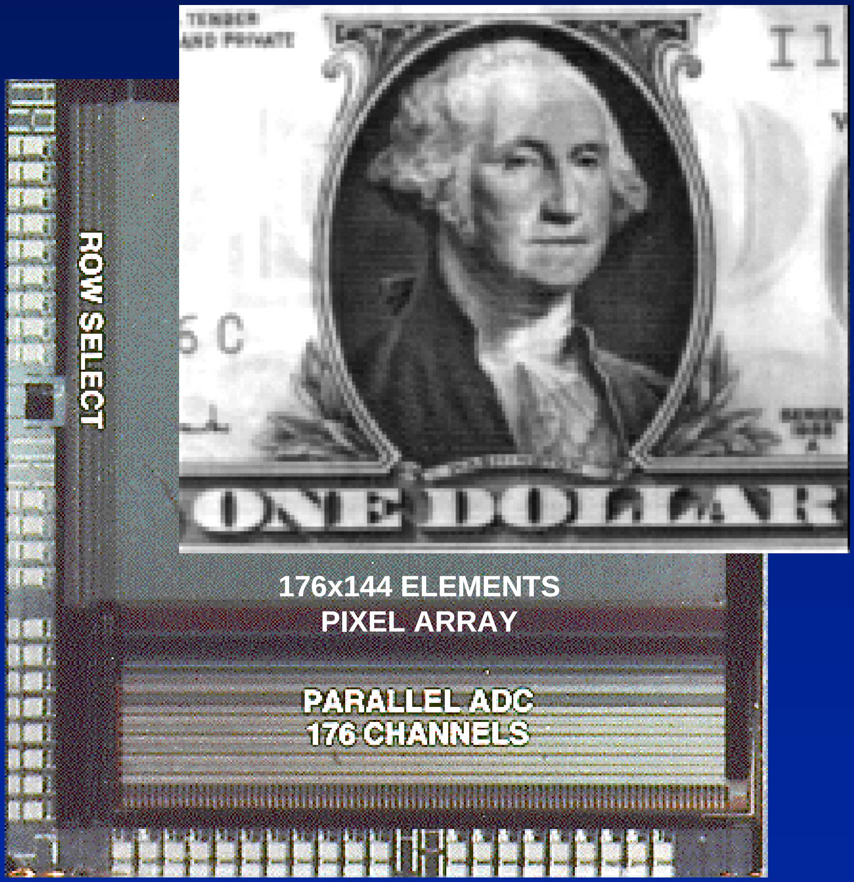
CMOS Image Sensors

On-Chip Functionality

CMOS Functionality Advantage

- On-chip timing and control circuits
- On-chip analog signal processing
  - » Correlated double sampling
  - » Fixed pattern noise suppression
  - » Local neighborhood image processing
  - » Compression preprocessing
- On-chip analog-to-digital conversion
- On-chip DSP and digital sensor control

JPL/AT&T Digital CMOS APS



- 176x144 elements
- 20 μm pixel pitch
- Single-slope ADC per column
- 176 ADCs per chip
- 8 bit resolution
- 35 mW at 30 Hz
- 3.5 volt supply

Mendis, Inglis, Dickinson, and Fossum 1995

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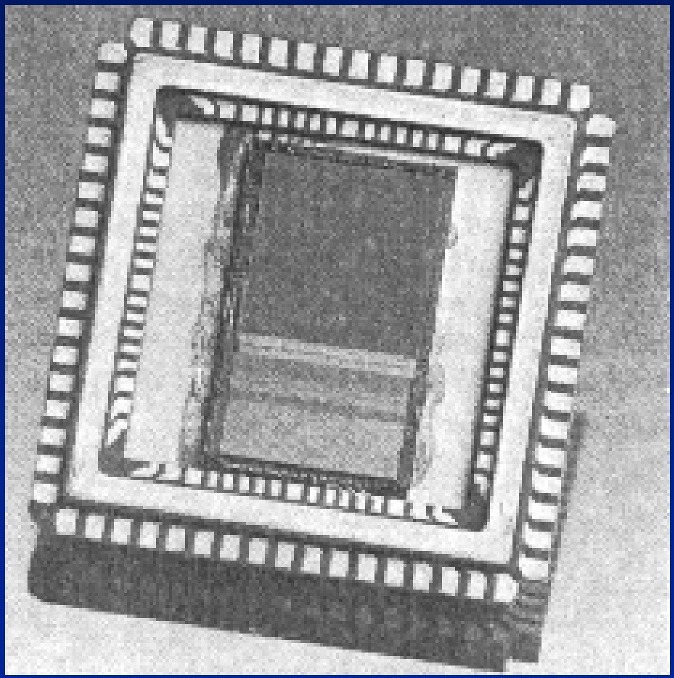
CMOS Sensor and Image Processor



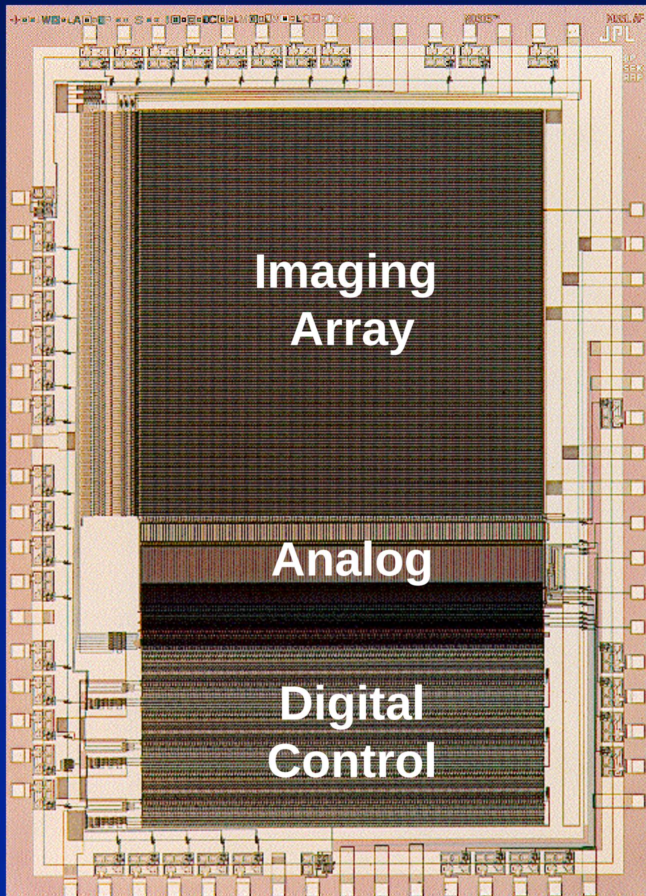
IVP's MAPP 2200

- 256x256 element
- Passive pixel
- 32 μm pitch
- On-chip ADC
- Bit-slice image processor
- 150 mm^2 chip size

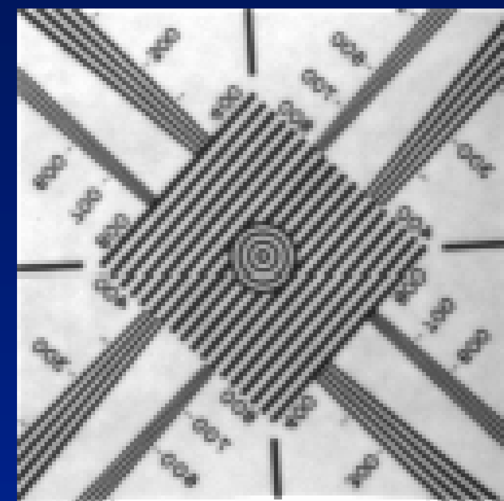
Forchheimer, Ingelhag, and Jansson 1992

- VLSI vision burglar alarm/modem

JPL Multiresolution Sensor



Process:	HP 1.2 um n-well CMOS
Pixel pitch:	24 um
No. pixels:	128 x 128
Pwr suppy:	5 volts
Saturation:	1200 mV
Conv. gain:	8 uV/e-
Noise:	116 uV rms 15 e- rms
Dynamic Range:	80 dB
FPN:	<3 mV p-p <2.5 %
Power: at 30Hz	< 5 mW



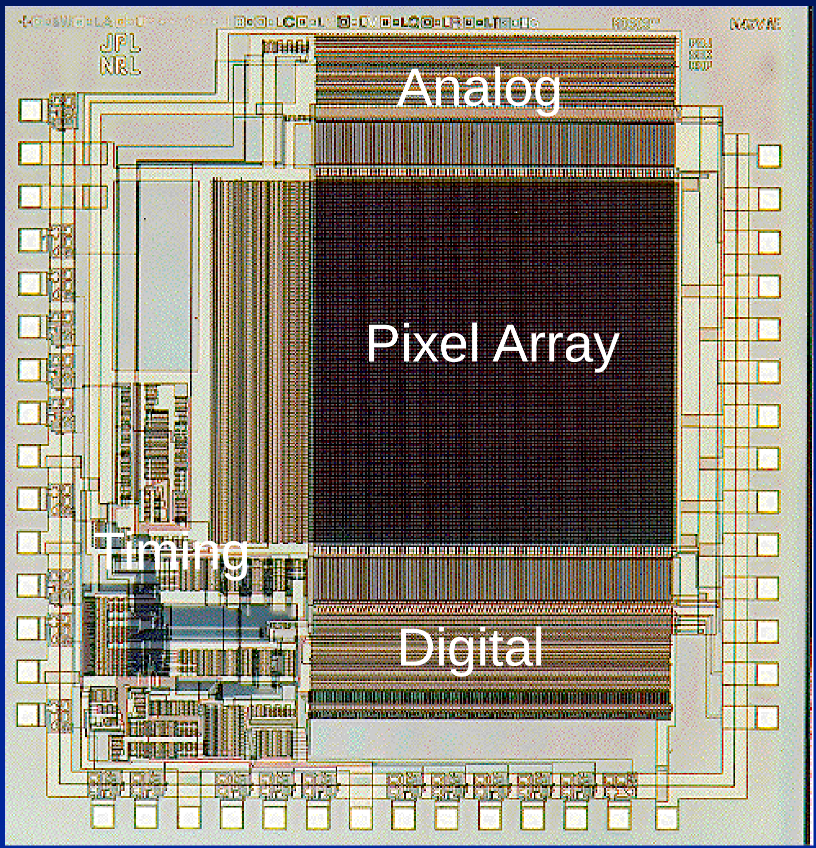
Full resolution image

4x4 Averaged image (left)

1/4 Subsampled image (right)

Kemeny, Panicacci, Pain, Matthies, Fossum 1995

JPL High Speed CMOS APS



- 128x128 elements
- Photodiode active pixels
- 16 μm pixel pitch
- Analog output (top)
- 1-bit Digital output (bottom)
- 8,000 frames per second
- On-chip timing and control

Panicacci, Jones, Fossum 1994

JPL High Speed CMOS APS

- Analog Image

- Binary Image

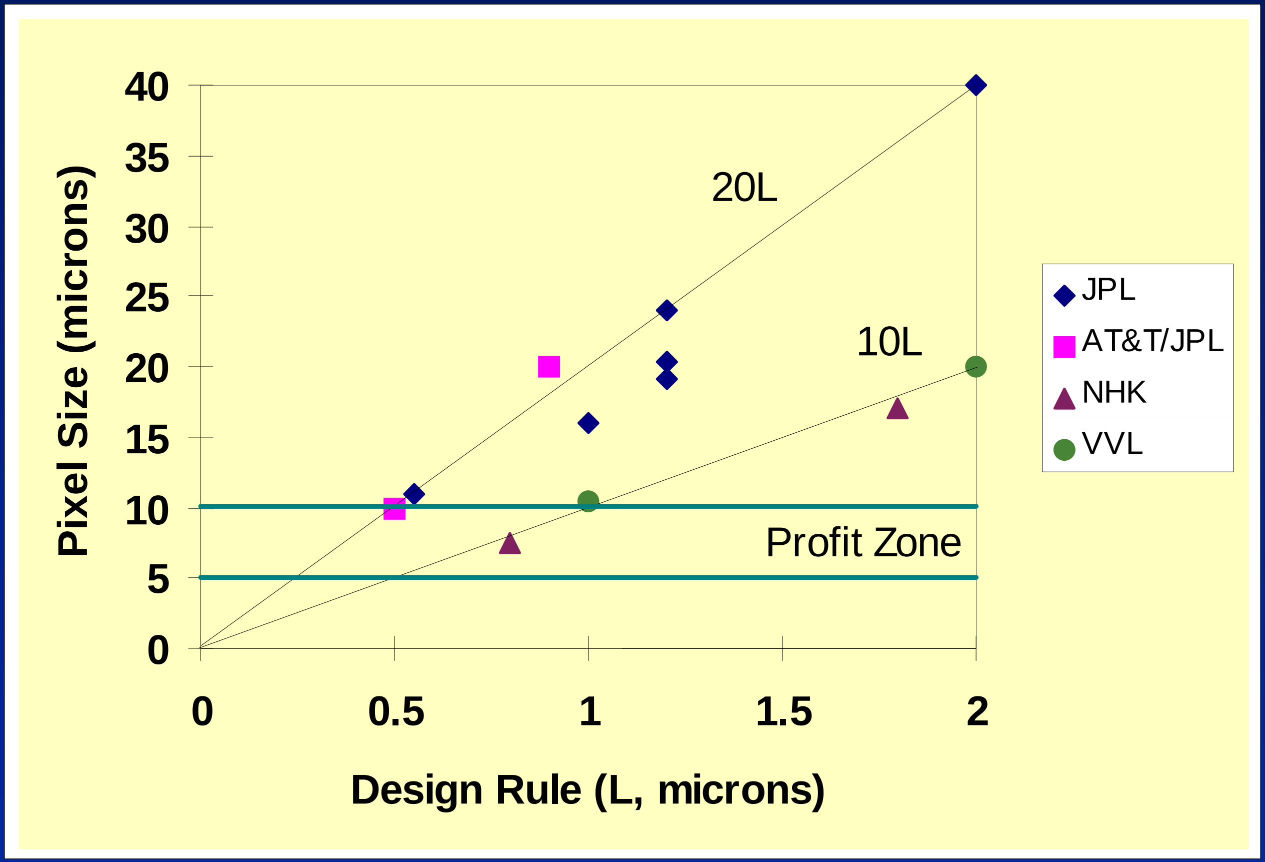
Pixel-Level Functionality

- Stanford University - Gamal
  - » Pixel level oversampled ADC
- University of Tokyo - Aizawa
  - » Pixel level compression logic
- Carnegie-Mellon University - Kanade
  - » Pixel level pixel sorting logic
- California Institute of Technology - Mead
  - » Retina-like functions

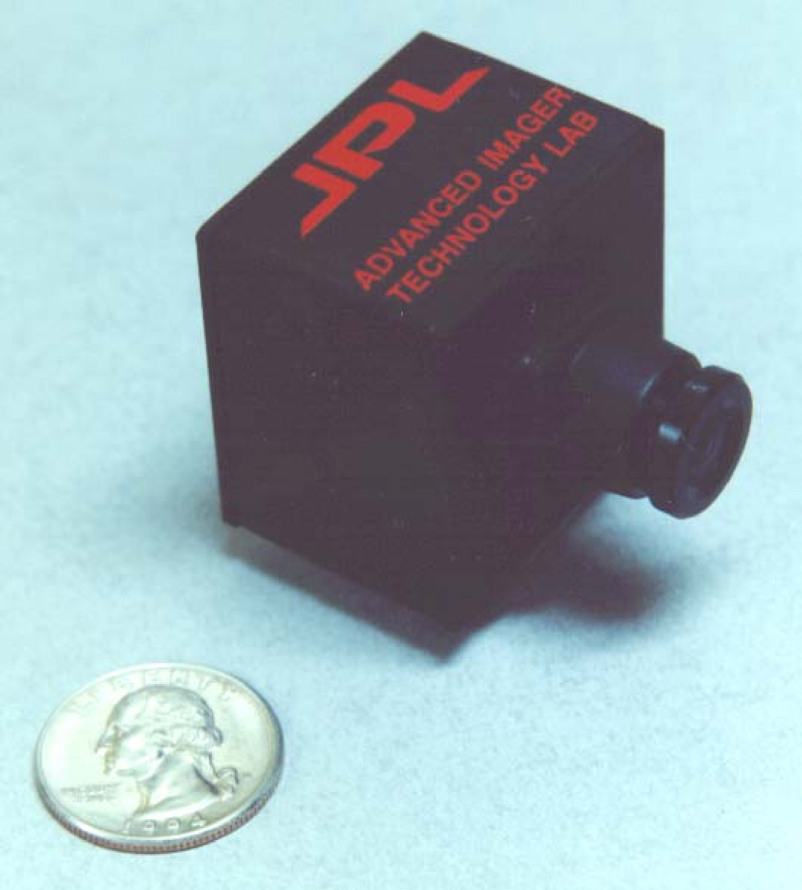
Fabrication Issues

- Opaque silicides - need silicide mask
- Dark current - more sensitive than memory devices
- Collection depth - SOI is a problem
- Capacitor implants are nice
- Low voltages - reduced amplifier swing and dynamic range
- Low 1/f noise transistors help

Scaling Trend

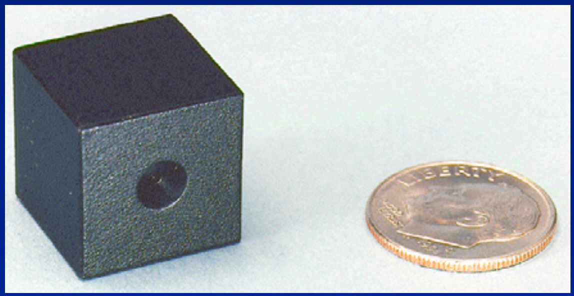


Miniaturized CMOS APS Cameras



Technology demonstration camera

- 256x256 CMOS APS Camera
- Full digital interface
- Electronic pan and zoom



Next demonstration camera

- On-chip ADC
- Automatic exposure control

Conclusions

- CMOS APS has achieved "respectability" in performance
- CMOS image sensors offer significant advantages for:
  - » System miniaturization
  - » Low power portable applications
  - » Functionality vs. cost
- Expect significant growth in market share and creation of new markets

Acknowledgments

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- Advanced Research Projects Agency - Low Power Electronics Program