FUTURE PROSPECTS FOR CMOS ACTIVE PIXEL SENSORS

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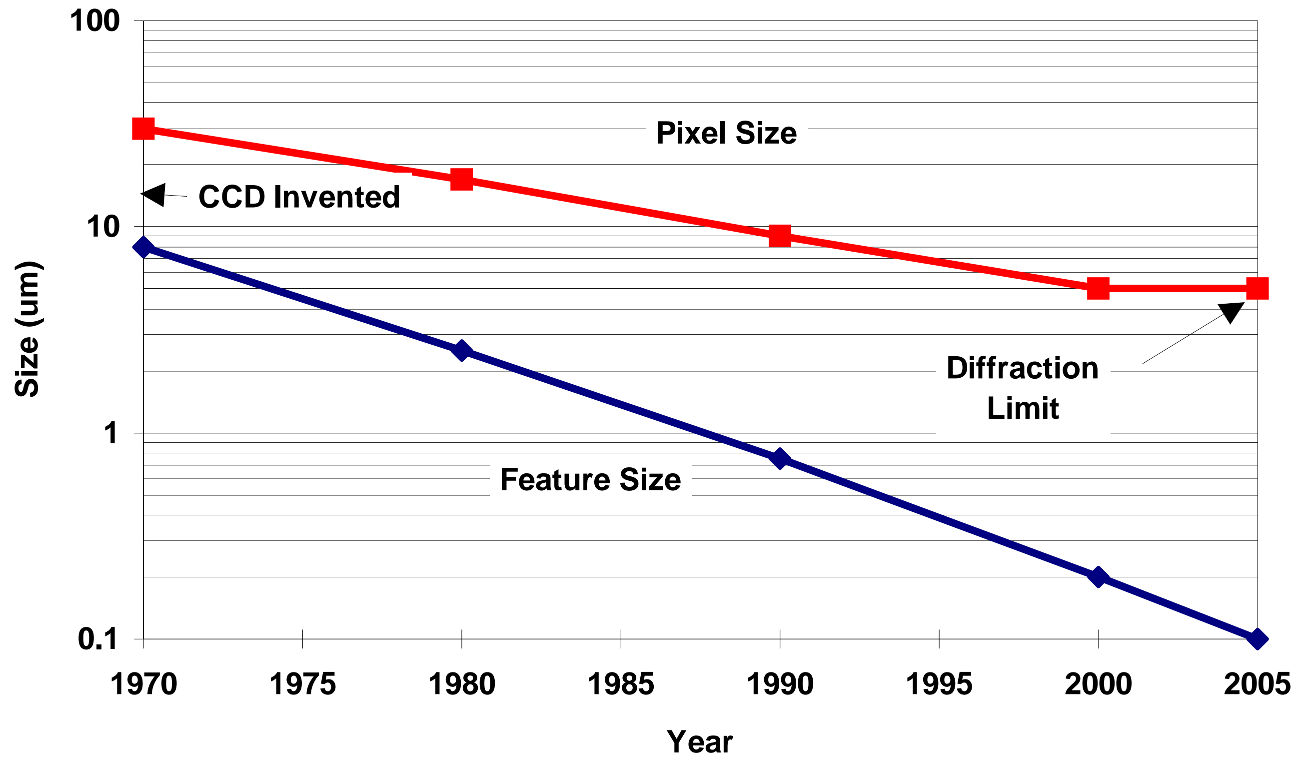
CMOS APS OVERVIEW

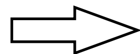
- Second generation solid-state image sensor technology
- Retains nearly all the performance of a CCD
- Unique advantages of CMOS APS:
  - Ultra low power system, >100x less than CCD system
  - Highly integrated on-chip electronics reduces component count
  - Commercial CMOS technology leverage
  - Don’t need a dedicated CCD fab line to make sensors ($$)
  - Random access and window-of-interest pixel readout
  - Standard 5 volt (or 3.3 volt) operation
  - Faster readout
  - Radiation hard
  - Larger format arrays
- Strong commercial, biomedical, defense, and space applications

PROBLEMS WITH CCDs

- Charge-coupled devices (CCDs) invented around 1970.
  - Uses repeated lateral charge transfer to readout image.
- Need for nearly perfect charge transfer efficiency is Achilles' heel.
  - Requires specialized fabrication process so not 100% CMOS compatible.
  - Requires numerous different voltages to achieve good performance
  - Susceptible to bulk radiation damage so radiation "soft"
- CCDs are large capacitance devices so on-chip drive circuits difficult to implement.
  - Excessive power dissipation
  - Hot electron photon emission
  - Process incompatibility
- On-chip signal processing (e.g. ADC) difficult to implement in CCD technology.

EVOLUTION OF MICROELECTRONICS FEATURE SIZE





Enough space to put amplifier into each pixel.

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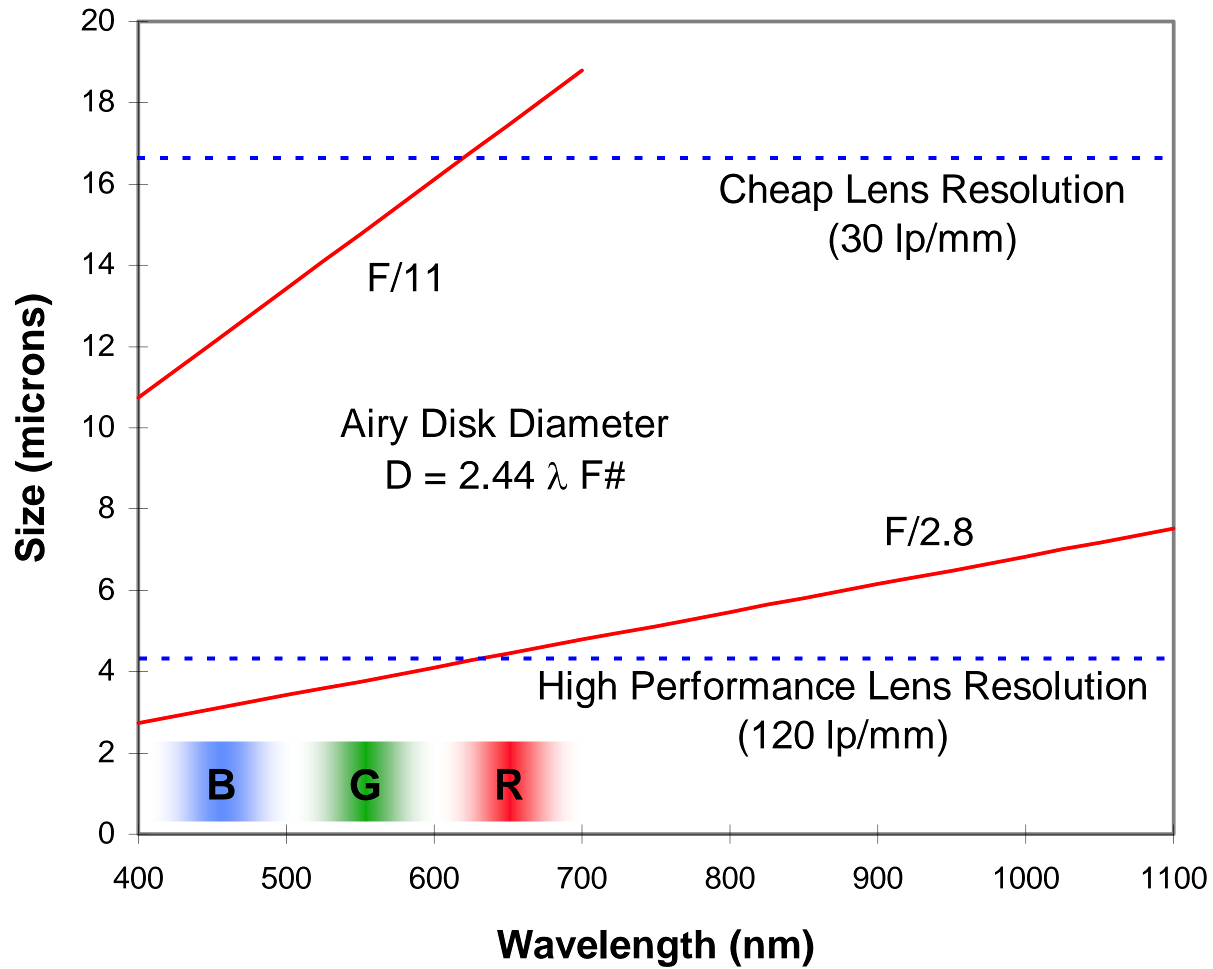
RESOLUTION LIMITS



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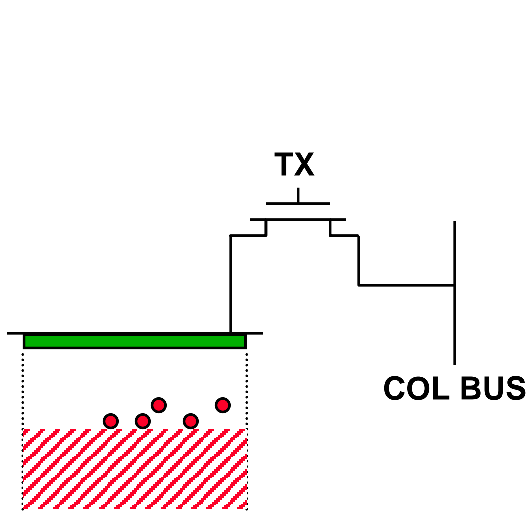
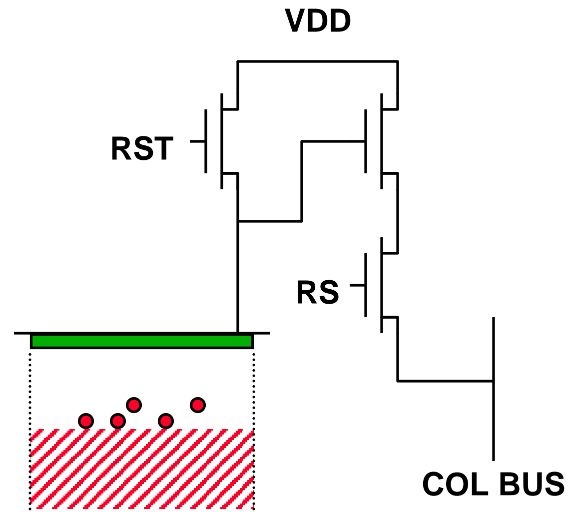
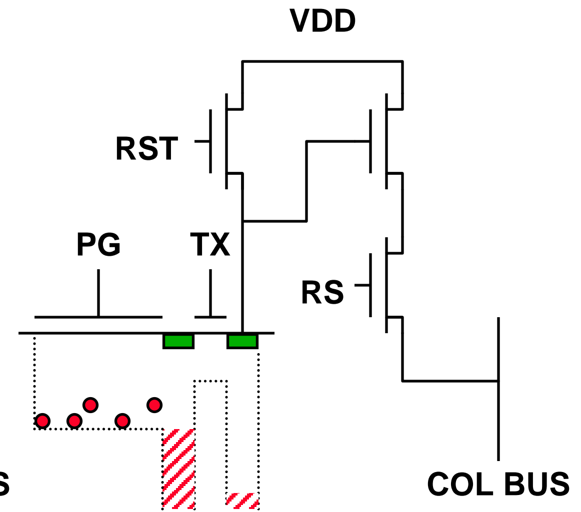
COMMON CMOS PIXELS







Passive Pixel

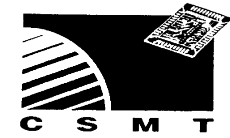
- 1 transistor pixel
- 10 L scaling
- Great QE
- Poor noise (250 e-)
- Poor large & fast scaling

Photodiode CMOS APS

- 3 transistor pixel
- 15 L scaling
- Great QE
- OK noise (50-100 e-)
- Good large & fast scaling

Photogate CMOS APS

- 5 transistor pixel
- 20 L scaling
- Good QE
- Great noise (15 e-)
- Good large & fast scaling



28x28

cc256

FOTOS

SXRS

JPL AT&T DIgital QCIF

AT&T 10 um CIF

JPL AT&T 1Kx1K

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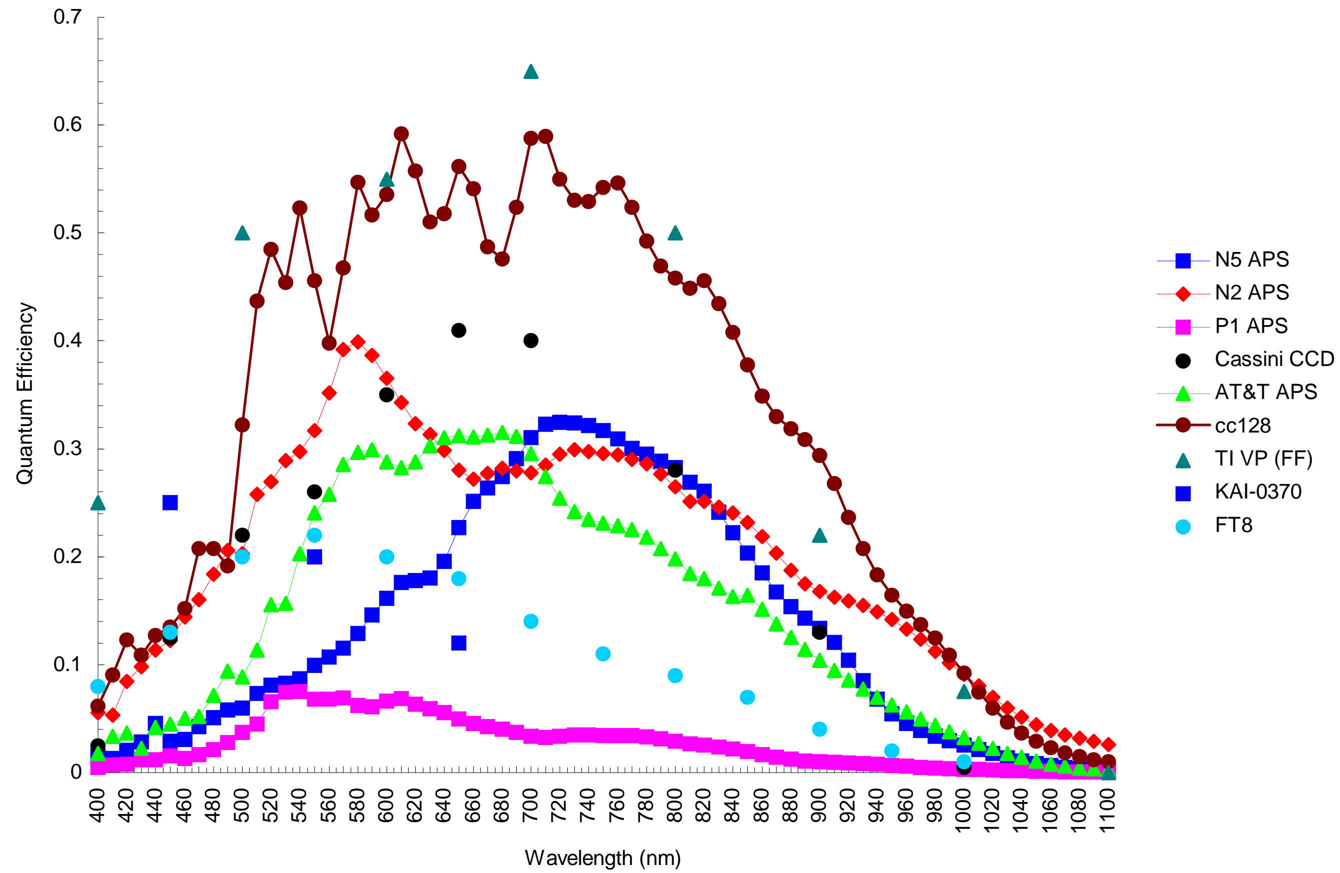
C S M T

APS and CCD Measured Quantum Efficiencies



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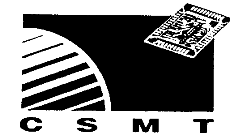
SCALING TREND IN CMOS APS



Pixel Size (microns)

40
35
30
25
20
15
10
5
0

20L
15L
10L
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NHK

0
0.5
1
1.5
2

Drawn Design Rule (L)

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PRINCIPAL DEVICE TECHNOLOGY CHARACTERISTICS

YEAR (1st DRAM shipment)	1980	1983	1986	1989	1992	1995
Minimum lithographic feature size (0.7x/gen) [μm]	2	1.5	1.0	0.7	0.5	0.35
Isolation	LOCOS	LOCOS	LOCOS	LOCOS	LOCOS	LOCOS, STI
Gate Oxide [nm]	41-71	29-50	20-35	14-24	10-17	7-12
Gate Electrode	n+poly	n+poly	n+poly silicide	n+poly silicide	n+poly n+/p+ silicide	n+/p+ silicide
Substrate doping [cm^{-3}]	10^{16}	$2x10^{16}$	$4x10^{16}$	$8x10^{16}$	$1.2x10^{17}$	$2.5x10^{17}$
Source/drain junction	abrupt	abrupt	LDD	LDD	LDD	LDD, S/D ext
Source/drain junction depth [μm]	0.5-0.6	0.45-0.55	0.5-0.5	0.35-0.45	0.3-0.4	0.2-0.3
Power supply [V]	5	5	5	5	5/3.3	3.3/2.5
Threshold voltage [V]	1.0	0.9	0.8	0.7	0.6	0.5
Threshold voltage variation [+/- mV, wafer-wafer]	170	125	80	75	70	60-70
DRAM bits/chip (4x/generation)	64K	256K	1M	4M	16M	64M
DRAM chip size (1.5x/generation) [mm^2]	27	40	60	90	130	190
DRAM cell size (0.4x/generation) [μm^2]	146	58	23	9.4	3.75	1.5
SRAM bits/chip (4x/generation)	16K	64K	256K	1M	4M	16M
SRAM chip size (1.5x/generation) [mm^2]	31	47	70	100	150	220
SRAM cell size (0.4x/generation) [μm^2]	781	313	125	50	20	8
CMOS APS pixel pitch (0.7x/generation, 20L) [μm]	40	28	20	14	10	7
CMOS APS image pixel size (0.5x/generation, 20L) [μm^2]	1600	800	400	200	100	50
CMOS APS fill factor	25	25	25	25	25	25
Imager format size (HDTV)					1”	
Imager format size (NTSC-TV)		1”		2/3”		1/3”

CONSEQUENCES OF TECHNOLOGY SCALING

QUANTUM EFFICIENCY

Silicide (polycide/salicide)

- Opaque layer used to reduce resistivity of poly and S/D junctions
- $CoSi_2$ less opaque than $TiSi_2$
- Used below L < 0.8 - 0.35 microns
- Mask for removal “not a big deal” (std. layer in some processes)
- Not used in DRAM processes
- Possibly useful as additional light shield

Fill factor

- Smaller L yields larger fill factor for given pixel pitch

CONSEQUENCES OF TECHNOLOGY SCALING

QUANTUM EFFICIENCY (cont.)

Carrier Collection Depth

- Depletion region shrinking
  - lower operating voltage
  - higher substrate doping concentrations
- Loss at p+ substrate/p-epi interface due to gettering at interface
- SOI thickness < 200 nm
- Retrograde wells retards collection from neutral region (built-in field)

Thinner Polysilicon

- 1.5 - 2.0 micron process, poly typically 400 nm thickness
- 0.5 micron process poly -> 200 nm thickness

CONSEQUENCES OF TECHNOLOGY SCALING

CROSSTALK

Isolation
- LOCOS --> Shallow Trench Isolation (STI)
  – not much effect - may actually be improvement:
  – less stress
  – more radiation hard
  – less dark current
- Deep trench possible (DRAM-like process)
- SOI eliminates all crosstalk (and most QE)

Shallower depletion regions
- Tend to increase longer wavelength crosstalk since more diffusion

Upper metal layers yield loose light shields

CONSEQUENCES OF TECHNOLOGY SCALING

DARK CURRENT

- “OFF” Currents increase
  - shorter length
  - lower threshold voltage
- Higher doping will increase pn junction leakage currents
- Better contamination control will lower dark current
- Gate oxide tunneling current not too important
  - current scales with electric field (i.e. signal charge)
  - tunneling current looks mostly like majority carrier current
  - minority carrier tunneling will lead to “anti-blooming effect”
- Gate-induced leakage current a concern in higher doped junctions
- Hot carrier effects not expected to increase due to voltage scaling

CONSEQUENCES OF TECHNOLOGY SCALING

DYNAMIC RANGE

- Define as ratio of saturation signal to noise floor

- Transistor noise
  - 1/f noise, white noise increases for smaller area
  - noise reduces for lower voltages
- Reduced capacitances will increase conversion gain (uV/e-)
- Reduced operating voltage will decrease saturation signal
- Reduced threshold voltages will increase saturation signal
- Well capacity of PG devices increase with decreased gate oxide thickness

- Net effect may result in constant dynamic range

CONSEQUENCES OF TECHNOLOGY SCALING

READOUT SPEED

- Dominated by parasitic capacitances and transistor sizing
- Wiring capacitance per unit length remains about constant
- Smaller pixel size, same no. elements, speed increases

DIE SIZE / ARRAY SIZE

- DRAM trend will drive toward larger die sizes
- Array size can increase like DRAM trend
- 17 - 20 mm standard (4Kx4K for 5 micron pixel)
- Larger tools will become available (e.g. 48 mm Canon tool)
- CMOS APS amenable to e-beam wafer scale integration
- CMOS APS amenable to stitching strategies for wafer scale integration

CONSEQUENCES OF TECHNOLOGY SCALING

SUMMARY

QUANTUM EFFICIENCY:	Looks OK until SOI
CROSSTALK:	Increases but no show stopper
DARK CURRENT:	Some increase possible
DYNAMIC RANGE:	Should remain nearly constant
READOUT SPEED:	Faster readout for fixed array size
DIE SIZE/ARRAY SIZE:	Smaller die for fixed array size Larger arrays possible

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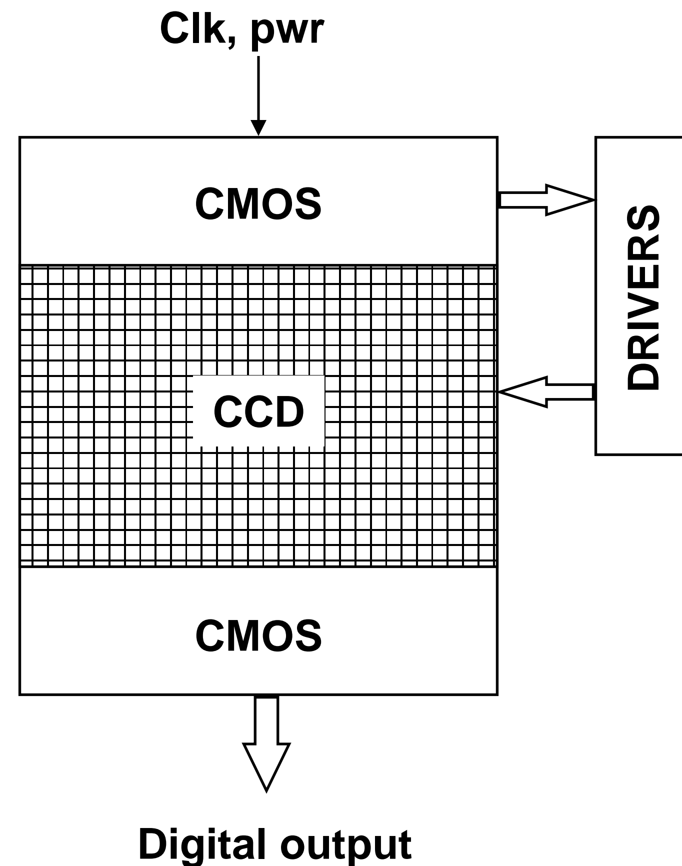
COMPETITIVE CCDs

Expect increased competition from CCDs:

- Reduced parasitic capacitances --> lower power
- Lower voltage operation
- Higher fill factor using smaller design rules
- Increasing use of CMOS/CCD combined process
  - On-chip timing and control
  - On-chip drivers using BiCMOS (?)
  - On-chip signal chain, ADC
- Reduced cost for Mpixel sensors



APS VS. CCD

PARAMETER	APS	CCD
FORMAT	Wafer scale (8”)	8096x8096 (2”)
VOLTAGE	3.3 VOLTS	+/-20.0 VOLTS
SYS. POWER	0.05 W	5 W
ON-CHIP TIMING	yes	none
WINDOW READOUT	yes	none
ON CHIP ADC RES.	10-12 bits	none
PIXEL SIZE	5 micron	5 micron
PROCESS	0.25 um CMOS	0.6 um CCD
FILL FACTOR	25%	25%
CONVERSION GAIN	10 uV/e-	10 uV/e-
SATURATION	100,000 e-	50,000 e-
INPUT REF. NOISE	15 e-	10 e-
DYNAMIC RANGE	74 dB	75 dB
PEAK QE	30%	25%

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DISCUSSION