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ACTIVE PIXEL SENSORS
VS.
CHARGE-COUPLED DEVICES

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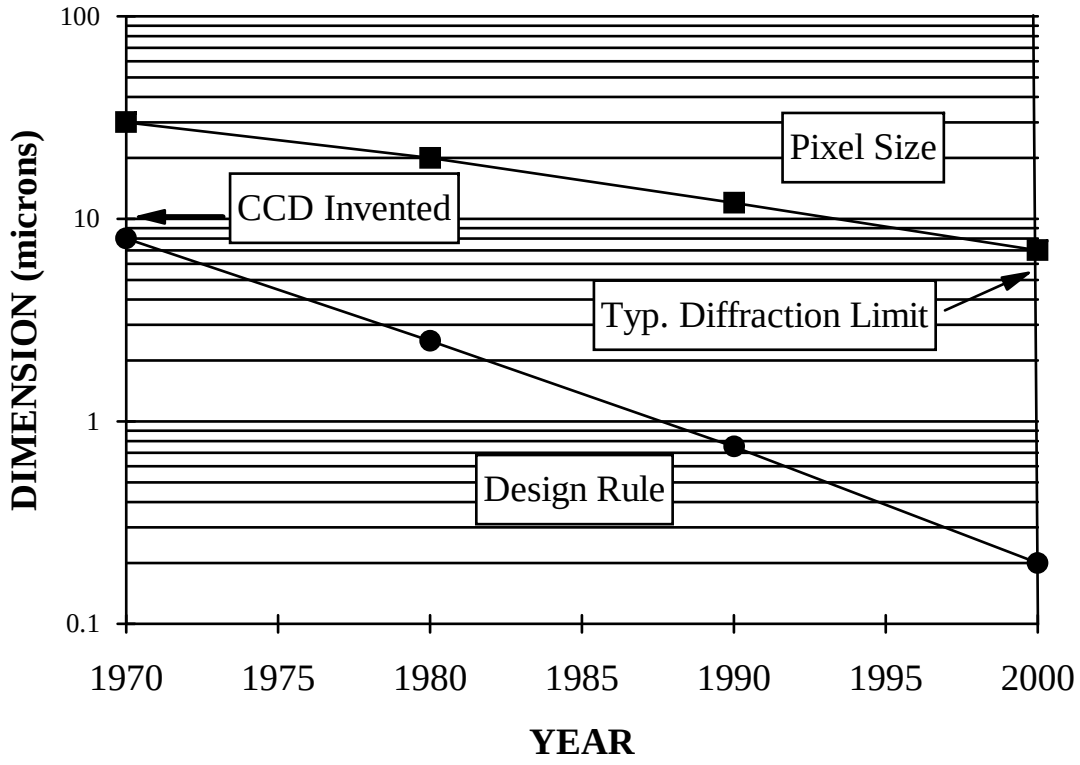
OUTLINE

1. A Brief History of CCDs
2. Active Pixel Sensors
3. State of the Art
4. Comparison of APS vs. CCD Technology
5. Speculation
6. Summary

EVOLUTION OF

PHOTOLITHOGRAPHIC FEATURE SIZE VS. PIXEL SIZE



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TYPICAL CCD PERFORMANCE

	COMMERCIAL	SCIENTIFIC
Array Size	1920x1036	2048x2048
CTE	>0.99997	>0.999995
Architecture	FIT 1"	Full Frame
Smear	-110 dB	n/a
Full Well	120,000	40,000
Noise	20-30 e-	3-5 e-
Dynamic Range	75 dB	80 dB
Power Dissipation	1.5 W	<10 mW
Pixel Size	7.3 μm x 7.6 μm	7.5 μm x 7.5 μm
Aperture	>60% with microlens	>90 %

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ADVANTAGES OF CCDS

- Incumbent technology
- Large formats demonstrated
- Very small pixels possible
- Noiseless charge domain processing (e.g. binning, TDI)

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SOME RELEVANT PROBLEMS WITH CCDS

1. Need for nearly perfect charge transfer efficiency

   - Signal fidelity ~ η^m, η=CTE, m=# of stages
     e.g. η=0.99995, m=8000, yields fidelity of 0.67

2. Radiation softness

   - Particularly susceptible to bulk silicon damage (reduced CTE)

3. Susceptible to smear

   - Requires good light shield, FIT structure

4. High power dissipation on-chip for large, fast arrays

   - Large capacitances to drive
   - Large voltage swings (power ~ CV^2f, electroluminescence)

SOME RELEVANT PROBLEMS WITH CCDS (CONT.)

5. Difficult to integrate on-chip electronics

   - Requires high power drive electronics
   - Many voltages required
   - Process incompatible for practical CMOS signal chain integration

6. Difficult to extend spectral range

   - Want UV response $\lambda < 0.4$ microns
   - Want SWIR response to 2.5 microns
   - High CTE in non-silicon materials unlikely
   - Backside illumination fraught with problems

7. Limited readout rate

   - HDTV rates (70 MHz) require dual channel architecture

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OTHER SOLID-STATE IMAGER TECHNOLOGIES

PHOTODIODE ARRAYS

- High noise (>250 e- r.m.s.)
- Lag
- Good blue/UV response

CIDS

- High noise (~ 200 e- r.m.s.)
- Non-destructive readout

HYBRID IR FPAs

- High fill factor
- Medium noise (30-50 e- r.m.s.)
- Hybrids expensive, small array sizes (<512x512)

ACTIVE PIXEL SENSOR CONCEPT

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One or more active transistors in the pixel.

- Eliminates the need for charge transfer
- Buffer the output signal
- Provides high sensitivity (low C)
- Provides current drive capability
- Provides random access capability
- Allows low power readout
- Simplifies system design

(insert George VG here)

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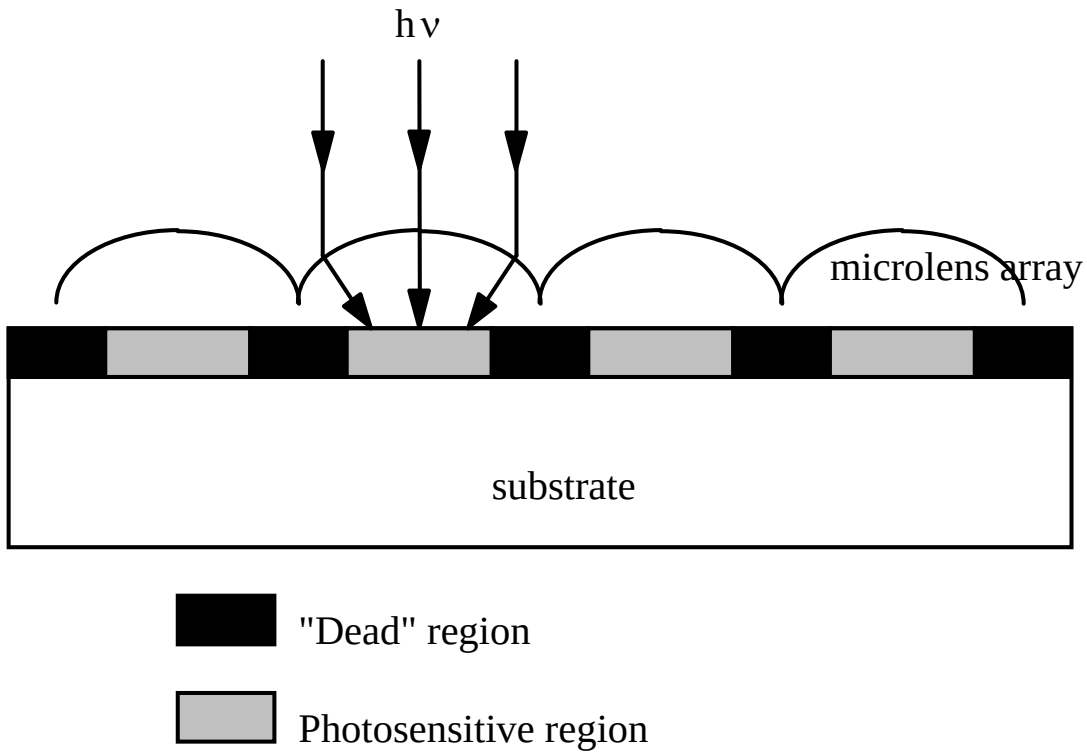
JPL CMOS ACTIVE PIXEL SENSOR

First Silicon Demonstrated:

- 100% TTL compatible input (0,5 V) on all input signals.
- X-Y addressability.
- Differential analog output signal.
- Lateral antiblooming control.
- Low read noise (22 e- rms expected)
- High sensitivity (4 μV/e-)
- Low dark current (1-10 nA/cm^2)
- High dynamic range (600 mV saturation)
- Low fixed pattern noise (<1.5% saturation)
- Vanilla CMOS design.

MICROLENS ARRAY TO INCREASE EFFECTIVE FILL FACTOR



SUMMARY OF STATE OF THE ART

	DGFSPT	CMD	BCMD	BASIS	SIT	AMI	CMOS
Developer	Toshiba	Olympus	Texas Instr.	Canon	Olympus	NHK	JPL/ Caltech
APS Type	Lateral	Vertical	Vertical	Vertical	Lateral	Lateral	Lateral
Output	Lateral	Lateral	Lateral	Vertical	Vertical	Lateral	Lateral
Pixel Size (μm)	13 x 13	5.0 x 5.2	10 x 10*	13.5 x 13.5	17 x 13.5	17.3x13.5	40 x 40*
Sensitivity	200 μV/e-	965 pA/e+	15.4 μV/e-	3.5 μV/e+	3.0 μV/e+	1.6 μV/e-	4.0 μV/e-
Input-Noise	0.8 e- rms	11.2 e+ rms	15 e- rms	60 e+ rms	69 e+ rms	130 e- rms*	22 e- rms
Dynamic Range	75 dB	68 dB	72 dB	76 dB	86.5 dB	77 dB	82 dB
FPN (p-p)	10 %	6 %	2 %	0.03 %	1.1 %	0.2 %	1.5 %
Anti-blooming	vertical	vertical*	vertical	none*	none*	lateral	lateral
Lag	0	0	0	<0.1 %	70 %	0	0
Note	discont.	*uses horiz. blnk.	*hex. layout	*uses clipping op	discont.	*100x gain e-beam=1.3	*2 μm design rule

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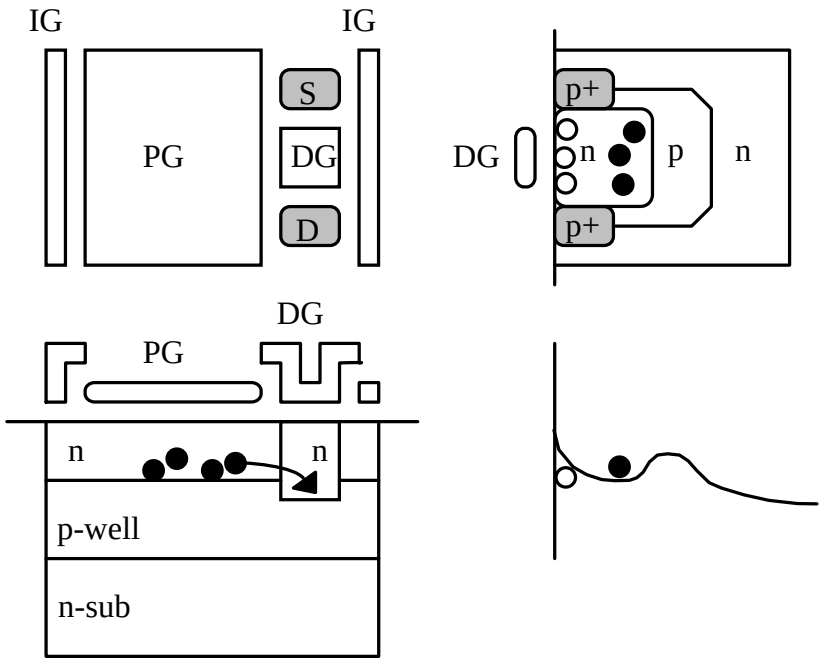
STATE OF THE ART:

TOSHIBA DOUBLE-GATE FLOATING SURFACE TRANSISTOR



- sensitivity of 200 μV/e-
- read noise 0.8 e- rms
- needs large voltage on DG

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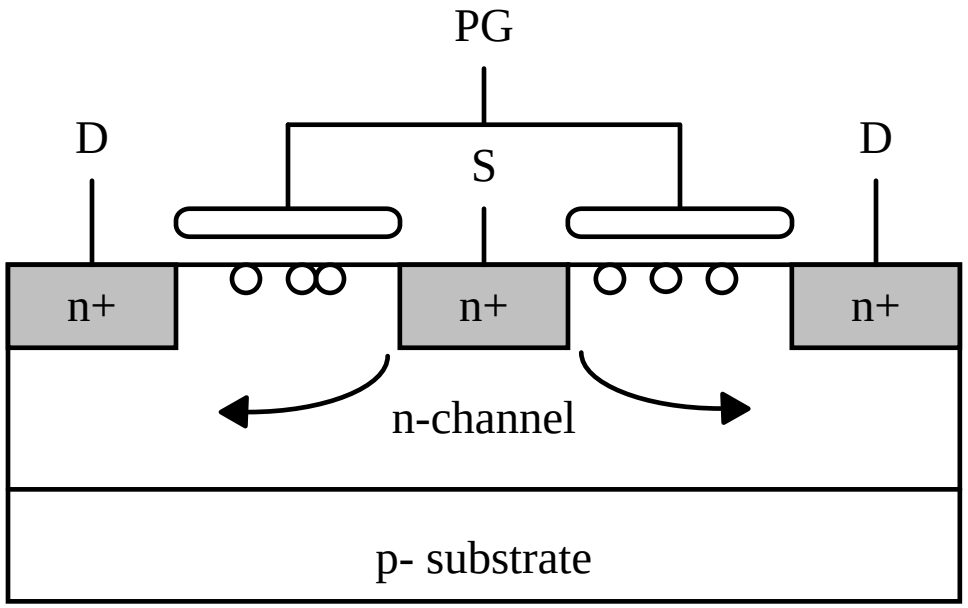
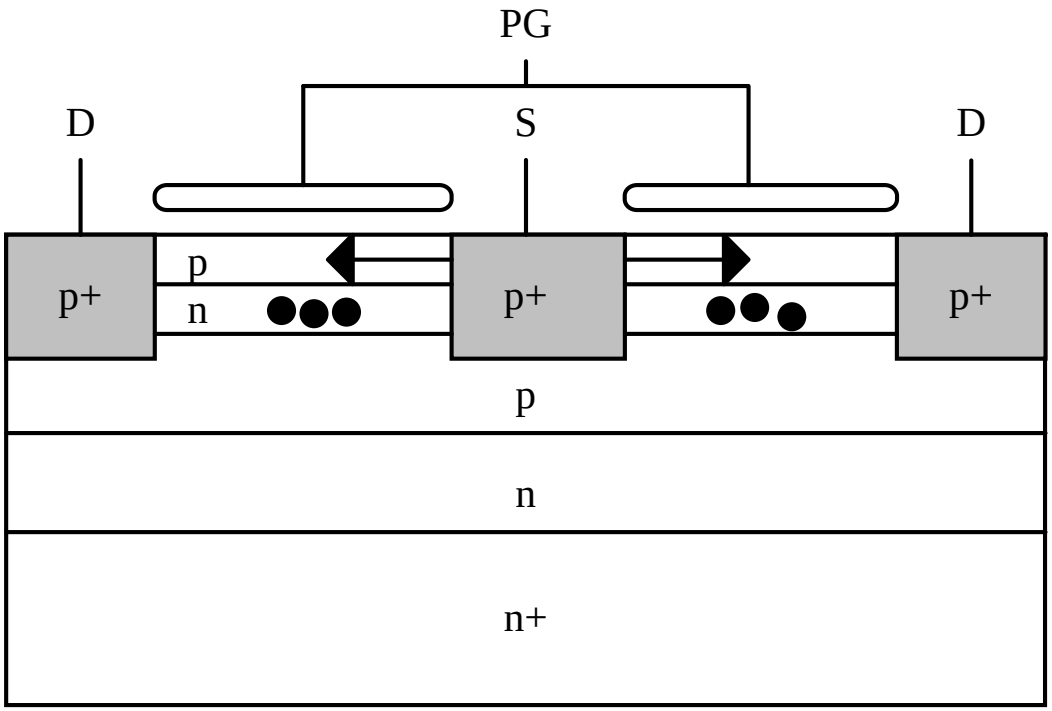
STATE OF THE ART:

OLYMPUS CHARGE-MODULATION DEVICE (CMD)



- small pixel (5.0 μm x 5.2 μm)
- gain is 965 pA/hole, 11.2 e+ rms noise
- readout is current mode
- dark current and FPN problem

STATE OF THE ART:
TI BULK CHARGE-MODULATED DEVICE (BCMD)



- sensitivity 15 μV/e-
- read noise 15 e- r.m.s.
- complex vertical layer structure

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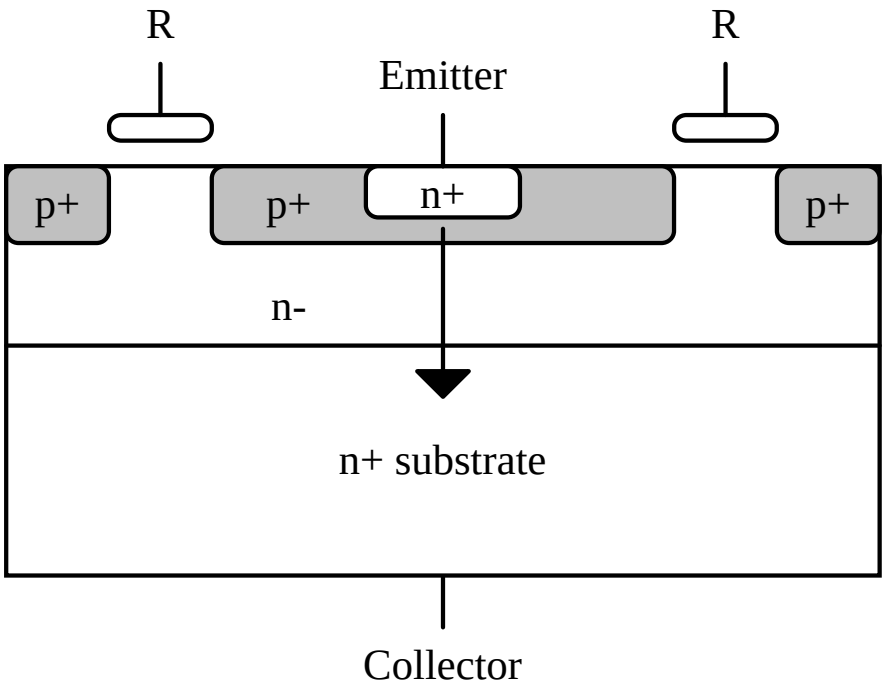
STATE OF THE ART

CANON BASE-STORED IMAGE SENSOR (BASIS)



- sensitivity 3.5 μV/e+, but kTC noise
- very low FPN (0.03%)
- good fill factor, blue response

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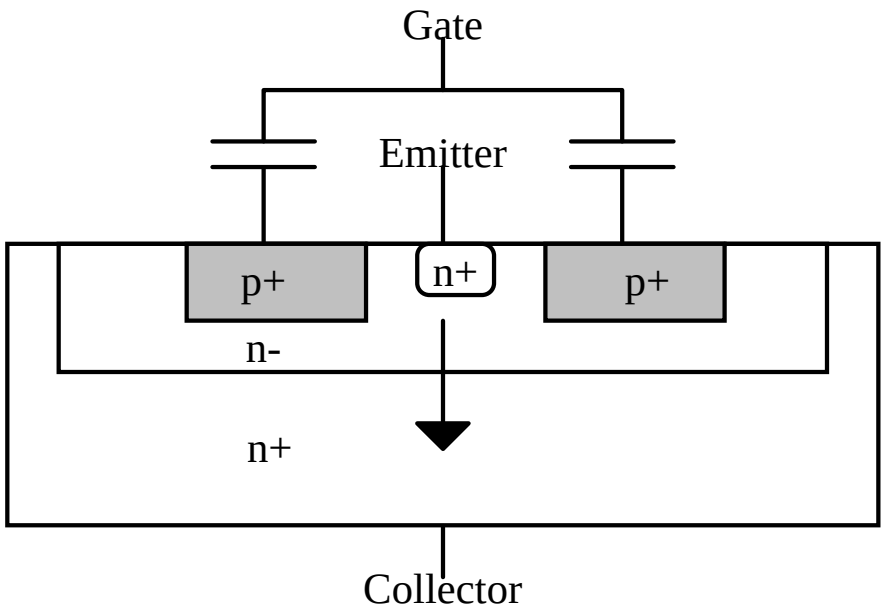
STATE OF THE ART:

OLYMPUS STATIC INDUCTION TRANSISTOR



- sensitivity 3.0 μV/e+
- large dynamic range
- large lag problem

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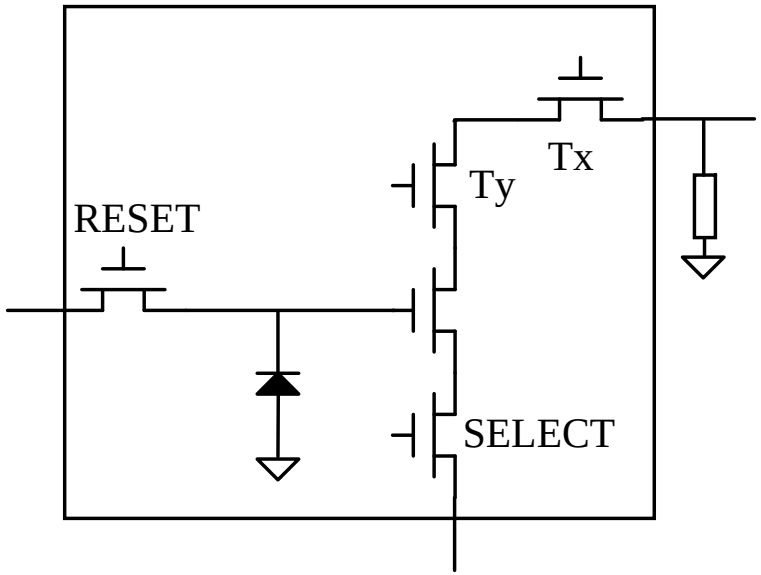
STATE OF THE ART

NHK AMPLIFIED MOS IMAGER (AMI)



- 100 x gain due to avalanche effect in a-Si
- 130 e- kTC noise = 1.3 e- photocathode-referred noise
- photocathode QE = 10 %

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COMPARISON OF APS TECHNOLOGIES

	DGFSPT	CMD	BCMD	BASIS	SIT	AMI	CMOS
FPN	✗	✗		✓	✓	✗	
Random Noise	✓			✗	✗		
Small Pixel	✗	✓	✓	✗	✗		✗
Fill Factor		✓	✓	✓	✓	✓	✗
Voltages	✗	✗	✓			✗	✓
Microlense	✓	✗	✗	✓	✗	✗	✓
Snapshot (Transfer)	✓	✗	✗	✗	✗	✗	✓
CMOS Integration		✓	✓	✓			✓

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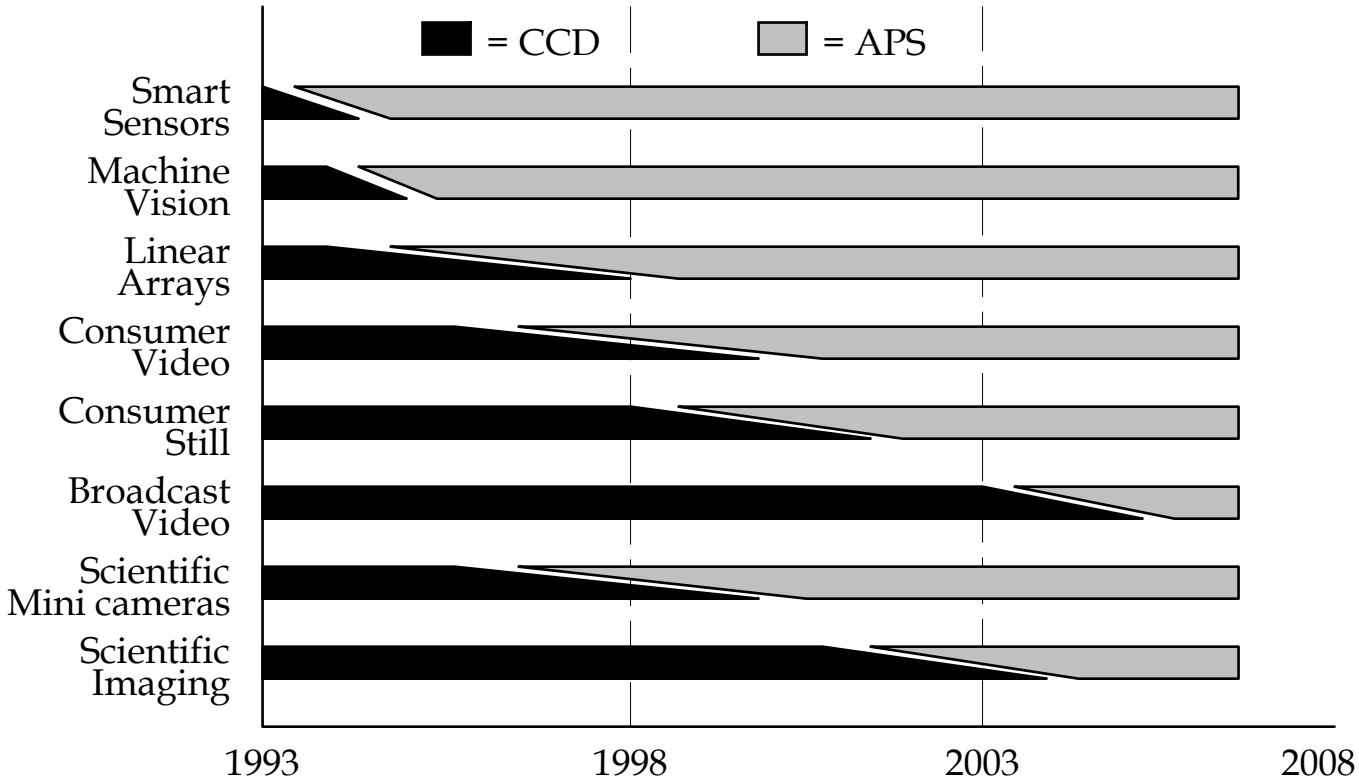
APS VS. CCD

	APS	CCD
Major Strengths	Low Power On-Chip Integration Low Smear Radiation Hardness Random Access	Incumbent Technology Small Pixels 5k x 5k Demo'd Charge-domain processing
Major Weaknesses	Lower Fill-Factor FPN Susceptibility Newer Technology	Power Requirements Incompatible w/ Integratn Need for perfect CTE

SPECULATION



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SUMMARY

- Active pixel sensors are a new, emerging technology
- APS is already becoming competitive to CCDs
- The major strength of CCDs is incumbency and current state of the art in IC design rules.
- APS needs to improve FPN using improved fab. and on-chip signal processing.
- APS is a stepping stone to highly integrated opto-electronic sensor systems (e.g. a camera on a chip)
- CCDs are future "dinosaurs".

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