ACTIVE PIXEL SENSORS:

ARE CCD'S DINOSAURS?

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SPIE Symposium on Electronic Imaging
February, 1993

ACKNOWLEDGMENTS

Tom Lee, Kodak
Suni Mendis, Columbia University
V. Sarohia, JPL
W. Hudson, NASA HQ

The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

ADVANTAGES OF CCDs

- Incumbent technology
- Large formats demonstrated
- Very small pixels possible
- Noiseless charge domain processing (e.g. binning, TDI)

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PROBLEMS WITH CCD'S

(1) Need for nearly perfect charge transfer

Table 1. CCD Fidelity vs. CTE

ARRAY SIZE	CTE	FRACTION AT OUTPUT
1024x1024	0.999	0.128
	0.9999	0.815
	0.99999	0.980
2048x2048	0.99999	0.960
4096x4096	0.99999	0.921
8192x8192	0.99999	0.849

0.99999 = 1 in 100 transfers for 1000 electrons!

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PROBLEMS WITH CCD'S (cont.)

(2) RADIATION SOFTNESS

(3) ARRAY SIZE

- CTE requirement grows
- Radiation dose tolerance decreases
- Manufacturability decreases
- Drive power increases (drive whole CCD for one pixel)

(4) DIFFICULT TO INTEGRATE ON-CHIP ELECTRONICS

- Drive electronics must drive large capacitance
- Large voltage swings require large power
- Hard to integrate with CMOS
- Large voltages lead to electroluminescence in FETs

PROBLEMS WITH CCD'S (cont.)

(5) DIFFICULT TO EXTEND SPECTRAL RANGE

- Want UV response $\lambda < 0.4$ microns
- Want SWIR response to 2.5 microns
- High CTE in non-silicon materials unlikely
- Backside illumination fraught with problems

(6) LIMITED READOUT RATE

- Scientific CCDs at 50 Kpixels/sec
- HDTV at ~50 Mpixels/sec
- Hard to drive large capacitances, poly lines at high frequencies
- CTE degrades with increasing transfer rate

OTHER SOLID-STATE IMAGER TECHNOLOGIES

PHOTODIODE ARRAYS

- High noise (>250 e- r.m.s.)
- Lag
- Good blue/UV response

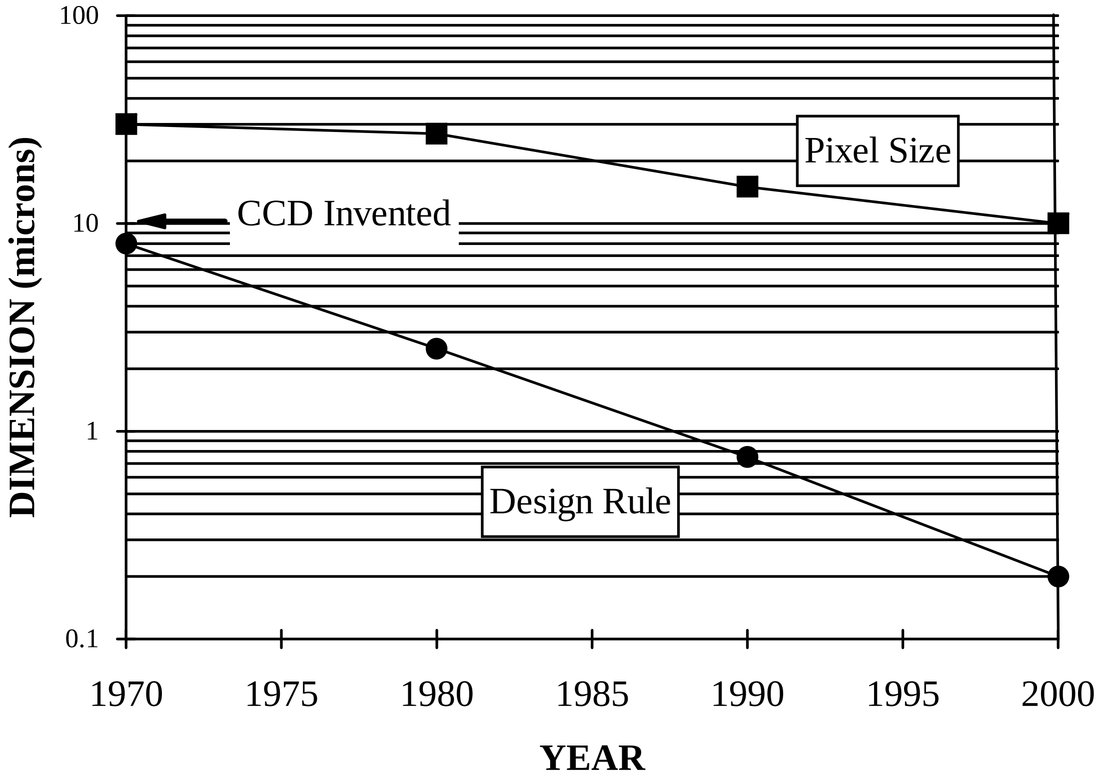
CIDS

- High noise (~ 200 e- r.m.s.)
- Non-destructive readout

HYBRID IR FPAs

- High fill factor
- Medium noise (30-50 e- r.m.s.)
- Hybrids expensive, small array sizes (<512x512)

EVOLUTION OF PHOTOLITHOGRAPHIC FEATURE SIZE VS. PIXEL SIZE



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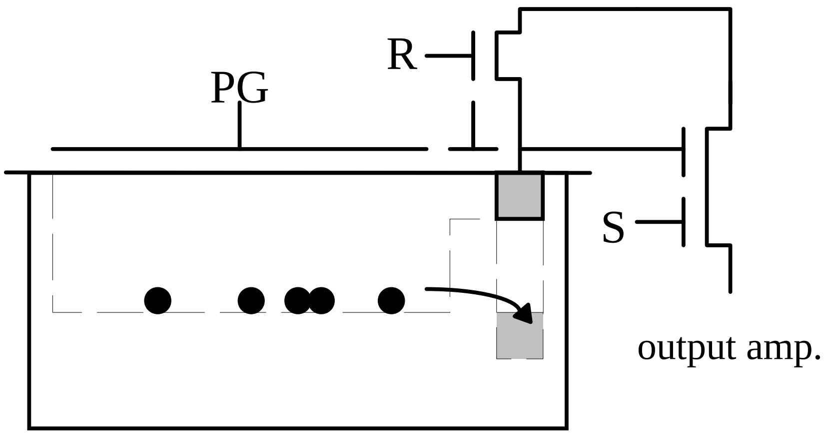
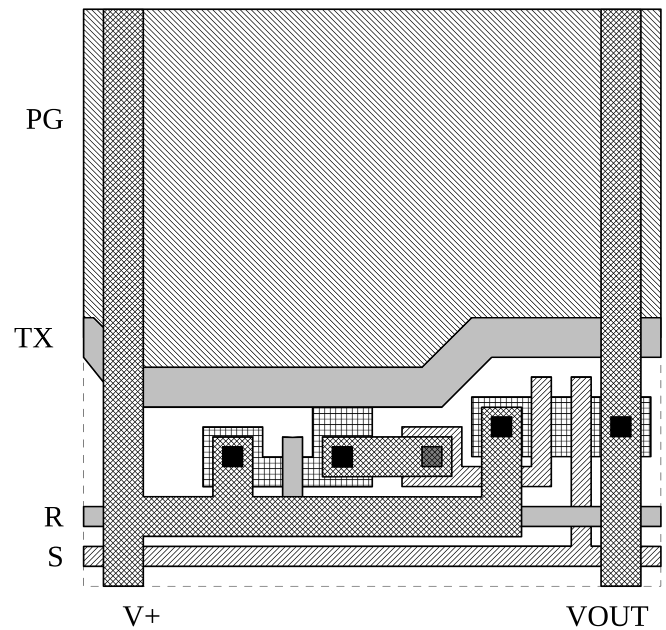
ACTIVE PIXEL CONCEPT

One or more active transistors in the pixel.

- Buffer the output signal
- Provides high sensitivity (low C)
- Provides current drive capability
- Eliminates the need for charge transfer
- Provides random access capability

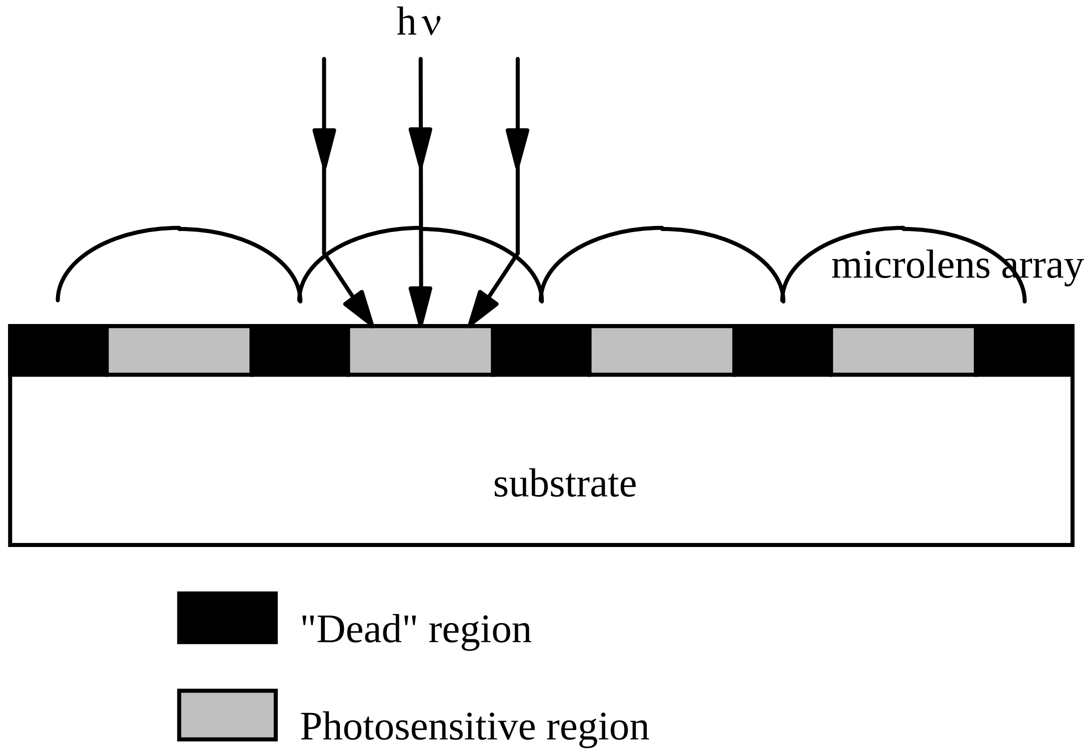
EXAMPLE OF SIMPLE APS



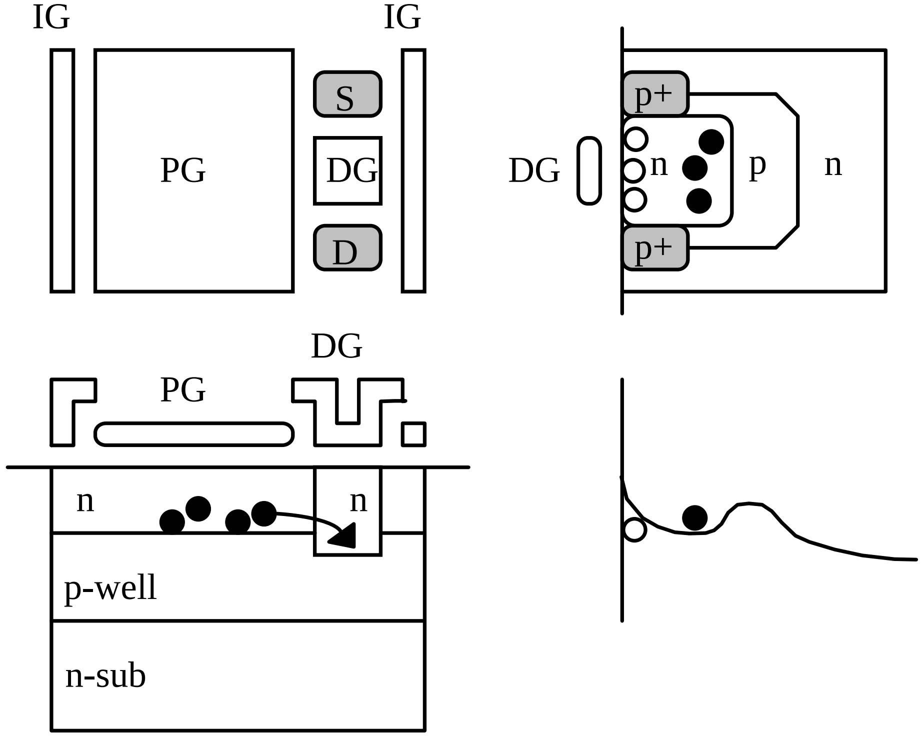


- High Sensitivity
- CDS possible for low kTC, 1/f, FPN

MICROLENS ARRAY TO INCREASE EFFECTIVE FILL FACTOR

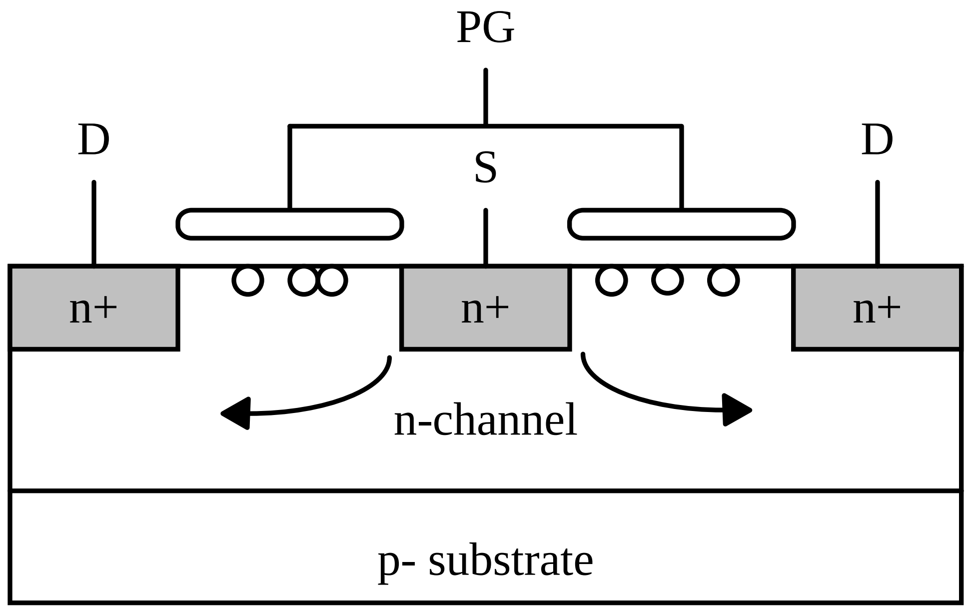


STATE OF THE ART:
TOSHIBA DOUBLE-GATE FLOATING SURFACE TRANSISTOR



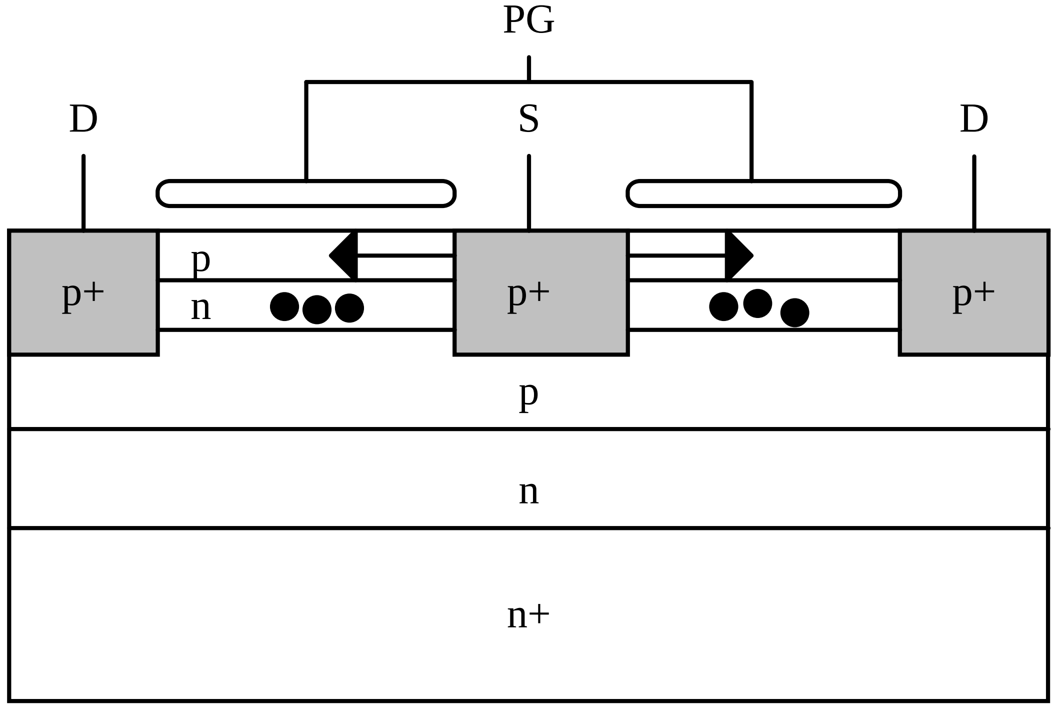
- sensitivity of 200 uV/e-
- read noise 0.8 e- rms

STATE OF THE ART:
OLYMPUS CHARGE-MODULATION DEVICE



- small pixel (7.3 um x 7.6 um)
- dark current problem
- gain is 200 pA/hole

STATE OF THE ART:
TI BULK CHARGE-MODULATED DEVICE



- sensitivity 15 uV/e-
- read noise 15 e- r.m.s.
- complex vertical layer structure

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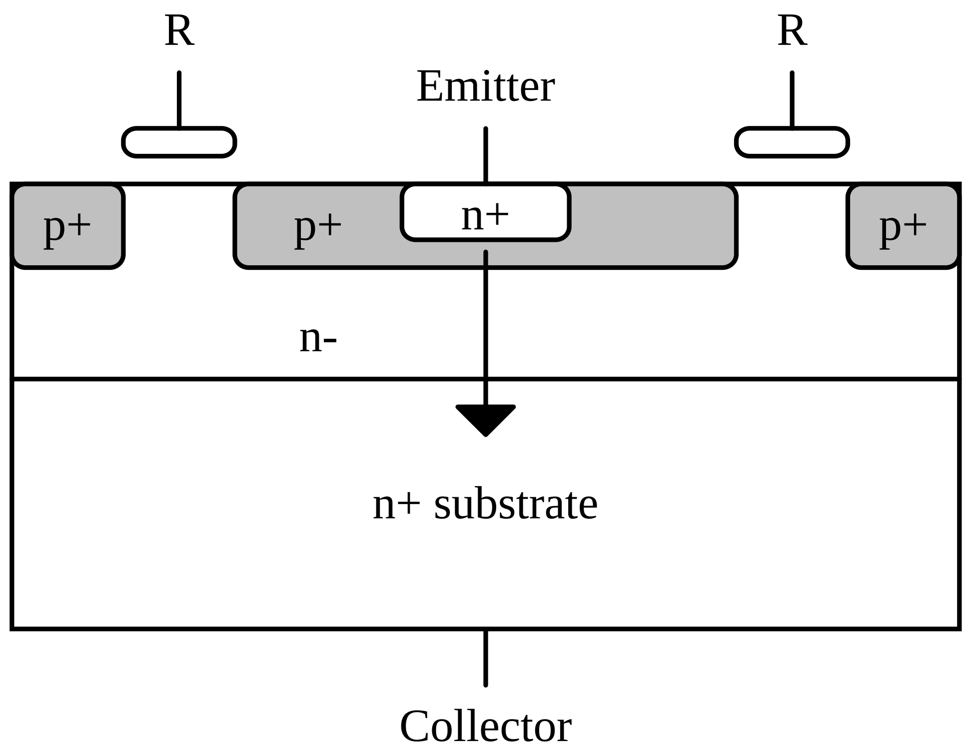
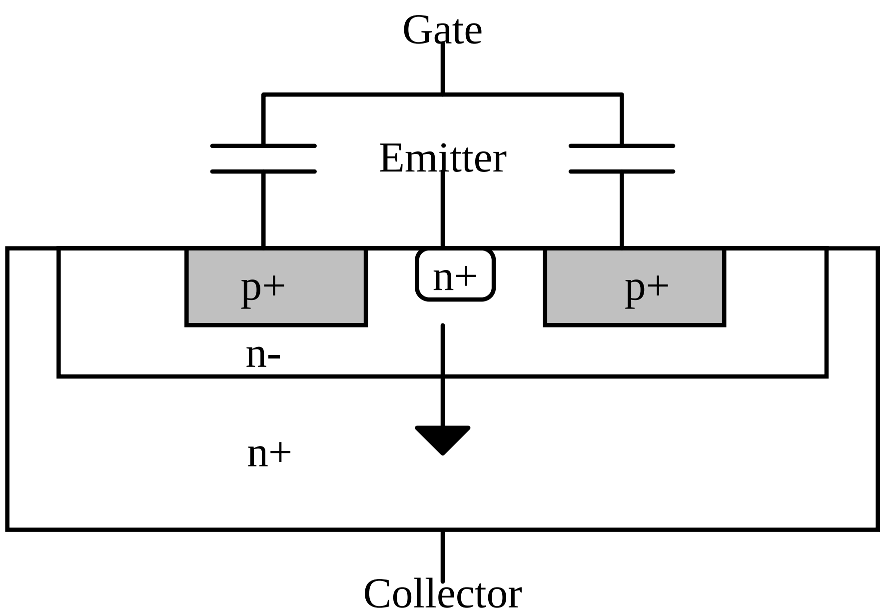
STATE OF THE ART
CANON BASE-STORED IMAGE SENSOR



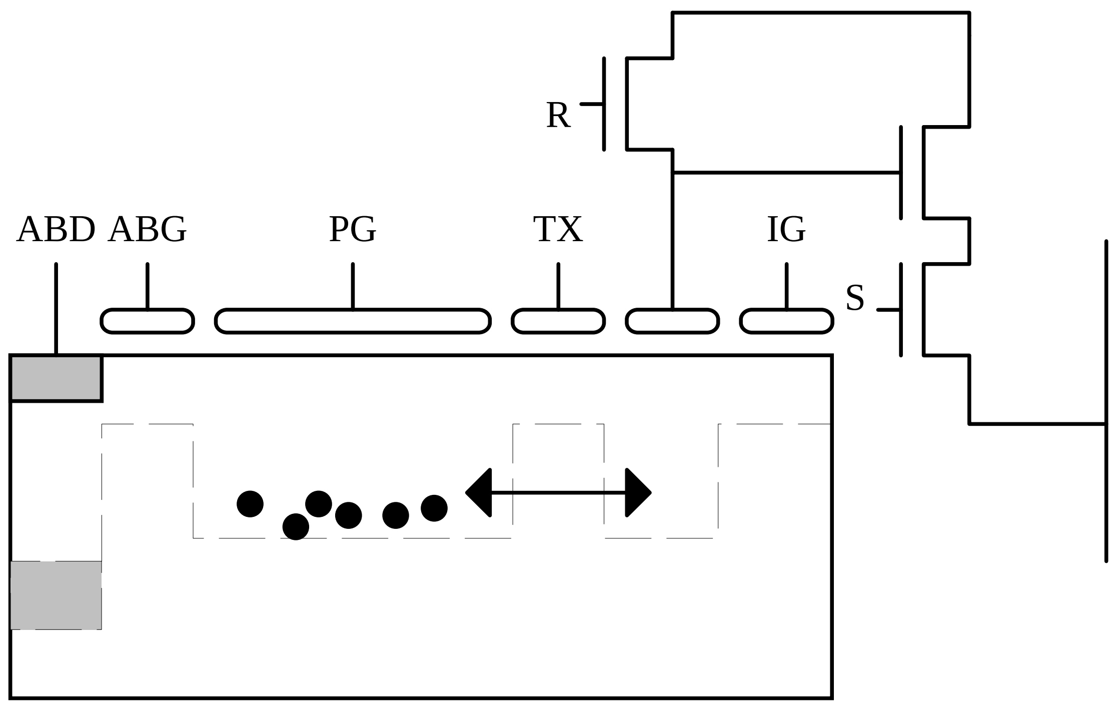
- sensitivity 3.5 µV/e+
- very low FPN (0.03%)

STATE OF THE ART:
OLYMPUS STATIC INDUCTION TRANSISTOR



- sensitivity 0.6 uV/e+
- large lag problem
- FPN 1.1 %

JPL CMOS APS



- Designed for use with on-chip A/D
  - Expect 11 e- rms read noise

SUMMARY OF STATE OF THE ART

	DGFSPT	CMD	BCMD	BASIS	SIT	CMOS
Developer	Toshiba	Olympus	Texas Instr.	Canon	Olympus	JPL/ Caltech
APS Type	Lateral	Vertical	Vertical	Vertical	Lateral	Lateral
Output	Lateral	Lateral	Lateral	Vertical	Vertical	Lateral
Pixel Size (μm)	13 x 13	7.3 x 7.6	10 x 10*	13.5 x 13.5	17 x 13.5	50 x 50
Sensitivity	200 μV/e-	250 pA/e+	15.4 μV/e-	3.5 μV/e+	0.6 μV/e+	0.6 μV/e-
Input-Noise	0.8 e- rms	400 e+ rms	15 e- rms	60 e+ rms	69 e+ rms	11 e- rms
Dynamic Range	75 dB	45 dB	72 dB	76 dB	86.5 dB	60 dB
FPN (p-p)	10 %	5 %	2 %	0.03 %	1.1 %	< 1 %
Anti-blooming	vertical	vertical	vertical	none*	none*	lateral
Lag	0	0	0	<0.1 %	70 %	0

FUTURE DIRECTIONS

- Camera-on-a-chip
- High Speed imaging
- Extended spectral range
- Guidance and navigation
- Low light level sensors

CONCLUSIONS

- Active Pixel Sensor technology in infancy compared to CCDs
- Performance already close to that of CCDs
- Eliminates many problems of CCD charge transfer
- Will likely supplant CCDs in future camera systems
- U.S. R&D activity marginal