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Berezin et al.

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(45) **Date of Patent: *May 13, 2008**

(54) **MULTI JUNCTION APS WITH DUAL SIMULTANEOUS INTEGRATION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 847 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/758,013**

(22) Filed: **Jan. 16, 2004**

(65) **Prior Publication Data**

US 2004/0169209 A1 Sep. 2, 2004

Related U.S. Application Data

(63) Continuation of application No. 09/519,930, filed on Mar. 7, 2000, now Pat. No. 6,724,426.

(60) Provisional application No. 60/124,153, filed on Mar. 8, 1999.

(51) **Int. Cl.**
H04N 5/335 (2006.01)

(52) **U.S. Cl.** **348/308**; 348/294; 348/311

(58) **Field of Classification Search** 348/303, 348/304, 305, 306, 307, 309
See application file for complete search history.

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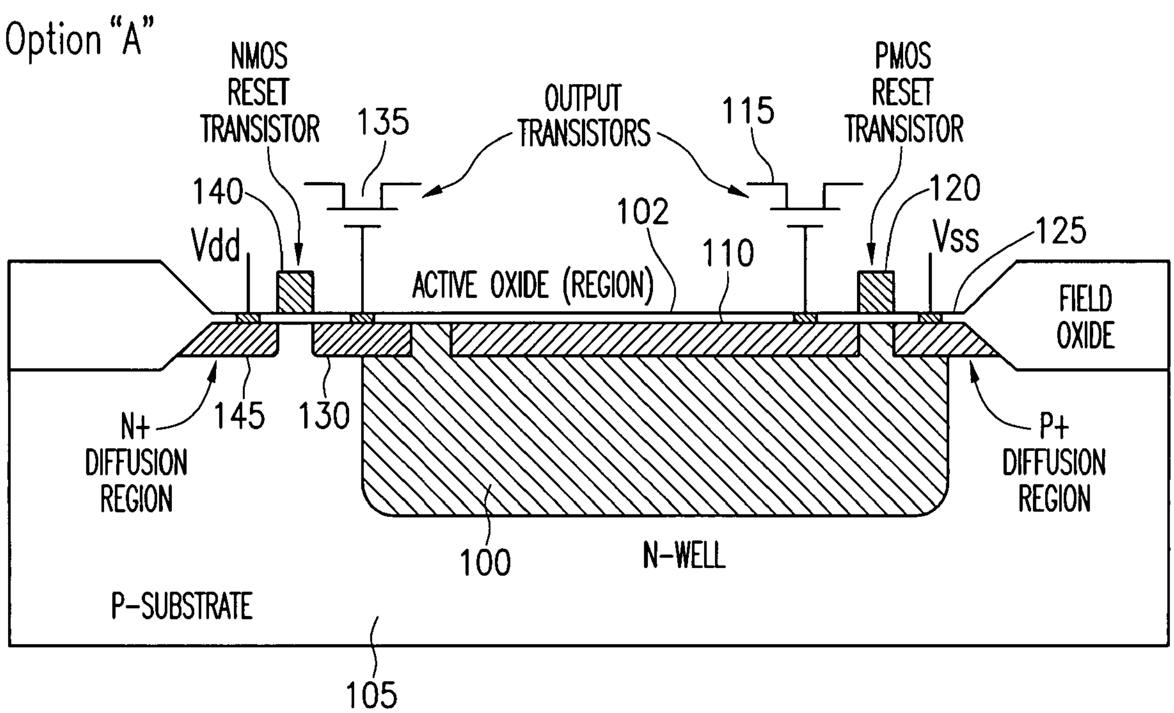
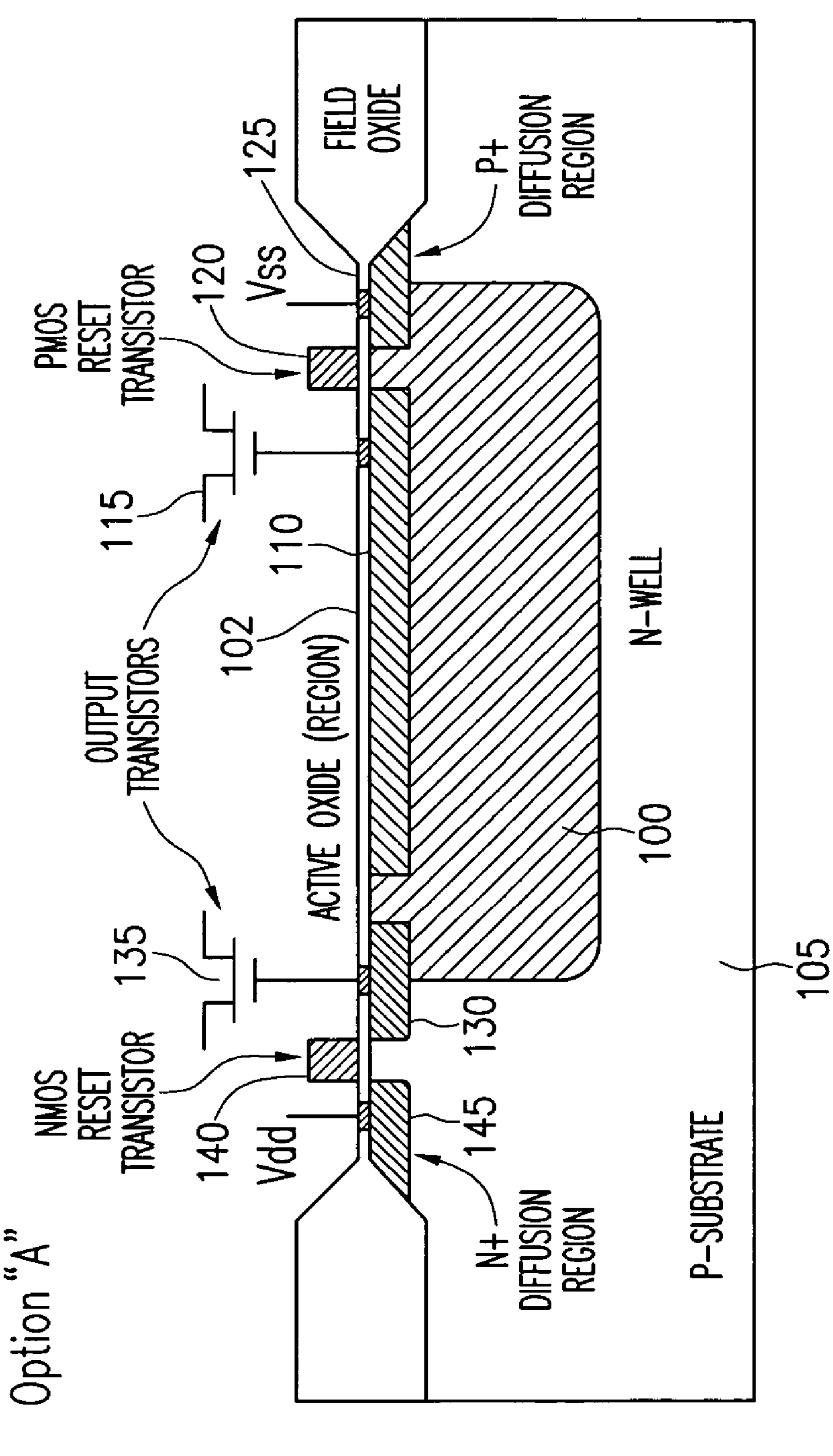
(57) **ABSTRACT**

A new kind of pixel is formed of two floating diffusions of different sizes and different conductivity type. The two floating diffusions have different image characteristics, and hence form a knee-shaped slope.

12 Claims, 2 Drawing Sheets

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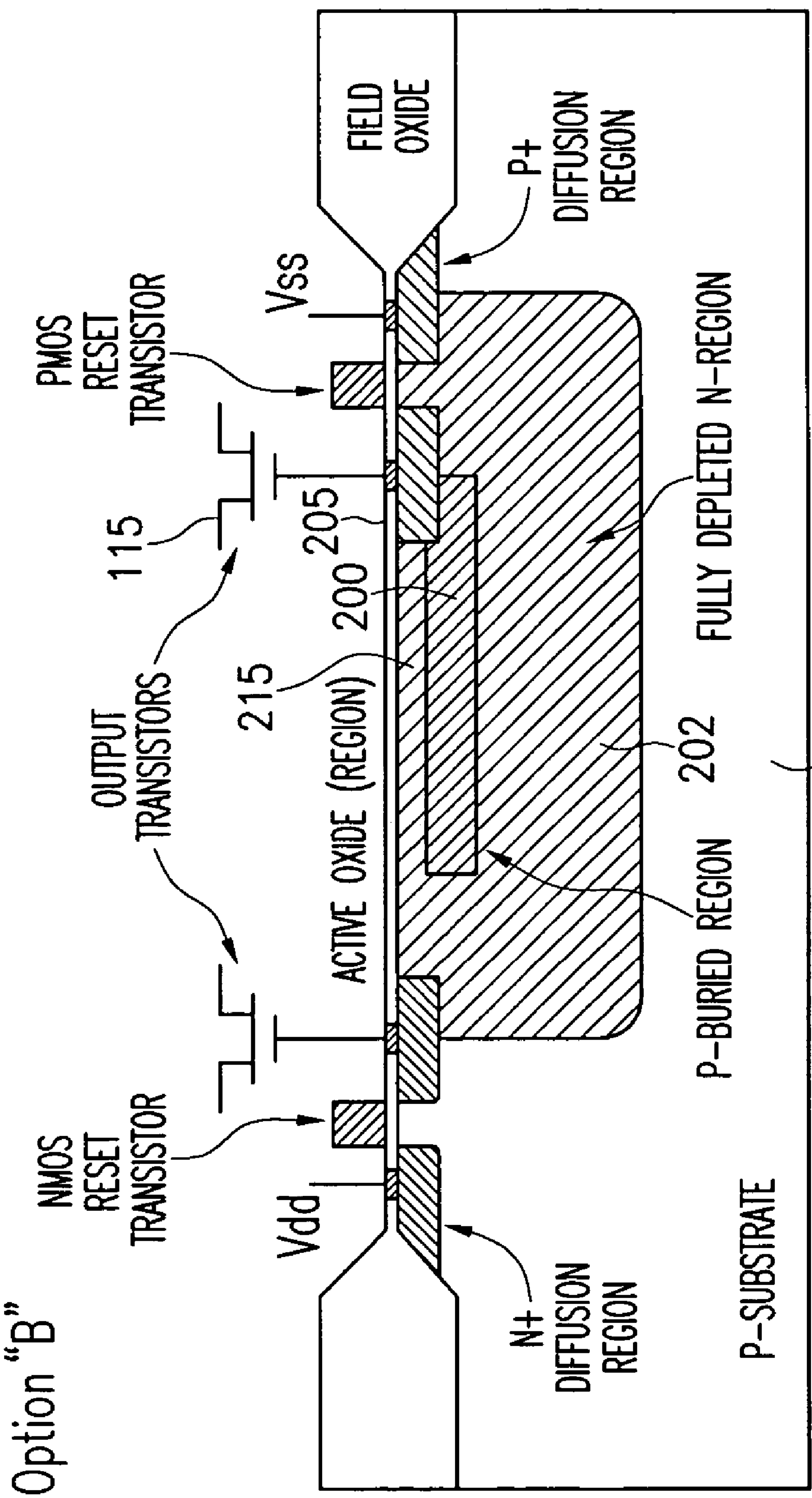
N-WELL
P-SUBSTRATE
105

FIG. 1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FULLY DEPLETED N-REGION
202
105
P-BURIED REGION
NMOS RESET TRANSISTOR
Vdd
N+ DIFFUSION REGION
P-SUBSTRATE

FIG. 2

MULTI JUNCTION APS WITH DUAL SIMULTANEOUS INTEGRATION

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefit of U.S. Provisional application No. 60/124,153, filed Mar. 8, 1999.

This application is a continuation of application Ser. No. 09/519,930, filed Mar. 7, 2000 now U.S. Pat. No. 6,724,426 (now allowed), the subject matter of which is incorporated by reference herein.

BACKGROUND

Active pixel sensors are described in U.S. Pat. No. 5,417,215. Higher charge and efficiency from these devices is desirable. In addition, different parameters and operations can benefit from different kinds of samples. For example, a short sampling period can provide the highest amount of dynamic range, while a longer sampling period can provide better resolution. Fossum and Yadid-Pecht have described one such system and "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling, IEEE Transactions On Electronic Devices, volume 44 page 1721-1723, October 1997. In that system, two signals are obtained using two different integration intervals.

SUMMARY

The present application teaches a new pixel design with dual floating diffusion regions, each of which is separately controlled. The two regions collectively provide dual integration, but do so in a way that increases sensitivity, allows dual dynamic range, and also provides multiple junctions for improved photocarrier detection.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages and features of the invention will become more apparent from the detailed description of exemplary embodiments of the invention given below with reference to the accompanying drawings, in which:

FIG. **1** is an illustration of a first embodiment of the invention; and

FIG. **2** is an illustration of a second embodiment of the invention.

DETAILED DESCRIPTION

FIG. **1** shows a first embodiment which is formed by a more standard CMOS fabrication process. There is a relatively large floating diffusion capacitance, which can tend to reduce the charge conversion gain. However, this system may be easier to make due to its use of a standard CMOS process, with the floating diffusion being on the surface.

An N-type well **100** is formed in the P-type substrate **105**. A first floating diffusion region **110** is a P-type floating diffusion region formed on the surface, i.e., its top surface close to or touching the active oxide region **102**. The P-type floating diffusion region **110** is connected to a P-type output transistor **115** and a P-type reset transistor **120**. The reset transistor **120** connects to a P+-type diffusion region **125** which is biased, for example, to the voltage level of the drain voltage.

The second floating diffusion region **130** is an N-type floating diffusion region. Note that the second floating diffusion region **120** takes up a much smaller area then the first floating diffusion region, e.g. one fifth as much area.

The second floating diffusion region is N-type, and is connected to an N-type output transistor **135**. An NMOS reset transistor **140** connects the floating diffusion region to N+ diffusion region **145**, which can be connected to a supply voltage level. In this way, a P-type region is formed extending from the edge of the P-type floating diffusion **110** to the edge of the P-type diffusion **125**. The N-type region, starting at floating diffusion **130**, is separate from the P-type region. In addition, the N-type region can surround virtually the entire active P type region, and all of the P+ region.

This new pixel design needs two separate reset control lines, one for the NMOS reset transistor **140** and the other for the PMOS reset transistor **120**. One column can be used for both output signals, e.g. with two select control lines. Alternately, two output columns can be used with one select line.

Note that since the size of the two different floating diffusion regions is different, they will store different amounts of charge. Therefore, the floating diffusion **110** can store more charge then the floating diffusion **135**. Different integration periods for these two diffusion floating regions allow a flexible saturation exposure for each element. It also facilitates obtaining a highlighted compression knee sloped light transfer curve.

A second embodiment is shown in FIG. **2**. In this embodiment, the P type diffusion region **200** is formed below the surface of the N-well **202**. An overlying N region **215** is formed above the floating diffusion, covered by the active oxide. The N-well **202**, in this embodiment, is arranged to be fully depleted. A second smaller floating diffusion region **205** is connected to the buried floating diffusion **200**, and is connected to output transistor **115**. In this way, there are three superimposed PN junctions: A first junction between the overlying N region area **215** and the buried floating diffusion **200**. Another PN junction is formed between the bottom of the floating diffusion **215** and the N region **202**. The third PN junction is between the fully depleted N region **202**, and the P type substrate **105**. The capacitance for the floating N type diffusion can be reduced by this structure.

Although only a few embodiments have been disclosed and detailed above, other modifications are possible. All such modifications are intended to be encompassed within the following claims, in which:

What is claimed is:

1. A semiconductor device, comprising:

a substrate;

a semiconductor well, formed in said substrate;

a plurality of floating diffusion regions, each having a different size and each in contact with said semiconductor well; and

a plurality of output transistors, each of said output transistors coupled to a respective one of said plurality of floating diffusion regions.

2. The device of claim **1**, wherein each of said plurality of floating diffusion regions is formed at a surface of the semiconductor well.

3. The device of claim **1**, further comprising:

an active oxide covering a surface of said semiconductor well.

4. The device of claim **1**, wherein each of said floating diffusion regions further is coupled to its own reset transistor, for controllably supplying a reset level in response to a reset signal.

5. The device of claim 1, wherein said semiconductor substrate is of a first conductivity type and said semiconductor well is of a second conductivity type different from said first conductivity type.

6. An image sensor, comprising:

a semiconductor substrate;

a first semiconductor well, formed within said semiconductor substrate;

a plurality of floating diffusion regions, each of a different size and each at least partially formed in said first semiconductor well;

a plurality of transistor connection elements, each enabling connection to a respective one of said plurality of floating diffusion regions, to obtain outputs indicative of an amount of light collected thereby; and

a photosensor, disposed on said semiconductor substrate, for supplying charged based upon light incident upon said photosensor to said floating diffusion regions.

7. The sensor of claim 6, further comprising:

a plurality of reset elements, each respectively connected to reset a respective one of said plurality of floating diffusion regions.

8. The sensor of claim 6, wherein said semiconductor substrate is P-type, said semiconductor well is N-type, and said plurality of floating diffusion regions include at least one N-type region and at least one P-type region.

9. The sensor of claim 6, wherein at least one of said floating diffusion regions surround another one of said floating diffusion regions.

10. The sensor of claim 6, wherein when said sensor is operational said semiconductor well is fully depleted.

11. A method of converting light to a signal, comprising:

receiving light simultaneously in a plurality of floating diffusion regions, each having a different size, each having a conductivity type, and each producing an output indicative of a different gradation of the incoming light; and

sampling each of said floating diffusion regions using a transistor.

12. The method of claim 11, wherein each said transistor used to sample a floating diffusion region has a same conductivity type as the floating diffusion region being sampled.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,372,490 B2
APPLICATION NO. : 10/758013
DATED : May 13, 2008
INVENTOR(S) : Berezin et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 1, line 11, before ", the" delete "(now allowed)".

Signed and Sealed this

Twenty-sixth Day of August, 2008

JON W. DUDAS
Director of the United States Patent and Trademark Office