

(54) **DIFFERENTIAL NON-LINEARITY CORRECTION SCHEME**

(75) Inventor: **Eric R. Fossum**, La Crescenta, CA (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **May 14, 2002**

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Related U.S. Application Data

(63) Continuation of application No. 09/739,932, filed on Dec. 18, 2000, now Pat. No. 6,388,593, which is a continuation of application No. 09/170,944, filed on Oct. 13, 1998, now Pat. No. 6,215,428.

(60) Provisional application No. 60/062,854, filed on Oct. 14, 1997.

(51) **Int. Cl.⁷** **H03M 1/06**

(52) **U.S. Cl.** **341/118; 341/155**

(58) **Field of Search** **341/118, 155, 341/172, 163, 144**

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,385,286	A *	5/1983	Haque	341/144
4,404,544	A *	9/1983	Dwarakanath	341/172
4,618,847	A *	10/1986	Iida et al.	341/144
4,764,750	A *	8/1988	Kawada	341/163
4,831,381	A *	5/1989	Hester	341/172
4,908,620	A *	3/1990	Fujisawa	341/108
5,258,761	A *	11/1993	Fotoubi et al.	341/172
5,416,485	A *	5/1995	Lee	341/172
5,581,252	A *	12/1996	Thomas	341/144
6,288,661	B1 *	9/2001	Holberg	341/145
6,388,593	B2 *	5/2002	Fossum	341/118

* cited by examiner

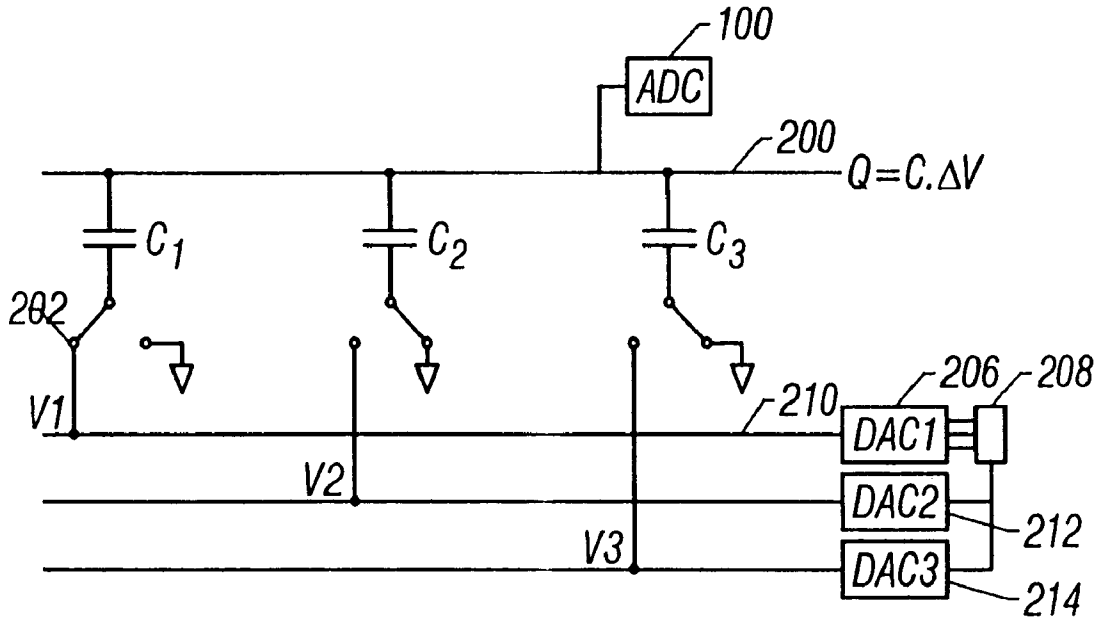
Primary Examiner—Peguy Jeanpierre

(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin & Oshinsky LLP

(57) **ABSTRACT**

Differential non-linearity errors in an A/D converter are corrected by an analog system. The system produces different analog voltages which are used to correct the input voltage to the capacitor. The input voltage is changed by an amount which is effective to correct the $C\Delta V$ to be the same as it would have been if the DNL error had not occurred.

15 Claims, 1 Drawing Sheet



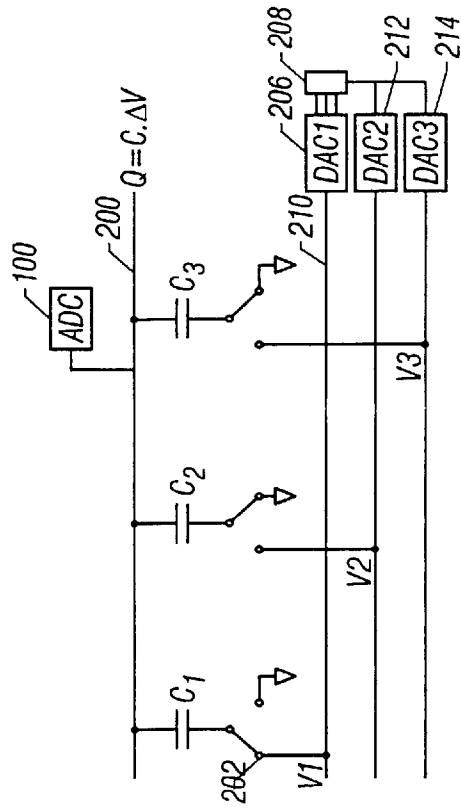


FIG. 2

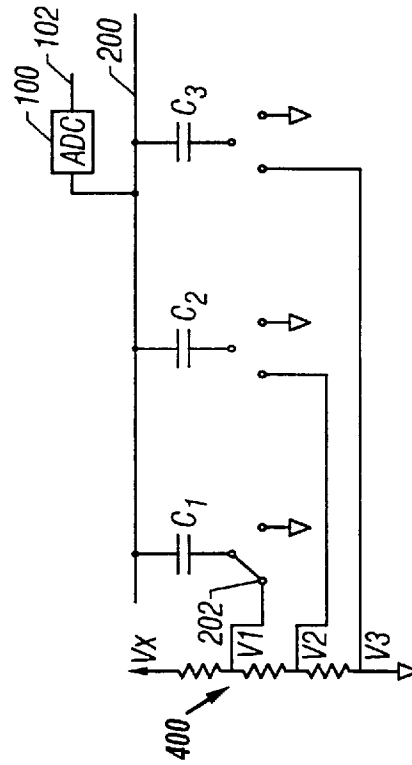


FIG. 4

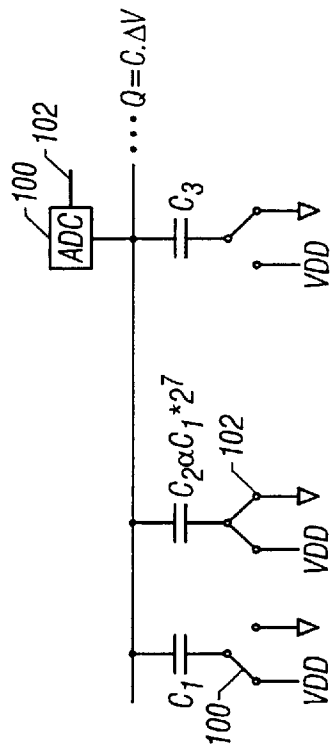


FIG. 1
(Prior Art)

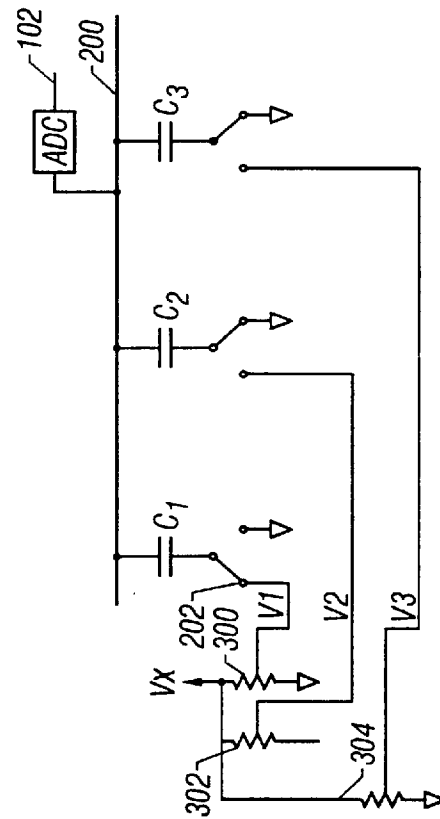


FIG. 3

DIFFERENTIAL NON-LINEARITY CORRECTION SCHEME

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 09/739,932, filed Dec. 18, 2000 now U.S. Pat. No. 6,388,593, which is a continuation of U.S. application Ser. No. 09/170,944, filed Oct. 13, 1998, now U.S. Pat. No. 6,219,428 which claims the benefit of the U.S. Provisional Application Nos. 60/062,854, filed on Oct. 14, 1997.

FIELD

The present specification describes a technique of correcting for differential non-linearity in an A/D converter.

BACKGROUND

Certain A/D converters, including a successive approximation A/D converter, operate based on calibrated capacitors.

A plurality of capacitors are provided. Each capacitor has a capacitance that is related to the other capacitors according to powers of 2. Hence, the capacitors produce an output charge where each represents one bit of the final digital signal. The A/D converter uses these capacitors to estimate the digital signal that it will produce.

The estimation includes changing each bit between a 1 and 0, which effectively changes the connection to each capacitor. FIG. 1 shows the connection to each capacitor C1, C2, C3, being switched between two voltages: the source voltage VDD and ground. The switching is based on whether the bit associated with that capacitor is 1 or 0. The number of switches and number of capacitors hence corresponds to the number of bits, with one capacitor being associated with one bit.

The output of the capacitor string is used by the A/D converter 100 to produce its output 102. The output 102 depends, upon other things, on the accuracy of the capacitors and their scaling.

As described above, each capacitor has a capacitance value which should be equal to a basic capacitance value $C_x \cdot 2^n$, where n+1 is the number of bits of resolution of the A to D converter.

Even though the capacitors are scaled relative to one another, there are often errors in the scaling. A differential non-linearity can occur based on errors in the relationship of the sizes and capacities of the capacitors. The mechanisms and causes of differential non-linearities are well known in the art.

The differential non-linearities cause certain codes in the output of the A/D converter to be missing. This effectively reduces the dynamic range of the A/D converter, causes granularity, and also may be perceived as noise. It is desirable to correct the differential non-linearity.

It has been suggested to correct a differential non-linearity by using a look-up table for each value. This, however, requires a lot of memory.

A co-pending and commonly-assigned application suggests correcting the differential non-linearity by assigning a correction value to each active bit.

The present specification teaches a different solution to solving differential non-linearity problems. This is done by adjusting an analog voltage which is placed on the capacitor. Hence, the previous-known solutions require a digital correction.

According to the preferred mode, the operation is corrected by changing the bias voltage that is applied to the capacitors. In the prior art, each of the capacitors C1, C2, . . . CN, receives the same voltage: typically the rail voltage VDD. According to this system, at least a number of the capacitors receive customized voltages which are different than the rail voltage. These voltages are customized to correct for the differential non-linearity error caused by errors in scaling of the values of the capacitors.

In a first preferred mode, the corrected voltages are produced by digital-to-analog converters which are driven by a memory storing correction values.

Another alternative which is completely analog uses a variable resistor or resistor ladder to do this.

DESCRIPTION OF THE DRAWINGS

These and other aspects will now be described in detail with reference to the accompanying drawings, wherein:

FIG. 1 shows a prior art system of operating A/D converter using a capacitor bank;

FIG. 2 shows a first embodiment using a biased capacitor bank to operate an A/D converter;

FIG. 3 shows a third embodiment using an all analog system with a potentiometer to operate the A/D converter bank; and

FIG. 4 shows a fourth embodiment using a resistor ladder.

DESCRIPTION OF THE EMBODIMENTS

FIG. 2 shows a preferred embodiment of the compensation system. The output charge on the line 200, which is connected to the A/D converter 100, is proportional to the voltage on the capacitors and the values of the capacitors. The capacitors in FIG. 2 are scaled similarly to those in FIG. 1: where a value of each capacitor $C_n = C_x \cdot 2^n + \text{offset}_n$, where n ranges from 0 to the number of total bits—1. The offsets_n represents the differential non-linearity for the specific bit, which represents the undesired effect.

The output charge on the line 200 drives the A/D converter and provides a reference for determining whether the current estimate of the A/D converter is correct. According to this embodiment, an active node 202 of the capacitor is connected to a voltage which differs from VDD by an amount which compensates for the error in capacitance value. All or just some of the capacitors can be compensated in this way. If only some of the capacitors are corrected, it is preferably the ones corresponding to the most significant bits.

Assuming FIG. 2 is to represent a three-bit A/D converter, the charge on the line 200 can be expressed as follows.

$$Q = (C_x + DNL_1) \cdot \Delta V_1 + (2C_x + DNL_2) \cdot \Delta V_2 + (4C_x + DNL_3) \cdot \Delta V_3 \quad (\text{Equation 1})$$

Differential non-linearities in the A to D converter are measured using a standard technique. The differential non-linearities associated with each of the bits is then taken as known, hence, DNL₁, DNL₂, and DNL₃ are all known in equation (1) Then, since Q=CAV, V₁, V₂, and V₃ can be calculated and stored as compensation values.

The compensation values are stored in programmable element 208 which can be, for example, fusible links or a memory. These values are used to drive the respective D/A converters which are preferably located on the same semiconductor substrate along with the A/D converter 100, and the capacitors C1 through C3. Each of the D/A converters 206, 212, and 214 produces a respective output. The DAC1

produces output **210** which represents the voltage value V_1 . Similarly, DAC2 produces an output V_2 and DAC3 produces an output V_3 . Effectively this changes the ΔV associated with the capacitor in a way which compensates for the respective non-linearity.

As described above, this solution, unlike other solutions, corrects the analog part of the analog to digital converter circuit.

A solution which is even more analog is shown in FIG. 3. FIG. 3 shows the same basic capacitor and A/D converter setup. However, in FIG. 3, a voltage V_X is provided biasing three potentiometers **300**, **302**, **304**. These potentiometers are set to a position where they will produce the desired output. For example, the potentiometer **300** is set to produce the voltage V_1 , the potentiometer **302** is set to produce the voltage V_2 , and the potentiometer **304** is set to produce the voltage V_3 . This effectively carries out a totally analog solution to the problem, without requiring any on-chip digital circuitry.

Yet another totally analog solution is shown in FIG. 4. In this solution, the bias voltage V_X biases a resistive ladder **400**. Taps between the various resistances are attached to the respective active terminals, e.g., terminal **200**. The voltage divider and taps are set such that the appropriate bias voltages V_1 , V_2 , V_3 are supplied to the appropriate pins.

Although only a few embodiments have been disclosed in detail above, those of skill in the art will certainly understand that modifications are possible in these embodiments while still maintaining within the teaching of the present invention and specifically within the claims.

For example, the preferred mode teaches the differential non-linearity-corrected total charge which is a reference for an A/D converter. However, the charge on line **200** could be used to drive any similar device which requires scaled charge. Other analog digital systems could be used to produce the DNL-corrective voltages V_1 , V_2 , V_3 . In addition, while an example of 3-bits is given, it should be understood that this same system could be used to correct 1 bit, 2 bits, or any number of bits. This system could be used to correct all bits of A/D converter, or only some bits of the A/D converter. This same concept could also be used to correct a D/A converter.

While the preferred mode describes changing one of the switched values on the capacitor, either one or both could be changed.

All of these modifications are intended to be encompassed within the claims, in which:

What is claimed is:

1. An electrical device, comprising:

a plurality of charge storage devices coupled together, each of said charge storage devices being configured to store a different level of charge relative to the other charge storage devices; and

a compensation portion for determining a level of compensation required by at least a first and a second one of said plurality of charge storage devices, wherein

said compensation portion is configured to charge said first charge storage device to a first voltage and said second charge storage device to a second voltage different from said first voltage.

2. The device as in claim 1, wherein said compensation portion comprises a potentiometer.

3. The device as in claim 1, wherein said compensation portion comprises a digitally controllable analog voltage production unit.

4. The device as in claim 3, wherein said compensation portion comprises a D/A converter.

5. The device as in claim 4, further comprising a memory for storing values indicative of said compensation levels, and wherein said memory is coupled to said D/A converter for forwarding to said D/A converter said values indicative of said compensation levels.

6. The device as in claim 1, wherein said charge storage devices comprise sealed capacitors.

7. An analog to digital converter, comprising:

a plurality of capacitors having storage capacities that are scaled relative to one another;

a memory for storing correction values for compensating for inaccuracies in said storage capacities of said plurality of capacitors; and

an analog correction portion for carrying out an analog correction of said inaccuracies.

8. The system as in claim 7, wherein said analog correction portion comprises a resistive ladder.

9. The system as in claim 8, wherein said analog correction portion comprises a potentiometer.

10. The system as in claim 8, wherein said analog correction portion comprises a D/A converter.

11. A differential non-linearity correction system, comprising:

a plurality of charge storage devices coupled together for respectively storing charges according to a scaled relationship between said plurality of scaled charge storage devices; and

a correction portion having a respective output coupled to each of said plurality of charge storage devices for correcting an error with said scaled relationship in an analog domain.

12. The system as in claim 11, wherein said correction portion comprises a resistive ladder.

13. The system as in claim 11, wherein said correction portion comprises at least one potentiometer.

14. The system as in claim 11, wherein said correction portion comprises at least one D/A converter.

15. The system as in claim 14, further comprising a memory device for storing a correction value for at least one of said plurality of charge storage devices, said memory device being coupled to said at least one D/A converter.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,677,872 B2
DATED : January 13, 2004
INVENTOR(S) : Eric R. Fossum

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2,

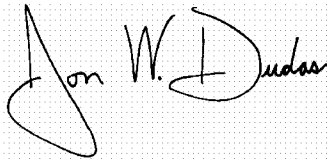
Line 37, "offsets,," should read -- offset_n --.

Column 4,

Line 1, "compression" should read -- compensation --; and
Lines 31 and 33, claim reference number "8" should read -- 7 --.

Signed and Sealed this

Sixth Day of July, 2004

A handwritten signature in black ink on a dotted background. The signature reads "Jon W. Dudas" in a cursive style.

JON W. DUDAS

Acting Director of the United States Patent and Trademark Office