

(12) **United States Patent**
Shaw et al.

(10) **Patent No.:** **US 6,606,122 B1**
(45) **Date of Patent:** **Aug. 12, 2003**

- (54) **SINGLE CHIP CAMERA ACTIVE PIXEL SENSOR**
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- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/162,920**

(22) Filed: **Sep. 29, 1998**

Related U.S. Application Data

- (60) Provisional application No. 60/060,236, filed on Sep. 29, 1997.
- (51) **Int. Cl.**⁷ **H04N 3/14; H04N 5/335; H01L 27/00**
- (52) **U.S. Cl.** **348/302; 250/208.1; 257/291; 348/308; 348/294**
- (58) **Field of Search** **250/208.1; 340/302, 340/294, 297, 298, 308, 311, 312; 257/290, 291, 292, 443, 444**

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Primary Examiner—Wendy R. Garber

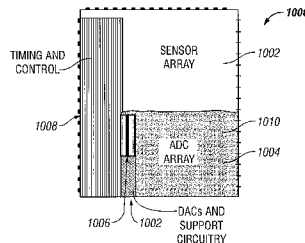
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(57) **ABSTRACT**

A totally digital single chip camera includes communications to operate most of its structure in serial communication mode. The digital single chip camera include a D/A converter for converting an input digital word into an analog reference signal. The chip includes all of the necessary circuitry for operating the chip using a single pin.

6 Claims, 13 Drawing Sheets



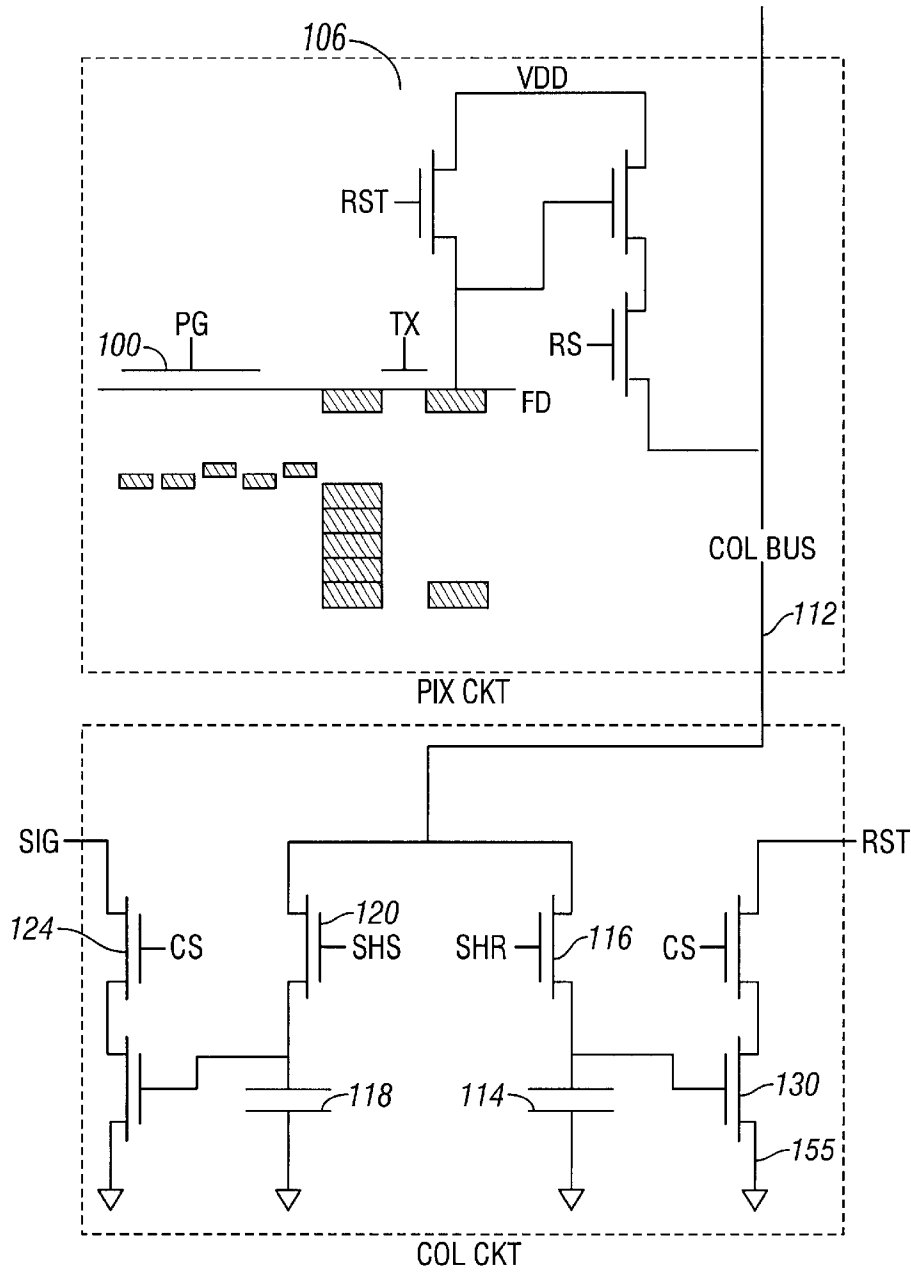


FIG. 1

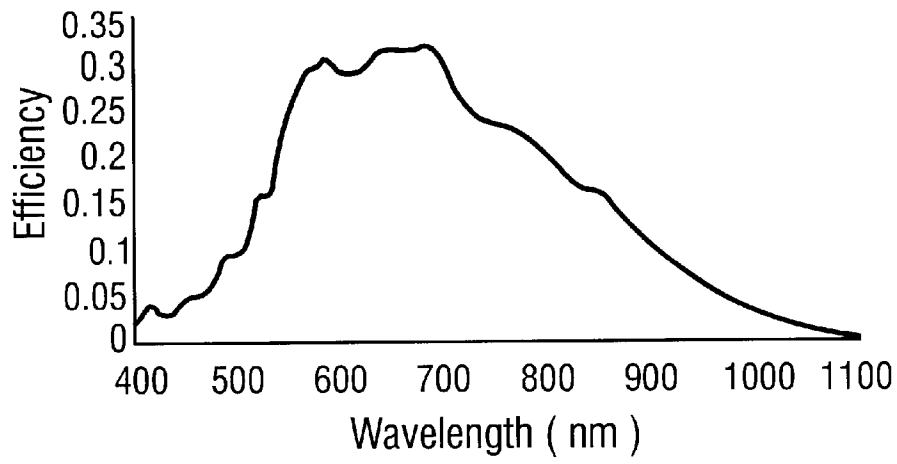
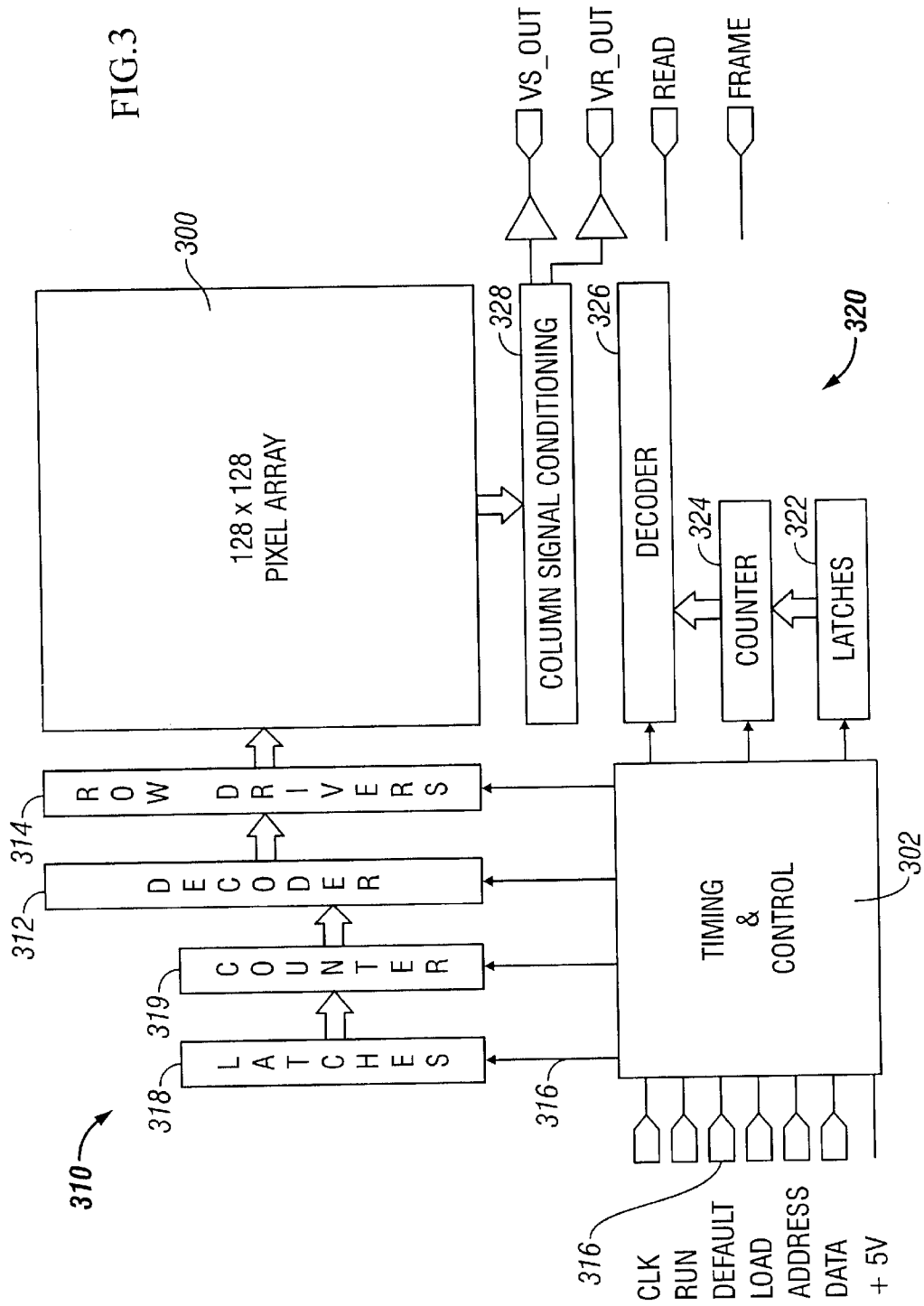


FIG. 2

FIG. 3



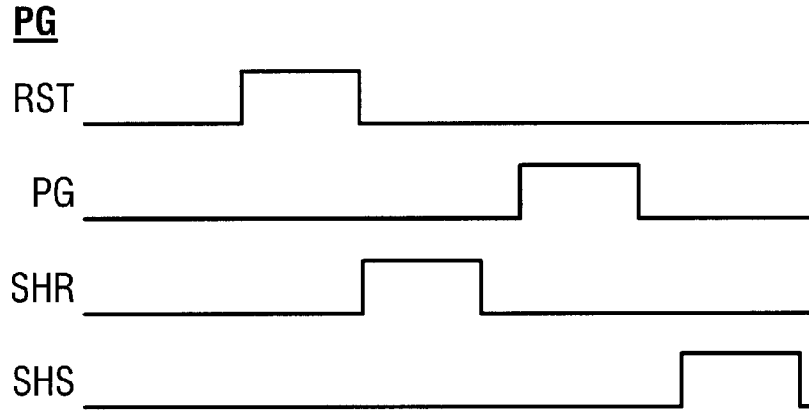


FIG. 4A

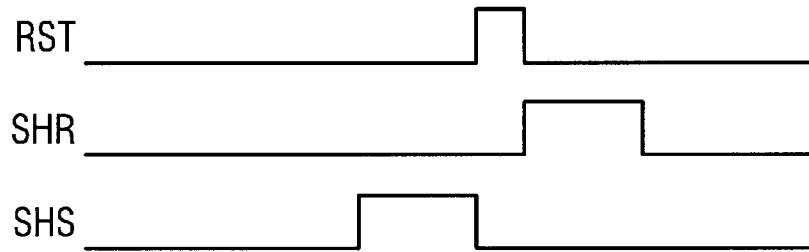


FIG. 4B

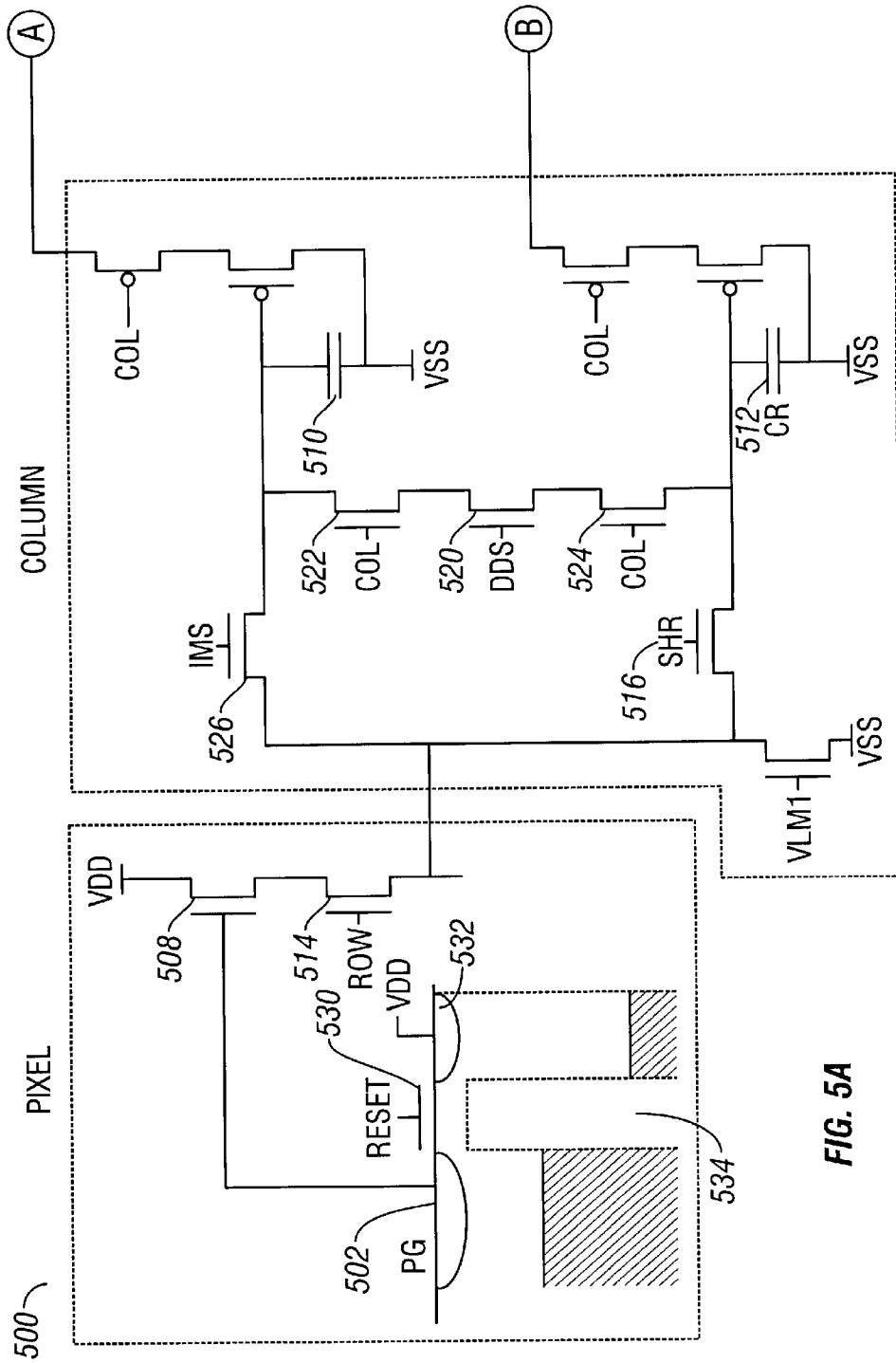


FIG. 5A

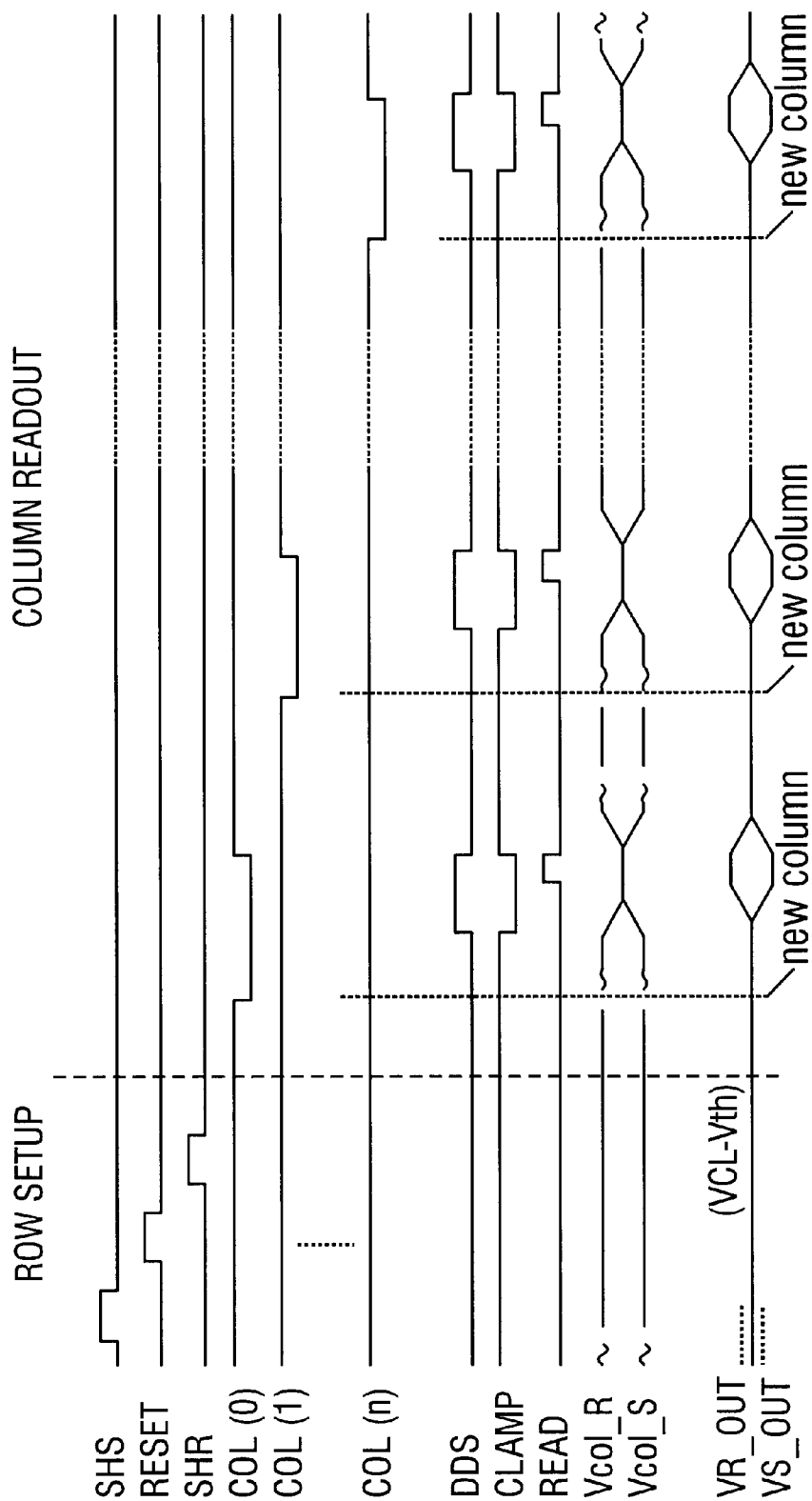


FIG. 6

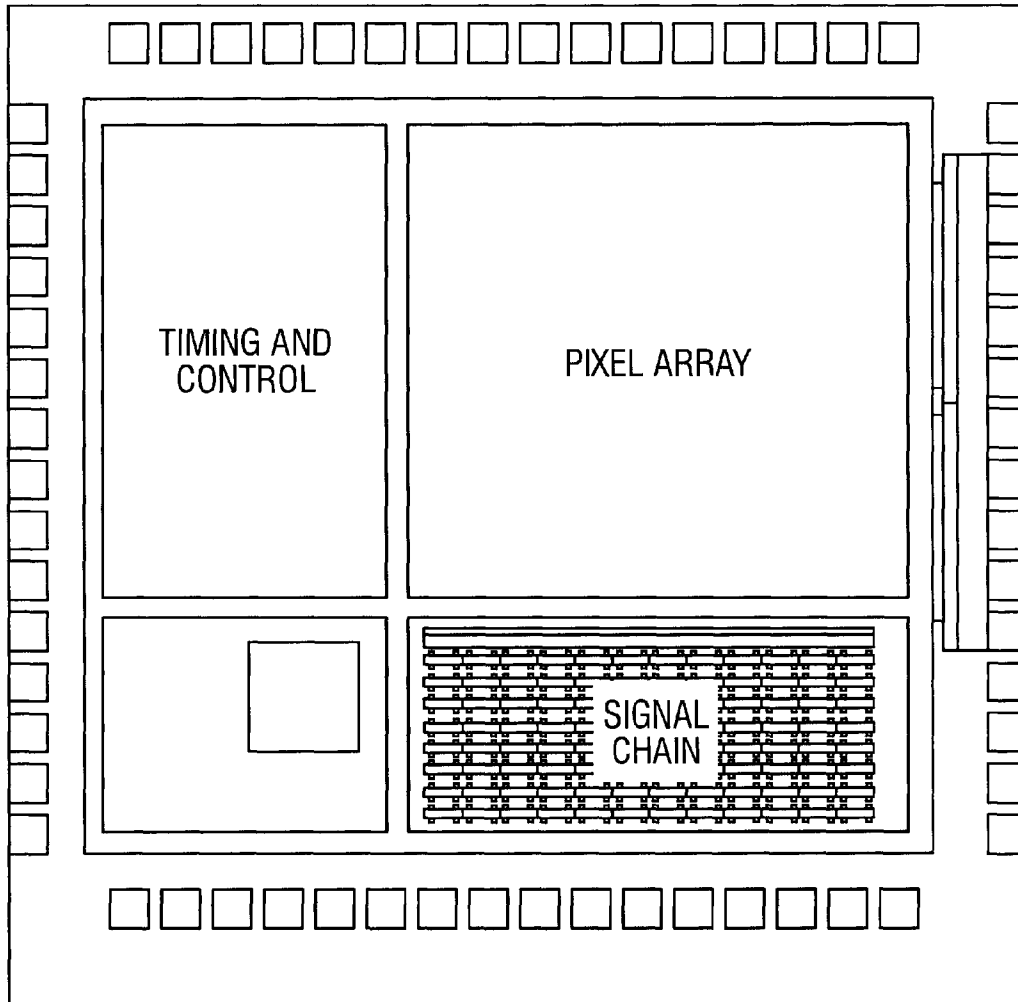


FIG. 7

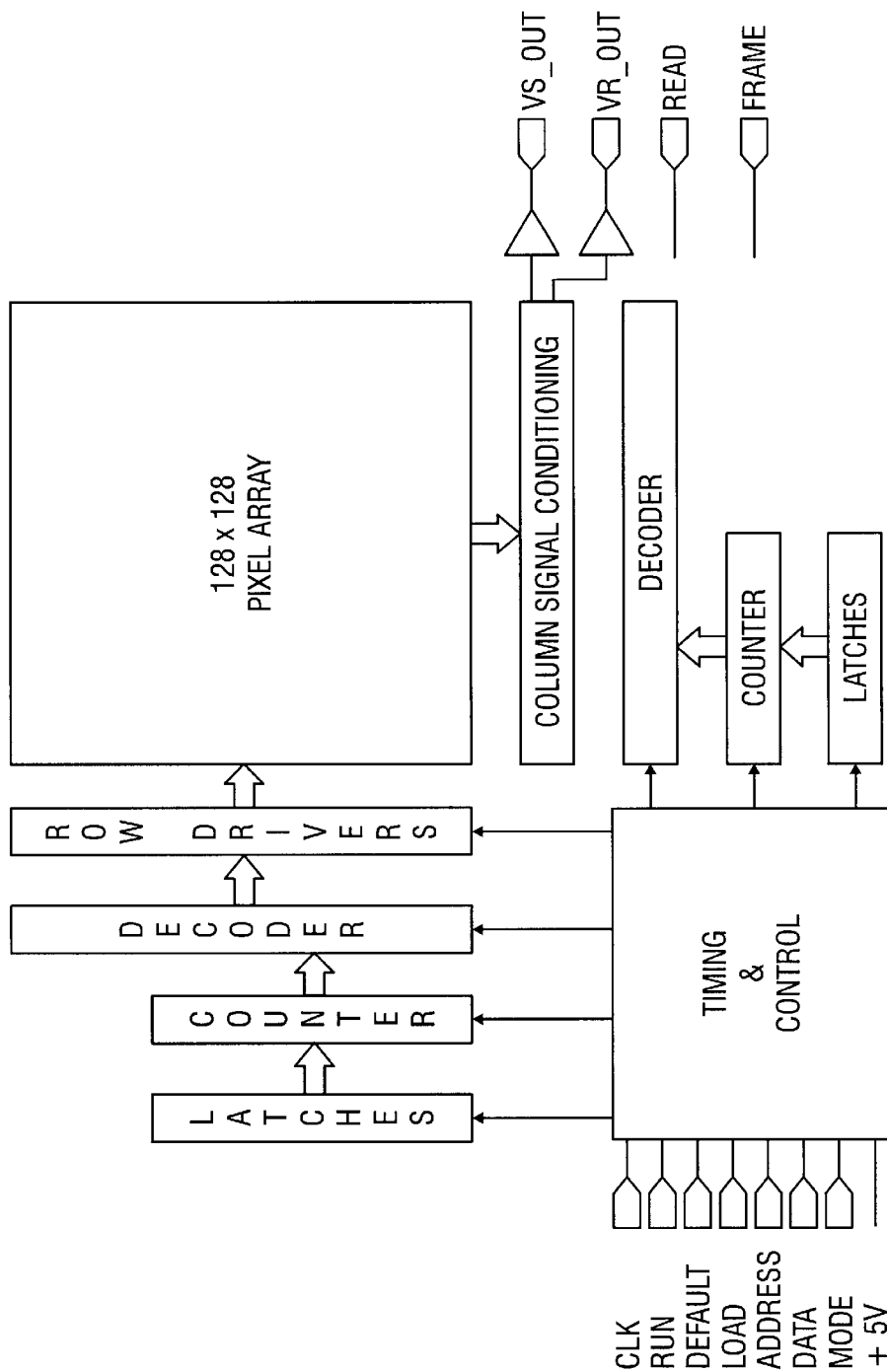
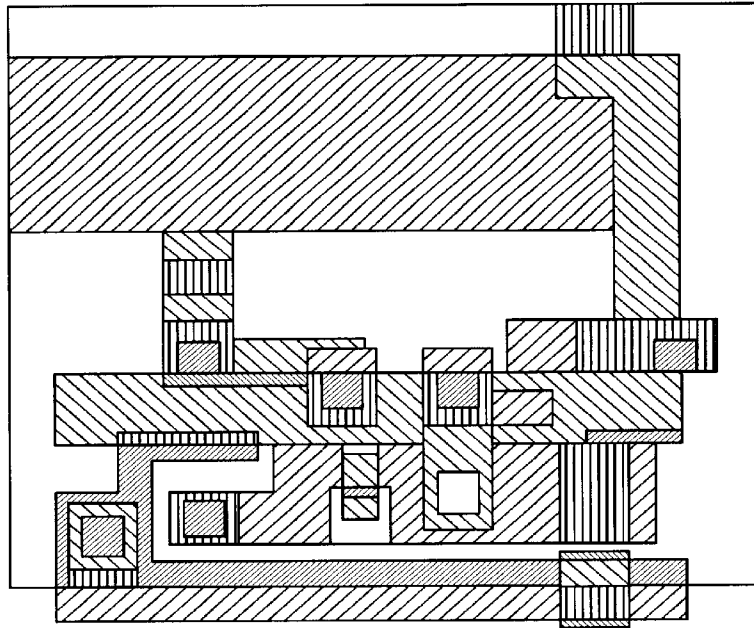
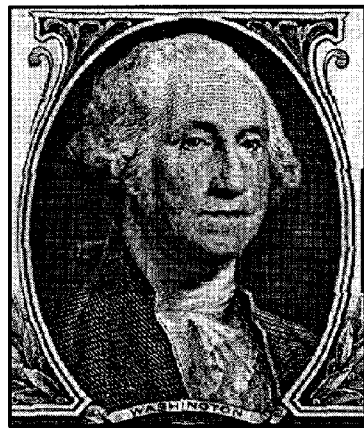
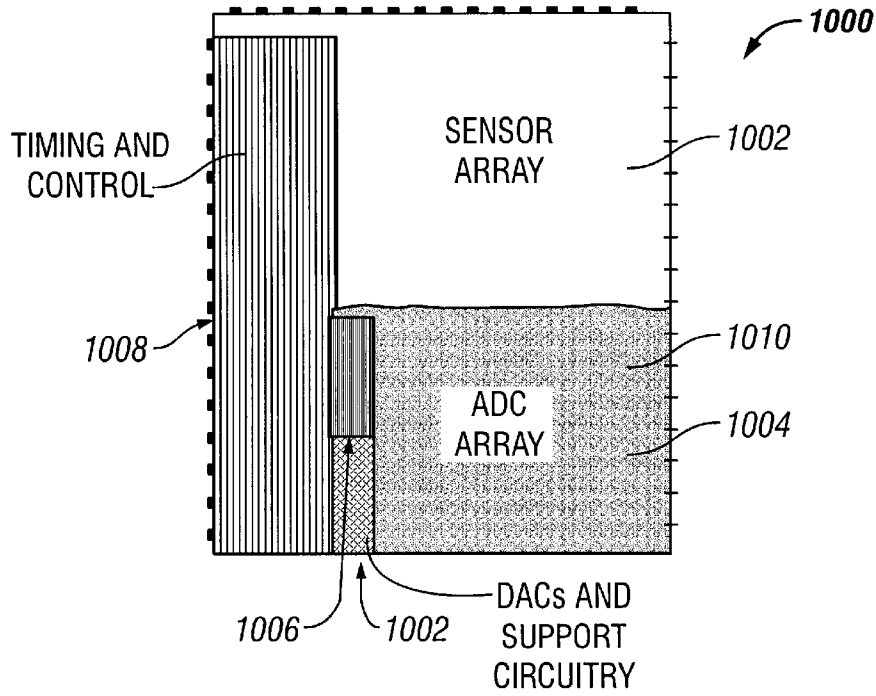


FIG. 8



Array Size	256 x 256
Pixel Size	20.4 μm
Technology	1.2 μm n-well CMOS (HP)
Maximum Clock Rate	10 MHz
Minimum Clock Rate	none
Maximum Pixel Rate	2.5 MHz
Maximum Integration Delay	16 x 10 ⁹ clock periods or 1600 secs at 10 MHz

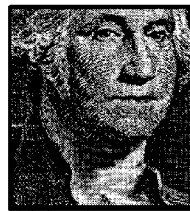
FIG. 9



Original



2 x 2 subsampling



Window of Interest

FIG. 10

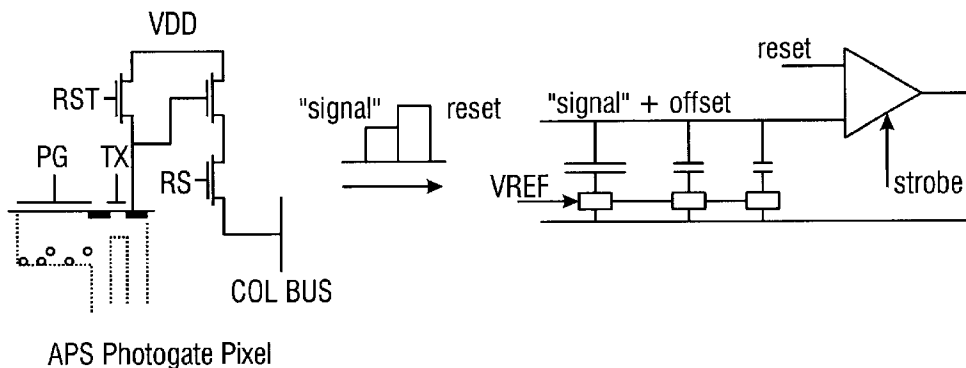


FIG. 11A

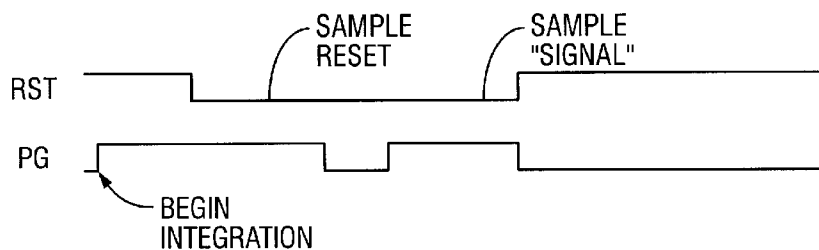


FIG. 11B

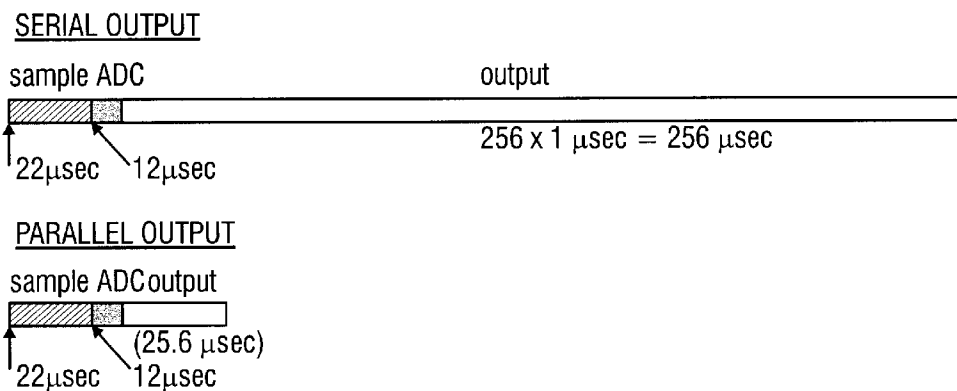


FIG. 11C

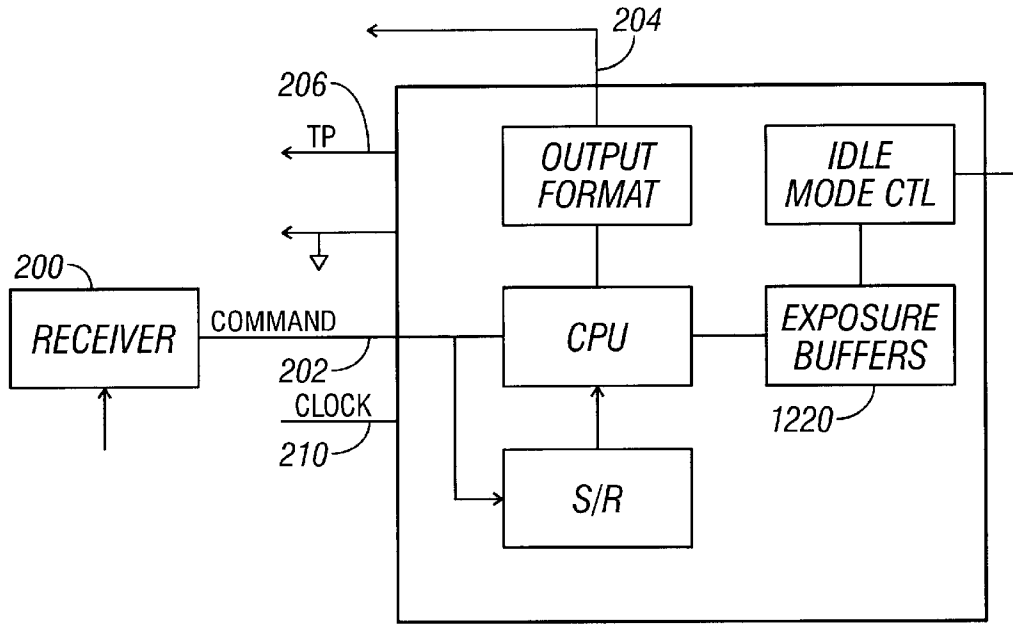


FIG. 12

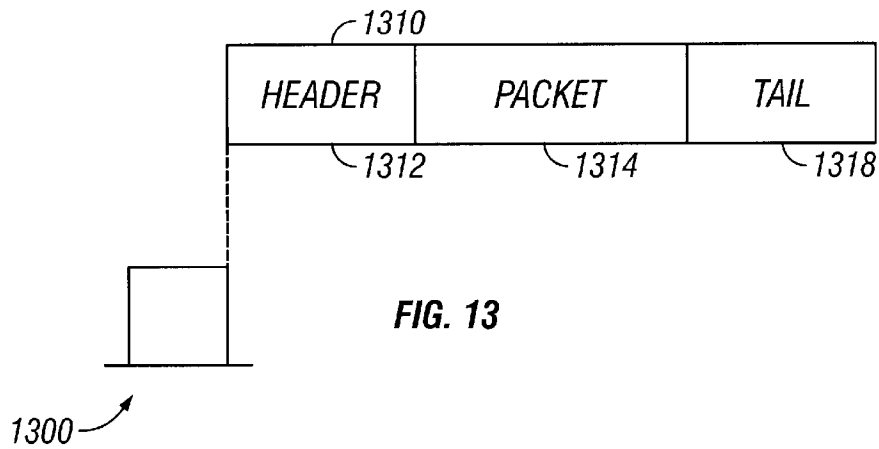


FIG. 13

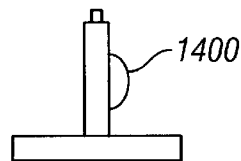


FIG. 14

SINGLE CHIP CAMERA ACTIVE PIXEL SENSOR

This claims priority from Provisional Application No. 60/060,236 having a filing date of Sep. 29, 1997.

Origin

The invention described herein was made in performance of work under NASA contract and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the contractor has elected to retain title.

FIELD OF THE INVENTION

The present invention relates to a single chip imaging sensor.

BACKGROUND AND SUMMARY

Imaging technology is the science of converting an image to a signal indicative thereof. Imaging systems have broad applications in many fields, including commercial, consumer, industrial, medical, defense and scientific markets.

The original image sensors included an array of photosensitive elements in series with switching elements. Each photosensitive element received an image of a portion of the scene being imaged. That portion is called a picture element or pixel. The image obtaining elements produce an electrical signal indicative of the image plus a noise component. Various techniques have been used in the art to minimize the noise, to thereby produce an output signal that closely follows the image.

Size minimization is also important. The development of the solid state charge coupled device ("CCD") in the early 1970's led to more compact image systems. CCDs use a process of repeated lateral transfer of charge in an MOS electrode-based analog shift register. Photo-generated signal electrons are read after they are shifted into appropriate positions. However, the shifting process requires high fidelity and low loss. A specialized semiconductor fabrication process was used to obtain these characteristics.

CCDs are mostly capacitive devices and hence dissipate very little power. The major power dissipation in a CCD system is from the support electronics. One reason for this problem is because of the realities of forming a CCD system.

The specialized semiconductor fabrication process alluded to above is not generally CMOS compatible. Hence, the support circuitry for such a CCD has been formed using control electronics which were not generally CMOS compatible. The control electronics have dissipated an inordinate percentage of the power in such imaging devices. For example, CCD-based camcorder imaging systems typically operate for an hour on an 1800 mA-hr 6 V NiCad rechargeable battery, corresponding to 10.8 W of power consumption. Approximately 8 watts of this is dissipated in the imaging system. The rest is used by the tape recording system, display, and autofocus servos.

Space-based imaging systems often have similar problems. The space based systems operate at lower pixel rates, but with a lower degree of integration, and typically dissipate 20 watts or more.

The CCD has many characteristics which cause it to act like a chip-sized MOS capacitor. The large capacitance of the MOS device, for example, requires large clock swings, ΔV , of the order of 5-15 V to achieve high charge transfer efficiency. The clock drive electronics dissipation is propor-

tional to $\Delta V^2 f$, and hence becomes large. In addition, the need for various CCD clocking voltages (e.g. 7 or more different voltage levels) leads to numerous power supplies with their attendant inefficiencies in conversion.

Signal chain electronics that perform correlated double sampling ("CDS") for noise reduction and amplification, and especially analog to digital converters (ADC), also dissipate significant power.

The inventors also noted other inefficiencies in imaging systems. These inefficiencies included fill factor inefficiencies, fixed pattern noise, clock pick up, temporal noise and large pixel size.

Active pixel sensors, such as described in U.S. Pat. No. 5,471,515, the disclosure of which is incorporated by reference herein, use special techniques to integrate both the photodetector and the readout amplifier into the pixel area or adjacent the pixel area. This allows the signal indicative of the pixel to be read out directly. These techniques have enabled use of a logic family whose fabrication processes are compatible with CMOS. This has enabled the controlling circuitry to be made from CMOS or some other low power-dissipating logic family.

The inventors of the present invention have recognized techniques and special efficiencies that are obtained by specialized support electronics that are integrated onto the same substrate as the photosensitive element. Aspects of the present invention include integration, timing, control electronics, signal chain electronics, A/D conversion, and other important control systems integrated on the same substrate as the photosensitive element.

The disclosure also describes various improvements in such a system.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a basic block diagram of a CMOS active pixel circuit;

FIG. 2 shows a graph of typical APS quantum efficiency;

FIG. 3 shows the block diagram of the overall chip including drivers and controlling structures;

FIGS. 4A and 4B show the timing diagrams for photogate operation and photodiode operation, respectively;

FIG. 5 shows a schematic of the active pixel sensor unit cell and readout circuitry;

FIG. 6 shows a timing diagram for setup and readout;

FIG. 7 shows a drawing of an actual layout of the pixel and control circuitry;

FIG. 8 shows a block diagram of a CMOS APS chip; and

FIG. 9 shows an exemplary pixel layout.

FIG. 10 shows the basic array of the improved noise reduction circuit embodiment.

FIGS. 11A and 11B show the noise reduction circuit embodiment.

FIG. 11C shows serial and parallel output from the A/D converter.

FIG. 12 shows a functional block diagram of the improved embodiment.

FIG. 13 shows a timing diagram of the serial communication.

FIG. 14 shows an alternate mounting configuration for the chip with the devicemounted on its side.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An active pixel sensor is herewith described with reference to FIGS. 1-4.

A block diagram of a CMOS active pixel circuit is shown in FIG. 1. The device has a pixel circuit **150**, and a column circuit **155**.

Incident photons pass through the photogate ("PG") **100** in the pixel circuit **150** and generate electrons which are integrated and stored under PG **100**. A number of the pixel circuits are arranged in each row of the circuit. One of the rows is selected for readout by enabling the row selection transistor **102** ("RS").

In the preferred embodiment, the floating diffusion output node **104** ("FD") is first reset by pulsing reset transistor ("RST") **106**. The resultant voltage on FD **104** is read out from the pixel circuitry onto the column bus **112** using the source follower **110** within the pixel. The voltage on the column bus **112** is sampled onto a first holding capacitor **114** by pulsing transistor SHR **116**. This initial charge is used as the baseline.

The signal charge is then transferred to FD **104** by pulsing PG **100** low. The voltage on FD **104** drops in proportion to the number of photoelectrons and the capacitance of FD. The new voltage on the column bus **112** is sampled onto a second capacitor **118** by pulsing SHR **120**. The difference between the voltages on first capacitor **114** and second capacitor **118** is therefore indicative of the number of photoelectrons that were allowed to enter the floating diffusion.

The capacitors **114**, **118** are preferably 1-4 pf capacitors.

All pixels on a selected row are processed simultaneously and sampled onto capacitor at the bottom of their respective columns. The column-parallel sampling process typically takes 1-10 μ sec, and preferably occurs during the so-called horizontal blanking interval of a video image.

Each column is successively selected for read-out by turning on column selection p-channel transistors ("CS") **130**. The p-channel source-followers **122**, **124** in the column respectively drive the signal (SIG) and horizontal reset (RST) bus lines. These lines are loaded by p-channel load transistors which can be sent directly to a pad for off-chip drive, or can be buffered.

Noise in the sensor is preferably suppressed by the above-described correlated double sampling ("CDS") between the pixel output just after reset, before and after signal charge transfer to FD as described above. The CDS suppresses kTC noise from pixel reset, suppresses 1/f noise from the in-pixel source follower, and suppresses fixed pattern noise (FPN) originating from pixel-to-pixel variation in source follower threshold voltage.

The inventors found, however, that kTC noise may be reintroduced by sampling the signal onto the capacitors **114**, **118** at the bottom of the column. Typical output noise measured in CMOS APS arrays is of the order of 140-170 μ V/e-, corresponding to noise of the order of 13-25 electrons rms. This is similar to noise obtained in most commercial CCDs, through scientific CCDs have been reported with read noise in the 3-5 electrons rms.

Typical biasing for each column's source-follower is 10 μ A. This permits charging of the sampling capacitors in the allotted time. The source-followers can then be turned off by cutting the voltage on each load transistor.

The sampling average power dissipation P_s corresponds to:

$$P_s = n I V d$$

where n is number of columns, I is the load transistor bias, V is the supply voltage, and d is the duty cycle. Using n=512, I= μ A, V=5V and d=10%, a value for P_s of 2.5 mW is obtained.

A load current of 1 mA or more is needed to drive the horizontal bus lines at the video scan rate. The power dissipated is typically 5 mW.

Quantum efficiency measured in this CMOS APS array is similar to that for interline CCDs. A typical response curve is shown in FIG. 2. The inventors noticed from this that the quantum efficiency reflects significant responsivity in the "dead" part of the pixel; the part containing the readout circuitry rather than the photogate collector. The responsiveness was measured by intra-pixel laser spot scanning.

The inventors postulate the following reason. The transistor gate and channel absorb photons with short absorption lengths (i.e. blue/green). However, longer wavelength photons penetrate through these regions. The subsequently-generated carriers diffuse laterally and are subsequently collected by the photogate.

Thus, despite a fill factor of 25%-30%, the CMOS APS achieves quantum efficiencies that peak between 30%-35% in the red and near infrared. Microlenses are preferably added to refract photoelectrons from the dead part to a live part and hence improve quantum efficiency.

An important feature of the system described herein is the integration of on-chip timing and control circuits within the same substrate that houses the pixel array and the signal chain electronics. A block diagram of the chip architecture is shown in FIG. 3.

The analog outputs VS_out (signal) and VR_out (reset) are as described above. The digital outputs include FRAME and READ. Most of the inputs to the chip are asynchronous digital signals, as described herein.

The chip includes a pixel array **300**, which is driven by on-chip electronics. Timing and control circuit **302** drives row electronics **310**, and column electronics **320**.

The control circuits can command read-out of any area of interest within the array. Row decoder **312** controls row drivers **314** which can select a certain row for readout. A specific row is selected by entry of a row value **316** which is output from timing and control **302**. Row value **316** is stored in latch **318** which drives counter **319**. Counter **319** can allow selection of subsequent rows that follow the current row. Similarly, columns can be selected and accessed by latches **322**, counter **324**, decoder **326** and column signal conditioning **328**.

Each of the decoder counters can be preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus **330**. Therefore, as described above, selection of a row commands pixels in that row to be transferred to the appropriate row decoding elements, e.g., capacitors. Preferably there is one capacitor associated with each column. This provides for the sequential readout of rows using the column. The capacitors are preferably included within the column signal conditioner **328**. Column decoders **326** also allow selection of only a certain column to be read. There are two parts of each column selection: where to start reading, and where to stop reading. Preferably the operation is carried out using counters and registers. A binary up-counter within the decoder **326** is preset to the start value. A preset number of rows is used by loading the 2's complement. The up counter then counts up until an overflow.

An alternate loading command is provided using the DEFAULT LOAD input line **332**. Activation of this line forces all counters to a readout window of 128×128.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus **330**. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. The counter can hence provide vary large integration delays. The input clock can be any frequency up to about 10 MHz. The pixel readout rate is tied to one-fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. The integration time is therefore equal to the delay time and the readout time for a 2.5 MHz clock. The maximum delay time is $2^{32}/2.5$ MHz, or around 28 minutes. These values therefore easily allow obtaining a 30 Hz frame.

The timing and control circuit controls the phase generation to generate the sequences for accessing the rows. The sequences must occur in a specified order. However, different sequences are used for different modes of operation. The system is selectable between the photodiode mode of operation and the photogate mode of operation. The timing diagrams for the two gates are respectively shown in FIGS. **4A** and **4B**. FIG. **4A** shows an operation to operate in the photogate mode and FIG. **4B** shows operating in the photodiode mode. These different timing diagrams show that different column operations are possible. Conceptually this is done as follows. Column fixed pattern noise is based on differences in source follower thresholds between the different transistors. For example, if the base bias on a transistor is V_1 , the output is V_1 plus the threshold.

The column signal conditioning circuitry contains a double-delta sampling fixed pattern noise ("FPN") suppression stage that reduces FPN to below 0.2% sat with a random distribution. Since the APS is formed of a logic family that is compatible with CMOS, e.g., NMOS, the circuitry can be formed of CMOS. This allows power dissipation in the timing and control digital circuitry to be minimized and to scale with clock rate.

An active pixel sensor includes both a photodetector and the readout amplifier integrated within the same substrate as the light collecting device, e.g., the photodiode. The readout amplifier is preferably within and/or associated with a pixel.

A first embodiment of the present invention is a 128×128 CMOS photodiode type active pixel sensor that includes on chip timing, control and signal train electronics. A more detailed drawing of the chip is shown in FIG. **5**. Asynchronous digital signals are converted by this chip to VS and VR analog outputs which are used to run the chip.

Pixel portion **500** includes a photodiode **502** which stores incident photons under photogate **504**. The photons are integrated as electrons within the photogate well. The output is buffered by follower **508**.

The rows are arranged into an array. A particular row is selected by the row transistor **514**. This allows the information from within the selected pixel **500** to be passed to the column decoder circuitry. Reset transistor **530** is connected to a sink **532**. Reset transistor is biased to a low potential level to allow all charge to bleed to sink **532**, and hence hold the stored charge in reset. The system is removed from reset by biasing the gate to a level as shown. This level is less than a highest possible potential to thereby allow charge which accumulates above that level to pass to sink **532**. Hence, the charge cannot overflow in an undesired way. This suppresses the blooming effect.

The depicted photogate system is driven according to the readout sequence shown in FIG. **6**. A row is selected by

activating row selecting transistor **514**. The cycle begins by sampling the signal present on each column pixel in that row. Sampling is initiated by biasing transistor **526** to place the signal from each column pixel in the row onto the holding capacitor **510**.

After the current pixel value has been transferred to the capacitor **510**, the pixel in the row is reset by biasing reset transistor to a low level, to photodiode **502** to the preset voltage sink **532**.

Correlated double sampling is effected by sampling the reset value, as a reset level, onto the holding capacitor **512**. This is done by activating the reset transistor **516**.

The voltage value of the reset branch of the column circuit is given by

$$V_{col_R} = \beta \{ \alpha [V_{pdr} - V_{pix}] - V_{icolr} \}$$

Where α is the gain of the pixel source follower **508**, β is the gain of the column source follower **526**, and V_{pdr} is the voltage on the photodiode after reset, V_{pix} is the threshold voltage of the pixel source follower and channel transistor, and V_{icolr} is the threshold voltage of the column source follower p-channel transistor.

Using similar reasoning, the output voltage of the signal branch of the column circuit is

$$V_{col_S} = \beta \{ \alpha [V_{pds} - V_{pix}] - V_{icols} \}$$

where V_{pds} is the voltage on the photodiode with the signal charge present and V_{icols} is the threshold voltage of the column source-follower p-channel transistor.

The inventors have found experimentally that the peak-to-peak variation $V_{icolr} - V_{icols}$ is typically between 10 and 20 millivolts. This, however, is a source of column to column fixed pattern noise. The inventors herein suggest a double delta sampling technique to eliminate this column to column noise. The present approach represents an improved version of the previously-described double delta sampling circuitry. The operation proceeds as follows. A column is first selected. After a settling time equivalent to half of the column selection period, a special double delta sampling technique is performed to remove the column fixed pattern noise. Therefore, the varying thresholds on the different transistors cause varying outputs. According to this aspect, the threshold outputs of these transistors are equalized using a capacitor to equalize the charge. The capacitor is applied with the charge before and after the voltage change. Therefore, the output of the capacitor represents the difference between before and after, and the fixed pattern noise component drops out of the equation.

This system uses a DDS switch **520** and first and second column select switches **522**, **524** to short across the respective capacitors. All three switches are turned on to short across the two sample and hold capacitors **510**. This clamp operation is shown in line **8** of FIG. **6**.

Prior to the DDS operation, the reset and signal column components, V_{col_R} and V_{col_S} include their signal values plus a source follower voltage threshold component from the appropriate source follower. The object of the special following circuit of the present invention is to remove that source follower threshold component. The operation proceeds as follows. Prior to the beginning of some operation, the capacitors are precharged through clamp transistors to a clamp voltage V_{cl} . This is maintained by turning on clamp transistors **550** and **552** to connect the appropriate capacitors to the voltage V_{cl} . The clamp operation is shown on line **8** of FIG. **6**. Immediately after the clamp is released, the DDS transistors **520**, **522** and **524** are

turned on. This has the effect of shorting across the capacitors 510 and 512. When the transistors are shorted, the voltage that is applied to the output drivers 554, 556 includes only the voltage threshold component. The differential amplification of the voltage render the output voltage free of the voltage threshold component. Mathematically, prior to clamp being deactivated, the output signals are:

$$VR_OUT = \gamma(V_{cl} - V_{tr})$$

$$\text{and } VS_OUT = \gamma(V_{cl} - V_{ts})$$

where γ is the gain of the third stage source-follower, V_{cl} is the clamp voltage, and V_{tr} and V_{ts} are the threshold voltages of the third stage source-follower n-channel transistors, reset and signal branch respectively. Deactivation of the clamp circuit and simultaneous activation of the DDS switch causes several changes. The voltages in the two column branch sampling circuits equalize becoming:

$$V_{cs} = V_{cr} = \alpha[V_{pdr} - V_{pix} + V_{pds} - V_{pix}]/2$$

This in turn causes a change in V_{col_S} and V_{col_R} to:

$$V_{col_R}' = \beta\{\alpha[V_{pdr} - V_{pix} + V_{pds} - V_{pix}]/2 - V_{icotr}\}$$

$$\text{and } V_{col_S}' = \beta\{\alpha[V_{pdr} - V_{pix} + V_{pds} - V_{pix}]/2 - V_{icots}\}$$

Consequently, the voltage outputs change to:

$$VR_OUT = \gamma(V_{cl} - V_{col_R}' - V_{col_R} - V_{tr})$$

$$\text{and } VS_OUT = \gamma(V_{cl} - V_{col_S}' - V_{col_S} - V_{ts})$$

We note

$$V_{col_S}' - V_{col_S} = \beta\{\alpha[V_{pds} - V_{pdr}]/2\}$$

$$\text{and } V_{col_R}' - V_{col_R} = \beta\{\alpha[V_{pdr} - V_{pds}]/2\}$$

When the outputs are differentially amplified off-chip, the common clamp voltage V_{cl} is removed, leaving only the difference between signal and reset. The net differential output voltage is given by:

$$VR_OUT - VS_OUT = \alpha\gamma(V_{pdr} - V_{pds} = V_{const})$$

FIG. 7 shows the layout of the pixel for 128x128 array size device. This system formed a 19.2 micron pixel size using 1.2 μm n-well CMOS. The maximum clock rate is 10 MHz, the maximum pixel rate is 2.5 MHz and maximum integration delay is 1.6×10^9 clock periods.

A second embodiment uses similar design techniques to produce a 256x256 array size. This embodiment also uses a pixel with a photogate imaging element along with four transistors to perform the functions of readout, selection, and reset. Readout is preferably achieved using a column parallel architecture which is multiplexed one row at a time and then one column at a time through an on-chip amplifier/buffer. An important part of this embodiment, like the first embodiment, is the use of a chip common logic elements to control row and address decoders and delay counters.

This embodiment allows use in three modes of operation: Photogate mode, photodiode mode and differencing mode. The photogate mode is the standard mode for this chip. The photodiode mode alters the readout timing to be similar to that for photodiode operation. The differencing mode alters the readout timing in such a way that the value of each pixel output is the difference between the current frame and the previous frame. The chip inputs that are required are a single +5 V power supply, start command, and parallel data load

commands for defining integration time and windowing parameters. The output has two differential analog channels.

The second embodiment uses the block diagram of the chip architecture shown in FIG. 8. The analog outputs of VS_OUT (signal) and VR_OUT (reset), and digital outputs of FRAME and READ. The inputs to the chip are asynchronous digital signals. The chip includes addressing circuitry allowing readout of any area of interest within the 256x256 array. The decoder includes counters that are preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus. An alternate loading command is provided using the DEFAULT input line. Activation of this line forces all counters to a readout window of 256x256.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus. A 32-bit counter operates from one-fourth the clock input frequency and is preset at each frame from the latch. This counter allows forming very large integration delays. The input clock can be any frequency up to about 10 MHz. The pixel readout rate is tied to one fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. A 30 HZ frame rate can be achieved without difficulty.

The chip is idle when the RUN command is deactivated. This is the recommended time for setting the operating parameters. However, these parameters can be set at any time because of the asynchronous nature of operation. When RUN is activated, the chip begins continuous readout of frames based on the parameters loaded in the control registers. When RUN is deactivated, the frame in progress runs to completion and then stops.

The 256x256 CMOS APS uses a system having a similar block diagram to those described previously. The pixel unit cell has a photogate (PG), a source-follower input transistor, a row selection transistor and a reset transistor. A load transistor VLN and two output branches to store the reset and signal levels are located at the bottom of each column of pixels. Each branch has a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a source-follower with a column-selection switch (COL). The reset and signal levels are read out differentially, allowing correlated double sampling to suppress 1/f noise and fixed pattern noise (not kTC noise) from the pixel.

A double delta sampling (DDS) circuit shorts the sampled signals during the readout cycle reducing column fixed pattern noise. These readout circuits are common to an entire column of pixels. The load transistors of the second set of source followers (VLP) and the subsequent clamp circuits and output source followers are common to the entire array. After a row has been selected, each pixel is reset (RESET) and the reset value is sampled (SHR) onto the holding capacitor CR. Next, the charge under each photogate in the row is transferred to the floating diffusion (FD). This is followed by sampling this level (SHS) onto holding capacitor CS. These signals are then placed on the output data bus by the column select circuitry. In the Photodiode mode this process, is reversed; first the charge under the photogate is read out and then the reset level is sampled. This non-correlated double sampling mode would be primarily used with a photodiode, i.e., non active pixel sensor, pixel.

In the differencing mode, the capacitors CS and CR are used to store the signal from the previous frame and the current frame. This is achieved by altering the timing in the following way: Rather than starting with a reset operation, the signal on the floating diffusion is read out to one of the sample and hold capacitors. This represents the previous

pixel value. The reset is then performed followed by a normal read operation. This value is then stored on the other sample and hold capacitor. The difference between these two signals is now the frame to frame difference.

A simplified expression for the output of the reset branch 5 of the column circuit is given by:

$$V_{col_R} = \beta \{ \alpha [V_r - V_{pix}] - V_{colr} \}$$

where α is the gain of the pixel source-follower, β is the gain of the column source-follower, V_r is the voltage on the floating diffusion after reset, V_{pix} is the threshold voltage of the pixel source-follower n-channel transistor, and V_{colr} is the threshold voltage of the column source-follower p-channel transistor. Similarly, the output voltage of the signal branch of the column circuit is given by:

$$V_{col_S} = \beta \{ \alpha [V_s - V_{pix}] - V_{cols} \}$$

where V_s is the voltage on the floating diffusion with the signal charge present and V_{cols} is the threshold voltage of the column source-follower p-channel transistor. Experimentally, the peak to peak variation in $V_{colr} - V_{cols}$ is typically 10–20 mV. It is desirable to remove this source of column-to-column fixed pattern noise FPN. JPL has previously developed a double delta sampling (DDS) technique to eliminate the column-to-column FPN. This approach represented an improved version of the DDS circuitry.

Sequential readout of each column is as follows. First a column is selected. After a settling time equivalent to one-half the column selection period, the DDS is performed to remove column fixed pattern noise. In this operation, a DDS switch and two column selection switches on either side are used to short the two sample and hold capacitors CS and CR. Prior to the DDS operation the reset and signal outputs (V_{col_R} and V_{col_S}) contain their respective signal values plus a source follower voltage threshold component. The DDS switch is activated immediately after CLAMP is turned off. The result is a difference voltage coupled to the output drivers (VR_OUT and VS_OUT) that is free of the voltage threshold component.

This chip uses a similar pixel cell to that shown in FIG. 5. FIG. 9 shows the layout of the pixel cell. PG and RESET are routed horizontally in polysilicon while the pixel output is routed vertically in metal 1. Metal 2 was routed within the pixel for row selection. Metal 2 was also used as a light shield and covers most of the active area outside of the pixel array. The designed fill factor of the pixel is approximately 21%.

According to another feature, a logo can be formed on the acquired image by using a light blocking metal light shield. The light shield is formed to cover certain pixels in the shape of

the logo to be applied. This blocks out those underlying pixels in the array, thereby forming a logo in the shape of the blocked pixels.

The output saturation level of the sensor is 800 mV when operated from a 5 V supply. Saturation is determined by the difference between the reset level on the floating diffusion node (e.g. 3 V) and the minimum voltage allowed on the pixel source follower gate (e.g. threshold voltage of approx. 0.8 volts). This corresponds to a full well of approximately 75,000 electrons. This can be increased by operating at a larger supply voltage, gaining about 47,000 e⁻ per supply volt.

Dark current was measured at less than 500 pA/cm².

Conversion gain ($\mu V/e^-$) was obtained per pixel by plotting the variance in pixel output as a function of mean signal

for flat field exposure. The fixed pattern noise arising from dispersion in conversion gain was under 1%—similar to the value found in CCDs and consistent with the well-controlled gain of a source-follower buffer.

The quantum efficiency of the detector was measured using a CVI 1/4 m monochromator and a tungsten/halogen light source, calibrated using a photodiode traceable to NIST standards.

FIG. 10 shows a block diagram of an improved embodiment with new developments in the single chip camera active pixel sensor.

A block diagram of the embodiment is shown in FIG. 10, which shows the architectural layout of the sensor 1000. The sensor array 100 is surrounded by electrical connection pins 1002, each of which can have a predefined function. The sensor is arranged as a number of logical portions, including the sensor array 1002, the A to D converter array 1004, the D/A converters and support circuitry 1006. One side of the chip, here the left-most portion of the chip, forms timing and control circuit 1008. The other side, here the right most portion, includes the image acquisition structure—the photosensitive array and the analog to digital converters.

In this embodiment, the A/D converter array is formed of a plurality of columnar-shaped A/D converter devices 1010, preferably one of the devices for each row of the array. When each of the columnar A/D converter devices 1010 is associated with one of the columns of the sensor, the system operates in a so-called column-parallel mode where the information is output one column at a time. There are preferably 256 of the column-parallel 10 bit successive approximation A to D converters, one arranged under each column which it is associated. Each includes internal correlated double sampling (“CDS”) and offset correction.

There are two inputs to the A to D converter. One is for the pixel reference (reset value) and the other is for the pixel “signal” value. CDS involves subtracting the pixel “signal” value from the pixel reset level for any given cycle. In operation, the pixel reset level, which is higher than the pixel “signal” value, is sampled and stored on a single fixed capacitor at one of the inputs. The pixel “signal” is sampled and stored at the other input on a bank of id logarithmically scaled capacitors, with values $C/2^n$, $C/2$, $C/4$, $C/8$, etc. The bottom plates of these capacitors are initially set to ground. There are 10 capacitors defining a 10-bit A to D converter. The voltage level “VREF”, indicated in the figure, defines the dynamic range of the A to D converter. After the two inputs have been introduced, the A to D converter operation proceeds. First, the bottom plate of the largest capacitor ($C/2$) is switched from ground to VREF. This causes the “signal” side of the A to D converter to be roughly “signal” + VREF/2. If “signal” + VREF/2 is greater than the pixel reset value, the signal side of the A to D converter is returned to its initial value by switching the bottom plate of the $C/2$ capacitor back to ground. If pixel “signal” + VREF/2 is less than the pixel reset value, the bottom plate of the $C/2$ capacitor is kept at VREF. This set of operations is repeated for the remaining capacitors, in order of size, causing the “signal” side of the A to D converter to adjust in voltage increments of VREF/4, VREF/8, etc. As the algorithm proceeds the “signal” side of the A to D converter is forever approaching the reset side, until it is equal to it, to within the precision of the A to D converter. The voltage value VREF is produced by one of the on-chip DACs; changing this value alters the dynamic range and thus the gain of the A to D converter.

Due to fabrication inaccuracies, each A to D converter will have its own particular offset that will cause fixed

pattern noise. To suppress this fixed pattern noise, each A to D converter has offset correction circuitry. On the "signal" side of the A to D converter is a secondary bank of logarithmically scaled capacitors, used for this purpose. Before reading out a frame of data, the same voltage is applied to the two inputs of the A to D converter (pixel reset). The A to D converter operation, described above, is performed with the secondary bank of capacitors. The result for a perfect A to D converter would be zero, but in this case represents the A to D converter offset. This offset voltage is added to the signal side of the A to D converter to auto-zero the A to D converter in subsequent operations.

Certain analog references are needed on the chip. These analog references are used, for example, for the successive approximation A/D converter. They are also used for biasing the operational amps, such as tail currents in the operational amps, and the like. The analog references can also be used for adjusting the gain of the A/D converter. For example, one may want a high gain A/D converter for low light, but a low gain A/D converter for higher light operations. The current consumed by the A/D converter can be increased to make the A/D conversion occur faster. These references are generated with on-chip DACs thus eliminating the need for external analog reference generators and allowing the chip to have a complete digital interface.

All of these analog references are formed from a group of on-chip D to A converters, fed with a digital input. The A to D converter conversion time is also programmable. The clock cycle of the A/D converter can be increased in order to make the A/D conversion occur faster. This requires more current through the A/D converter to provide a faster settling time. For example, if the device is being used in a wireless camera, the throughput may be bandwidth limited. Therefore, A to D converter's conversion time can be reduced to save power.

This allows many of the operations to be carried out using digital external circuitry. The camera can be programmed and receive commands through a single digital pin **1002**. The programming includes the analog references noted above, and also programmable exposure time, programmable windowing, and subsampling. Also, pixel sample and hold time can be programmed in this way, by setting the amount of time that elapses between reset and sampling of the image in the correlated double sampling circuit.

A special advantage is obtained by using a single pin to obtain all interface into the chip by serially transferring the data. This also specially advantageous when used for wireless communication, as shown in the block diagram of FIG. 2. When a wireless control is effected, the control is inherently serial. The RF signal stream can then be downconverted and input on a single digital serial pin **202**. A special advantage of this system is that no data conversion is necessary since the chip accepts a serial command in the same form as the RF stream.

This system can also be programmed into a number of different imaging modes using the support circuitry. The modes are described herein.

This system can also be programmed into to support a number of different imaging modes using the support circuitry. It can be configured to image continuously or take a digital still. After taking a digital still the camera automatically enters a low power idle mode where it consumes 10 microwatts of power. The modes include a low power idle mode. These low power idle modes are well known in the art. Here it is implemented by turning off the digital-to-analog converters on the chip. That has the effect of turning off the other circuitry. Also, a switch can be placed in series

with the analog circuitry, thereby turning off that circuitry. One of these exemplary modes is described in U.S. Pat. No. 5,504,909.

A warm-up timer can also be digitally programmed to delay image capture to some later time. A programmable warm-up timer enables determining how long to wait before capturing the image. For example, a warm-up timer may be used so that the user can take a picture of oneself. The warm-up timer uses a down counter which counts down from a digital preset number also input through the serial input pin. Hence, each of the preset numbers represents a time.

The image can be provided in a number of different formats, including serial and parallel. The preferred image format is serial 10-bits. However, one could obtain less resolution from the system. The image information can also be provided in full or half duplex.

The preferred image format: is serial 10-bits. However, one could obtain less resolution from the system. The chip can be programmed to insert edges in the serial output data stream to ease data recovery. It can also be configured to provide horizontal and vertical frame syncs and pixel, row and frame clocks. The chip can also be commanded to output the internal state of its registers. Allowing a user to verify settings such as the exposure time, window size and output data format. The way in which all of this would be done is well known in the art.

A number of pins are used to provide input to, and receive output from, the chip for various purposes. However, the system is designed to operate with only five pins, which are preferably connected to 8 of the 64 external pins. These eight essential pins are all located on one side of the chip, which reduces the post-packaging footprint area of the chip. Digital pads, when not connected, are automatically pulled to ground when the chip is powered on and thus do not require connections. This has advantages when it is desired to mount the chip in a special way, for example on the chip's edge as shown in FIG. 14.

The five necessary pins are command, clock, data out, power, and ground. These five essential pins are all on one side of the chip. This allows, for example, a lens or other such device right on the chip. The five necessary pins include command, clock, data out, power, and ground. These five essential pins are all on one side of the chip. However, since the device is preferably included in a 32-pin chip, this enables 32 minus 5 which equals 27 other pins for other operations.

The physical size of the chip is minimized by allowing only wires connected to 8 pins on the chip with split power and ground. This leaves approximately 32-8=24 other pins. Preferably, the 8 pins used for power and ground are located on one side of the imager in order to minimize the post-packaging footprint area.

FIG. 11A shows the signal chain of the one-chip device, and FIG. 11B shows the timing diagram. A major difference from the first embodiment is that the floating diffusion is normally maintained in reset. This means that a soft reset is not required.

In operation, as shown in FIGS. 11B-C, first the reset and signal pixel values are sampled. They are then subtracted, digitized and output. This enable the operation to occur in a minimal amount of time.

A block diagram of the hardware operations carried out in the support circuitry is shown in FIG. 12. FIG. 12 shows this systems being used as a wireless camera **200**, however, it could also alternatively be used in a wired operation. FIG. 12 also shows the system with only the five necessary output

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pins including the input data pin 202, output data pin 204, power and ground 206, 208, and the clock pin 210. The clock is used for synchronization, and to indicate when the operation is ready.

An input data packet is shown in FIG. 13. Line 1300 5 indicates the clock signal on line 210. The falling edge of clock signal 1300 on line 210 indicates the start of the data packet 1310. Data packet 1310 includes a header portion 1312 which is a reserved sequence, followed by a packet which has 20-bits of information, followed by a tail portion 10 1316. The packet indicates some information, either a format of the information that will follow, or the actual further data for processing.

Although only a few embodiments have been described in detail above, other embodiments are contemplated by the inventor and are intended to be encompassed within the following claims. In addition, other modifications are contemplated and are also intended to be covered.

What is claimed is:

1. A single-chip camera apparatus, comprising: 20
 - a substrate, having integrated thereon a sensor array of photosensitive elements;
 - an A to D converter circuit, operating to convert outputs of said sensor array to a digital value;
 - timing and control and support circuitry, including a serial 25 communication network,
 - said substrate including an external periphery with a plurality of sides, including connection pins extending from said periphery to circuitry inside said periphery, 30 said chip being capable of operation with only power, ground, serial, clock, and output pins, wherein all of said necessary pins are located on one of said sides of said periphery, wherein said support circuitry includes

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an analog reference voltage associated therewith, wherein a digital word is input to said input pin indicating said analog reference, and said support circuitry includes a digital-to-analog converter, located on said substrate, for producing said analog reference.

2. A system as in claim 1 wherein said analog reference is a reference for a successive approximation A to D converter.

3. A system as in claim 1 wherein said reference is an exposure time for said camera.

4. A system as in claim 1 wherein said reference is a sample and hold time.

5. A system as in claim 1 wherein said reference is a time for a warm-up timer.

6. A totally digital single-chip camera apparatus, comprising:

a substrate, having integrated thereon a sensor array of photosensitive elements;

an A to D converter circuit, on said substrate, operating to convert outputs of said sensor array to a digital value as an output; and

timing and control and support circuitry, on said substrate, including a serial communication network, receiving digital values as input,

wherein at least one circuit on said substrate includes an analog reference voltage associated therewith, wherein a digital word is input indicating said analog reference, and said support circuitry includes a digital-to-analog converter, on said substrate chip, for producing said analog reference based on said digital word.

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